High Performance and 450°C Thermal Stability with Ultra-Scaled 20nm Contact Length Enabled by Ru S/D in Vertical Channel-All-Around IGZO FET

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***Abstract*—In ultra-scaled IGZO FET, contact resistance has become a critical factor limiting transistor performance. In this work, we employed advanced interconnect metal Ruthenium (Ru) in vertical Channel-All-Around (CAA) Indium-Gallium-Zinc Oxide (IGZO) FETs as both contact layer and routing metal to achieve low contact resistance (R_C) and low BL resistance (R_{BL}). We investigated the impact of contact length (L_C) scaling from 40 nm to 20nm in CAA FETs with Ru contact and achieved good contact with L_C of 20nm by optimizing Ru etching process. Furthermore, in the scaled CAA FET with CD of 80nm, high I_{on} (@V_{GS}=2V, V_{DS}=1V) of 148μA/μm, SS of 70mV/dec, V_{TH} > 0V and an ultra-low R_C of 202Ω·μm are obtained. The fabricated devices also exhibit strong thermal stability attributed to the stable IGZO/Ru interface after 450°C 2h annealing in N_2 atmosphere. These results validate Ru as a promising S/D candidate in nanoscale IGZO FETs for high-performance monolithic 3D integration.**

***Keywords*—Ru, ultra-scaled contact length, ultra-low contact resistance, thermal stability, IGZO vertical CAA FET**

I. Introduction

Amorphous oxide semiconductor (AOS) vertical channel transistors (VCTs) are highly promising for sub-10nm dynamic random-access memory (DRAM) applications and monolithic 3D integration due to the advantages of high on/off ratio and back end of line (BEOL) compatibility [1], [2], [3]. Vertical Channel-All-Around (CAA) structure based IGZO FETs have been demonstrated to offer a viable technical route for high-density 2T0C DRAM applications owing to their $4F^2$ footprint and excellent 3D stacking potential [4], [5], [6]. To further increase integration density, the scaling of devices is required. Contact resistance (R_C) has become the bottleneck of the current improvement in ultra scaled vertical structures. Many methods have been proposed to reduce R_C of IGZO FETs. However, these methods pose challenges: using oxide electrodes (e.g., ITO) introduces significant bit line parasitic resistance (R_{BL}) [7]. Incorporating contact buffer layer between the conventional metal (e.g., TiN) and IGZO complicates the process flow [8].

Ruthenium (Ru), due to its advantages of low resistivity and high reliability at the nanoscale, has emerged as one of the promising candidates to replace copper (Cu) in advanced interconnections [9]. Furthermore, Ru features high chemical inertness and does not undergo severe oxidation during the low temperature IGZO FETs fabrication. Currently, the contact scalability of Ru as source/drain (S/D) electrodes in IGZO vertical short-channel transistors, as well as the thermal stability of Ru/IGZO contact region, still lacks systematic investigation.

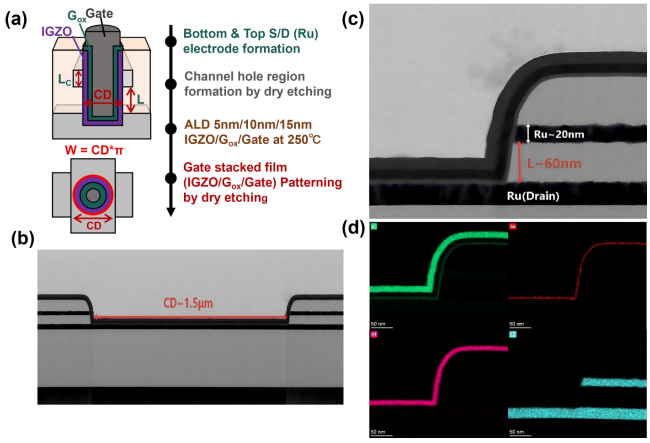

Fig. 1. (a) schematic diagram and process flow of the vertical CAA IGZO FET with Ru S/D electrode. (b) Cross TEM images of the fabricated CAA IGZO FET with CD of 1.5μm and Ru S/D electrode. (b) Right sidewall region of CAA IGZO FETs. (c) Element mapping by EDS (In, Ga, Hf and Ru)

In this work, Ru is employed as the S/D electrodes for vertical CAA IGZO FETs to achieve both low R_C and R_{BL}. By investigating the effect of L_C scaling and optimizing the Ru etching process, low R_C is obtained in the vertical CAA FETs with ultra-scaled L_C, which is of great significance for Z-pitch scaling and integration density enhancement in 3D DRAM. Furthermore, the fabricated devices show strong thermal stability due to the stable Ru/IGZO contact interface. Our results demonstrate the excellent potential of the application of Ru metal in ultra scaled IGZO FETs and monolithic 3D integration.

II. Experiments

Fig. 1(a) illustrate the schematic diagram and process flow of the vertical CAA IGZO FET with Ru S/D electrode. It is noted that the contact length (L_C) is defined by the thickness of the source/drain electrode. Firstly, Ru is deposited by PVD and etched as bottom electrode. A SiO_x layer is deposited by CVD to isolate bottom S/D. The thickness of the SiO_x spacer layer determines the channel length (L_{CH}) of the device. Then Ru is deposited by PVD as the top electrode, and another SiO_x layer is deposited by CVD. A hole is then etched to form the channel region. After that, layers of IGZO/HfO_x/IZO are deposited by ALD at 250°C as channel/G_{ox}/Gate layer. Finally, the gate stacked films are patterned by dry etching. Fig. 1(b) and (c) shows the TEM images of the fabricated CAA IGZO FETs with Ru S/D. Fig. 1(d) shows the corresponding element mapping of In, Ga, Hf and Ru. which shows a uniform distribution.

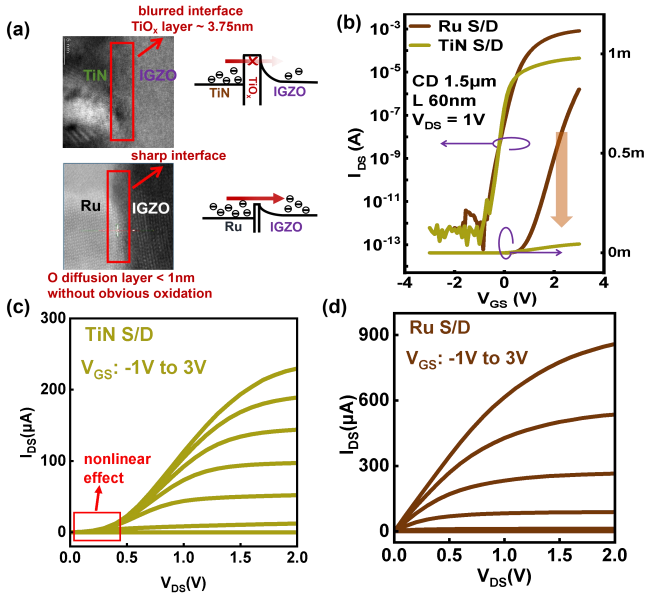

Fig. 2. (a) EELS analysis of the interface of TiN/IGZO and Ru/IGZO. (b) Comparison of the transfer curves of different materials as S/D electrodes in vertical CAA IGZO FET. (c) Output characteristics of TiN S/D and (d) Ru S/D with V_{GS} from -1V to 3V. TiN S/D exhibits obvious nonlinear effect

III. Results and Discussion

A. *The contact characteristics of TiN/IGZO and Ru/IGZO in CAA FETs*

During the fabrication process of IGZO FETs, conventional metal electrodes (e.g., TiN) are highly susceptible to oxidation, resulting in the formation of a high-resistance oxide layer, which degrades the metal/IGZO contact interface [10], [11]. Fig. 2(a) shows the contact interface of TiN/IGZO and Ru/IGZO by electron energy loss spectroscopy (EELS) analysis. In contrast to TiN, Ru and IGZO form a sharp interface at contact region with no obvious Ru oxidation detected by EELS analysis of valence state changes, which originates from the chemical inertness of Ru at low temperatures. Fig. 2(b-d) compares the transfer characteristics and output characteristics of CAA FETs with different S/D electrodes (TiN, Ru). From the output curves, the device with TiN S/D exhibits severe nonlinear effect, indicating a serious contact problem between TiN and IGZO. This is the main factor limiting the current in short-channel devices with TiN S/D. The above results indicate that, compared with conventional metal electrodes, Ru as a source/drain electrode exhibits certain advantages in IGZO vertical short-channel transistors.

B. *Contact length scaling and etching process optimization*

As we all know, contact length scaling results in higher contact resistance. We use the top electrode of the CAA as the source (when $V_{DS} > 0$, The source contact resistance is much larger than the drain contact resistance [12]) and scale the contact length (L_C) from 40nm down to 20nm to investigate the contact scalability of Ru in vertical CAA IGZO FETs (Fig. 3(a)). Fig. 3(b) and (c) show the L_C scaling results in vertical CAA FETs with Ru S/D. When L_C is scaled down to 20nm, the device still maintained a relatively high performance. Fig. 3(d) illustrates the procedure for extracting R_C of the vertical channel transistor using the Y-function method [13]. Fig. 3(e) shows the extracted R_C of the devices with different L_C. Although the

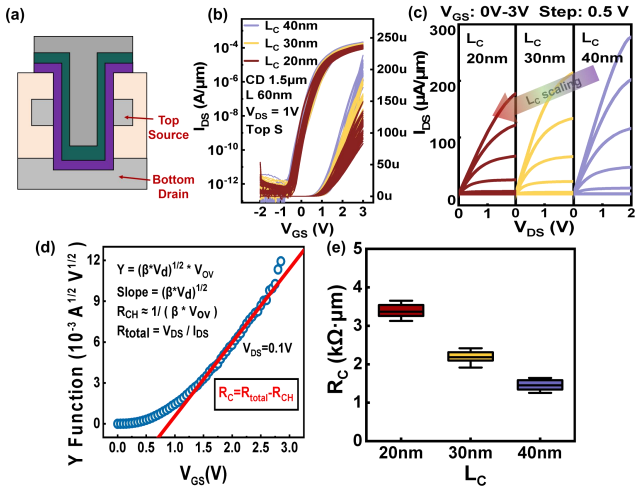

Fig. 3. (a) Schematic diagram of V_{DS} bias during electrical measurement to emphasize the top electrode R_C. (b) Transfer and (c) Output curves of CAA FET with different contact length. (d) Y-function versus V_{GS} curves from the experimental data. (e) Extracted R_C by Y-function method. When L_C is scaled down to 20 nm, the device still maintained a relatively high performance.

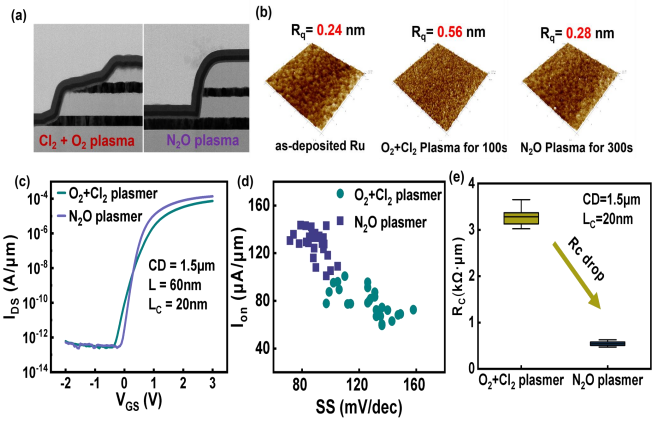

Fig. 4. (a) TEM images of etching profile with different etching methods. (b) AFM results after etching by different methods. N_2O plasma cause less etch damage to the film. (c) Transfer curves with different etching methods. (d) Comparison of the I_{on} and SS with different etching methods. (e) The extracted R_C by Y-function method.

R_C increases after L_C scaling, a relatively good contact characteristic and devices performance is still obtained.

In the device fabrication proces, improvement of the contact electrode etching method can effectively reduce the interface state density at the metal/IGZO contact interface and improve the contact resistance. For the first time, N_2O plasma is employed as a replacement for the conventional O_2 + Cl_2 plasma for etching the Ru electrode. Fig. 4(a) compares the etch profile of the devices before and after the etching method improvement. It can be seen that a superior sidewall profile is achieved using N_2O plasma. AFM was used to evaluate the Ru films after etching by different methods (Fig. 4(b)). The as-deposited Ru film exhibited a low surface roughness of 0.24nm. After N_2O plasma treatment for 300 s, the surface roughness slightly increased to 0.28nm. However, O_2+Cl_2 plasma treatment significantly degraded the surface, increasing surface roughness to 0.56nm. This indicates that, compared to O_2 + Cl_2 plasma, N_2O plasma cause less etch damage to the film. Fig. 4(c-e) show the changes of devices performance before and after the improvement of etching method. It is evident that the overall device performance is significantly improved by

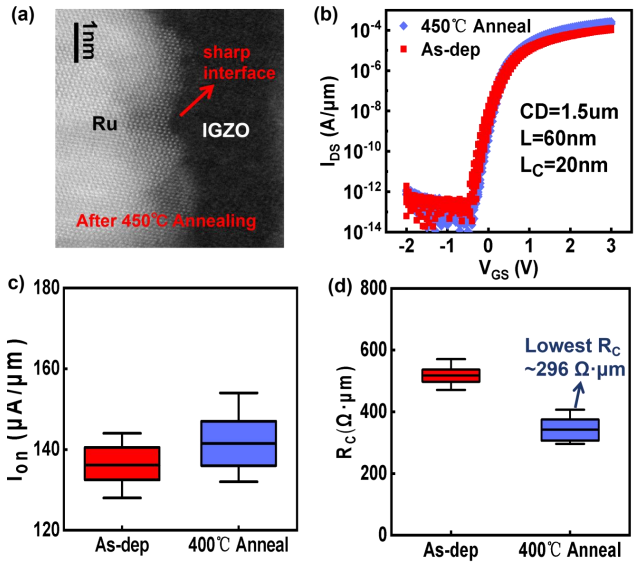

Fig. 5. (a) Sharp interface of IGZO/Ru after 450°C annealing in N_2 for about 2 hours where still no obvious oxidation can be observed. (b) Transfer curves of CAA IGZO FETs with L_C of 20nm before and after annealing. The changes of extracted parameters I_{on} and R_C are shown in (c) and (d). An ultra-low R_C of 296 Ω·μm is obtained.

using N_2O plasma etching. High I_{on} of 144 μA/μm, SS of 76 mV/dec and a low R_C of 451 Ω·μm is obtained with ultra-thin L_C of 20 nm. This demonstrates the potential of Ru as the Source/Drain electrode in the scaling vertical short channel transistors。

C. *The thermal stability of devices after 450°C annealing*

The thermal budget required for DRAM process integration is far higher than the BEOL process temperature [14]. Thus, the thermal stability to high temperature is strongly desirable. To investigate the thermal stability, the fabricated devices with Ru S/D were annealed at 450°C in a N_2 ambient for 2 h. Fig. 5(a) presents the interface of the Ru/IGZO after annealing by EELS analysis. Compared with Fig. 2(a), there is still no obvious oxidation and diffusion occurred. Fig. 5(b-d) presents the transfer curves and extracted parameter before and after annealing. The performance and contact resistance of the devices shows no degradation and an ultra-low R_C of 296 Ω·μm is obtained. This demonstrates that Ru and IGZO form a thermally stable contact interface.

D. *The performance of the further scaled CAA FETs*

Finally, we scaled the CD of CAA FETs down to 80 nm with L_{CH} of 40 nm and L_C of 30 nm. Fig. 6(a) shows the TEM images of the scaled device . Fig. 6(b) and (c) presents the transfer and output characteristics of the scaled CAA FETs. High I_{on} of 148 μA/μm and good SS of 70mV/dec is obtained. Fig. 6(d) shows the contact resistance extracted by the Y-function method. An ultra-low R_C of 202 Ω·μm is obtained. These results demonstrate that Ru can form excellent source/drain contacts in scaled short-channel IGZO FETs, exhibiting promising potential in 3D DRAM scaling.

Table I compares recent studies on contact engineering for Amorphous Oxide Semiconductor (AOS) FETs. We demonstrate for the first time the application potential of advanced interconnect metal Ru in continuously scaling vertical short-channel IGZO transistors, achieving superior device performance.

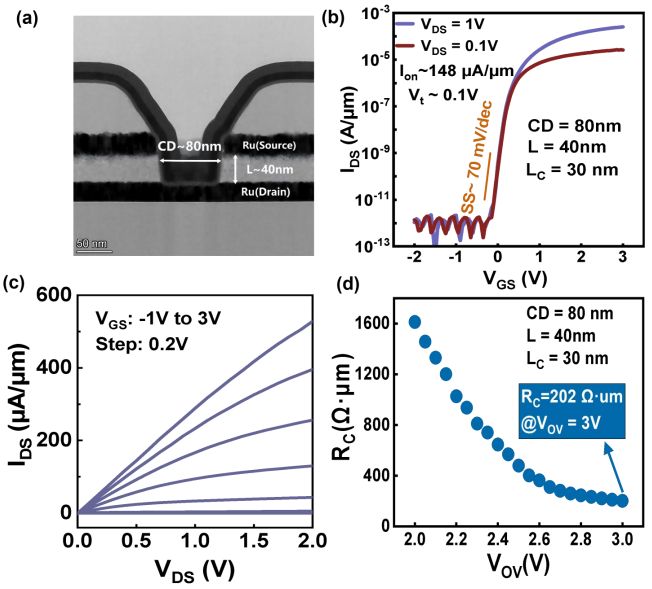

Fig. 6. (a) Cross-sectional TEM images of the scaled CAA IGZO FET with CD of 80nm, L of 40nm and Ru as S/D. (b) transfer and (c) output characteristics of the scaled CAA IGZO FET with contact length of 30nm, CD = 80nm, L= 40nm. Parameters are extracted from the curves and labeled in (a). (d) The contact resistance extracted by the Y-function method and an ultra-low R_C of 202 Ω·μm is obtained.

TABLE I. Comparison with state-of-the-art AOS FETs.

	This Work	**[15]**	**[3]**	**[16]**	**[17]**
Structure	**Vertical CAA**	**DG**	VDG	VGAA	**BG**
Channel	**IGZO**	IGZO	IGZO	IGZO	**InO**
S/D material	**Ru**	Ni	ITO	N.A	Ni
L_C(nm)	**20**	30	N.A	40	40
SS (mV/dec)	**70**	81	68	75	N.A
I_{on}(μA/μm)	**148 (V_{GS} = 2V V_{DS} = 1V)**	39.3	45.5	111.4	**1570 (V_{GS}=3V $I_{D,max}$)**
V_{TH}(V)	**0.1**	N.A	-0.3	0.13	0.01
R_C (Ω·μm)	**296 (L_C 20nm) 202 (L_C 30nm)**	340	N.A	N.A	140
Annealing	**450°C 2h**	N.A	N.A	400°C 1h	N.A

IV. Conclusion

This work offers a promising solution for IGZO vertical short-channel transistors to achieve both low R_C and low R_{BL}. Compared with traditional metals, Ru can form a more stable contact interface with IGZO. When contact length is scaled down to 20nm, the devices with Ru S/D still maintained a relatively high performance. By optimizing the etching process, an ultra-low R_C of 296 Ω·μm is obtained with ultra-thin L_C of 20 nm and CD of 1.5μm. Furthermore, a high I_{on} of 148 μA/μm and an ultra-low R_C of 202 Ω·μm are obtained in the scaled CAA IGZO FETs with CD of 80nm and L_C of 30nm. Besides, the Ru/IGZO contact interface is thermally stable. The strong thermal stability after high-temperature annealing at 450°C 2h is also demonstrated.

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