A 5V–21V Input, 42W, 95.7%-Efficient Full-Range Extended DSD (e-DSD) Converter for Fast-Charging Battery Chargers

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***Abstract*—This paper presents a full-range extended double step-down (e-DSD) converter that overcomes the traditional DSD duty-ratio limit (D < 0.5) for seamless 0-to-1 voltage conversion ratio (VCR) coverage. The proposed e-DSD topology transitions smoothly between 2- and 3-level operation without explicit mode control, featuring inherent inductor-current equalization and V_{CF} self-balancing across the full duty (D) range. Fabricated in a 180nm BCD, the e-DSD chip achieves a 95.7% peak efficiency and delivers 42W (10A) at a 21V input with 85% efficiency.**

***Keywords*—Battery charger, extended double step-down (e-DSD) converter, flying-capacitor self-balancing, inductor-current sharing, single-duty control, wide voltage conversion ratio (VCR)**

I. Introduction

Modern power converters demand high efficiency under high input voltage (V_{IN}) and heavy loads. To address this, the double step-down (DSD) converter [1] employs interleaved switching to inherently share load current (I_{Load}) via multiple inductors and balance the flying-capacitor voltage (V_{CF}). This mechanism minimizes conduction loss and switch-voltage stress. However, because the on-times of the two PWM signals cannot overlap, the DSD is limited to a duty ratio of D < 0.5 (and thus VCR (= V_O/V_{IN}) < 0.25), restricting its application to deep step-down scenarios [2]–[4]. For instance, modern mobile battery chargers [5]–[7] must accommodate both high V_{IN} (for fast charging) and legacy 5V inputs; the latter requires a VCR > 0.5—beyond the DSD limit. While 3-level converters [6]–[9] cover the full 0-to-1 VCR range, they require auxiliary loops for V_{CF} balancing [7], [8] and supervisors for multiphase current sharing [9]. Prior hybrid attempts have limitations: [10] extended VCR via multiple modes, exhibiting abrupt D jumps at boundaries. In contrast, [11] achieved seamless operation but compromised inherent current sharing and V_{CF} stability.

This paper presents a full-range extended DSD (e-DSD) converter that fully exploits the benefits of both DSD and 3-level topologies. Controlled by a single D, it enables seamless 0-to-1 VCR coverage—overcoming the D < 0.5 bound—without mode control. Furthermore, it preserves inherent inductor-current equalization and V_{CF} self-balancing, which respectively reduce the current stress on inductors and enable the use of low-voltage devices. These features make the proposed e-DSD converter well-suited for high-power (~42 W) mobile battery chargers supporting various USB-C PD inputs (5 to 21V).

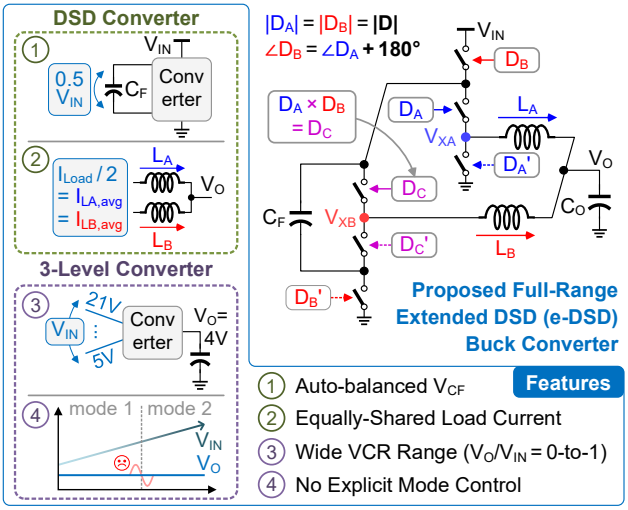


Fig. 1. Proposed full-range e-DSD converter and its key features.

II. Proposed Full-Range Extended-DSD Converter

Fig. 1 shows the proposed e-DSD converter. It comprises three switching groups driven by the PWMs D_A, D_B, and D_C. The primary D_A and D_B share the same duty ratio D (= $|D_A|$ = $|D_B|$) and are 180° out of phase ($\angle D_B = \angle D_A + 180°$), while D_C is the logical AND of the two: (D_A AND D_B) → D_C. For D < 0.5 (D_C = *low*), the switching-node voltages (V_{XA}, V_{XB}) of the two inductors (L_A, L_B) alternate between 0 and $V_{IN}/2$, exhibiting a VCR = V_O/V_{IN} = 0.5D. As illustrated in Fig. 2, the shared C_F maintains charge-balance by charging (via the L_B inductor current, I_{LB}) or discharging (via I_{LA}) whenever V_{XA} or V_{XB} is at $V_{IN}/2$. This inherent interaction (self-feedback) between V_{CF} and the two inductor currents naturally enforces I_{LA} = I_{LB} and V_{CF} = $V_{IN}/2$, as in the conventional DSD converter [1].

When D > 0.5, the on-times of D_A and D_B overlap, creating an interval with D_C = *high*, as shown in Fig. 2. The switching-node voltages (V_{XA}, V_{XB}) can now reach V_{IN}, yielding 3-level states of 0, $V_{IN}/2$, and V_{IN}. Introducing the V_{IN}-level extends the attainable VCR up to 1, governed by VCR = 1.5D – 0.5. Even in this (D > 0.5) region, charge transfer to and from C_F occurs only at $V_{IN}/2$, preserving the current-sharing (I_{LA} = I_{LB}) and voltage-balancing (V_{CF} = $V_{IN}/2$) as in the D < 0.5 case.

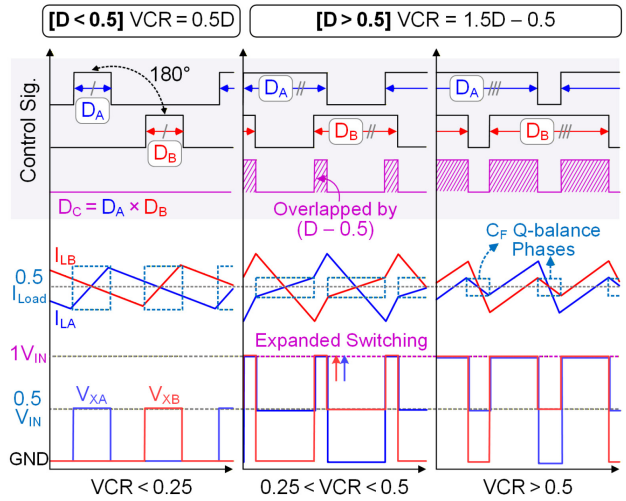


Fig. 2. Operational waveforms in different VCR (= V_O/V_{IN}) regimes.

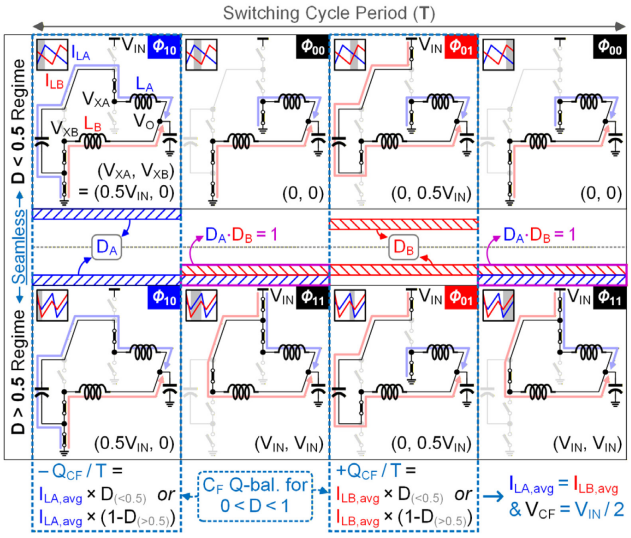


Fig. 3. Operational phases and C_F charge-balancing mechanism.

As derived from the two operating regimes, the overall VCR of the proposed e-DSD converter can be summarized as follows:

$$\text{VCR} = \frac{V_O}{V_{IN}} = \begin{cases} 0.5D, & \text{for } D \le 0.5 \\ 1.5D - 0.5, & \text{for } D > 0.5 \end{cases} \quad (1)$$

Because the entire 0-to-1 VCR range is seamlessly governed by this single duty ratio (D) and simple AND logic, the output (V_O) remains stable. This stability is maintained even during V_{IN} variations that traverse the boundary point of D = 0.5 (VCR = 0.25). Furthermore, as shown in Fig. 2, when a switching node is at $V_{IN}/2$, the inductor-current slope can be either positive or negative depending on the operating VCR, underscoring the proposed e-DSD topology's versatility.

Fig. 3 details the e-DSD operation. For $D < 0.5$, only the four D_A/D_B-associated switches toggle within each cycle (T), while the two D_C-group switches remain static. In this condition, V_{XA} and V_{XB} alternate between $V_{IN}/2$ (inductor build-up) and 0 (freewheeling). C_F is discharged by I_{LA} during Φ_{10} (for $D \cdot T$) and charged by I_{LB} during Φ_{01} (also for $D \cdot T$). Because these intervals are equal, charge balance on C_F dictates that $I_{LA,avg} = I_{LB,avg}$, which in turn auto-balances V_{CF} to $V_{IN}/2$. For $D > 0.5$, D_A and D_B overlap. This creates Φ_{11}, which activates the D_C-group switches and forms a direct path that simultaneously energizes both L_A and L_B from V_{IN}. The non-overlapping intervals mirror the ($D < 0.5$) case, where C_F balances charge over equal durations of $(1–D)\cdot T$. This equality ensures $I_{LA,avg} = I_{LB,avg}$ and maintains V_{CF} at $V_{IN}/2$ across the full range ($0 < D < 1$).

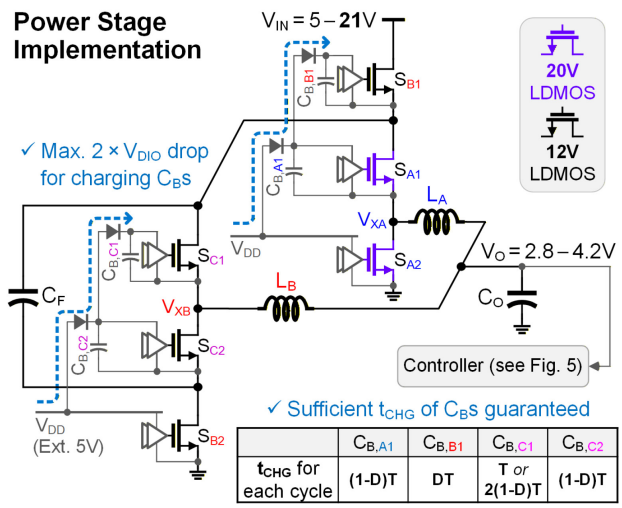


Fig. 4. Circuit-level implementation of the main power stage.

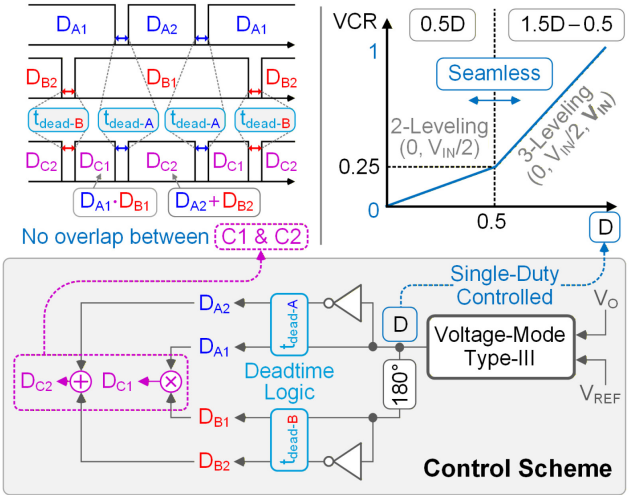
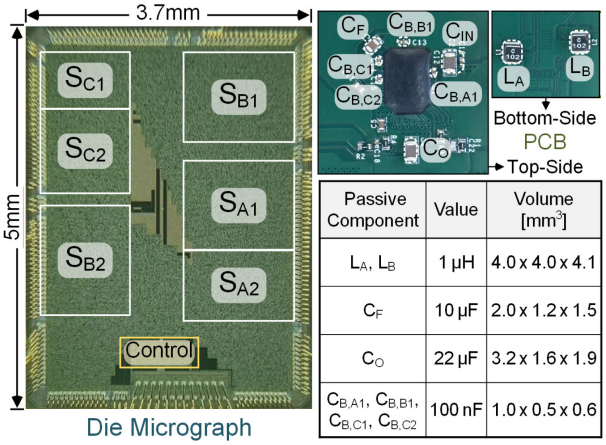


Fig. 5. Single-duty (D)-based control scheme with dead-time logics.

III. Circuit-Level Implementation

Fig. 4 depicts the e-DSD power stage designed with two 20V and four 12V LDMOS transistors for a 21V maximum V_{IN}. The auto-balanced V_{CF} allows the use of lower-R_{ON} 12V devices. Four bootstrap capacitors (C_Bs), sourced from a 5V supply via at most two diode drops, supply the high-side turn-on V_{GS}. Sufficient charging time (t_{CHG}) is ensured as the bottom-plate switches conduct for an adequate duration, even at $D \approx 0.5$.



Passive Component	Value	Volume [mm³]
L_A, L_B	1 µH	4.0 x 4.0 x 4.1
C_F	10 µF	2.0 x 1.2 x 1.5
C_O	22 µF	3.2 x 1.6 x 1.9
$C_{B,A1}$, $C_{B,B1}$, $C_{B,C1}$, $C_{B,C2}$	100 nF	1.0 x 0.5 x 0.6

Fig. 6. Die micrograph, test PCB, and details of the components used.

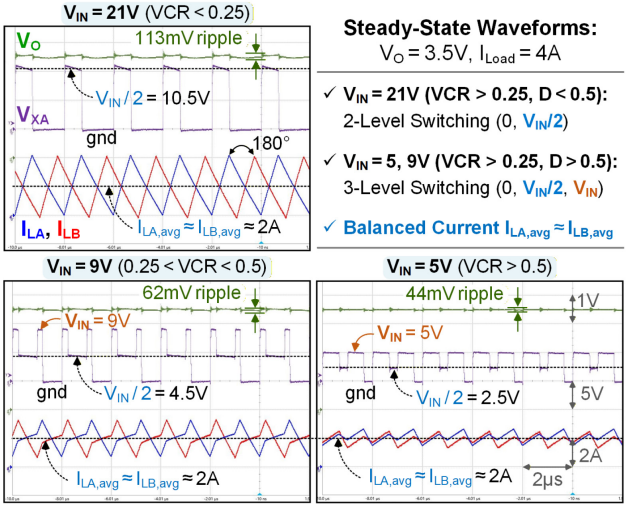


Fig. 7. Measured steady-state waveforms at different V_{IN} conditions.

Fig. 5 shows the output-voltage (V_O) regulation scheme, where a voltage-mode type-III controller generates a single D covering the full 0-to-1 VCR range. A seamless transition between the $D < 0.5$ and $D > 0.5$ regimes is achieved by simply sweeping D without any explicit mode control. Regarding the gate logic, dead-time blocks process D and its 180°-shifted version to produce non-overlapping pairs: D_{A1} (= D_A) / D_{A2} (= D_A') and D_{B1} (= D_B) / D_{B2} (= D_B'). Then, D_{C1} (= D_C) and D_{C2} (= D_C') are derived as $D_{A1} \cdot D_{B1}$ and $D_{A2} + D_{B2}$, respectively. This simple logic inherently guarantees the dead time between D_{C1} and D_{C2}, eliminating the need for extra delay blocks.

IV. Measurement Results

The 42W e-DSD converter chip was fabricated in a 180nm BCD process, as shown in Fig. 6, which also includes the detailed specifications of the passive components used. Fig. 7 presents steady-state waveforms at V_O = 3.5V and I_{Load} = 4A. V_{XA} confirms 2-level switching (0 to V_{IN}/2) for V_{IN} = 21V ($D <$ 0.5) and 3-level states (0, V_{IN}/2, V_{IN}) for V_{IN} = 9V and 5V ($D >$ 0.5), while consistently maintaining $I_{LA} = I_{LB} = I_{Load}/2$ (load sharing) and $V_{CF} = V_{IN}/2$ (C_F balancing).

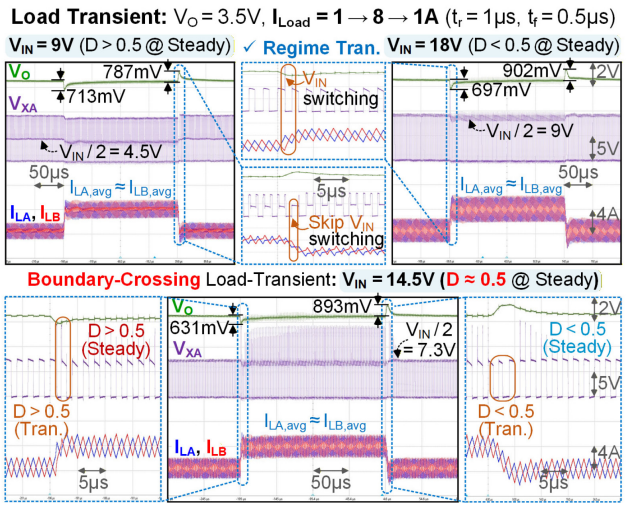


Fig. 8. Measured load-transient waveforms with 1↔8A load steps.

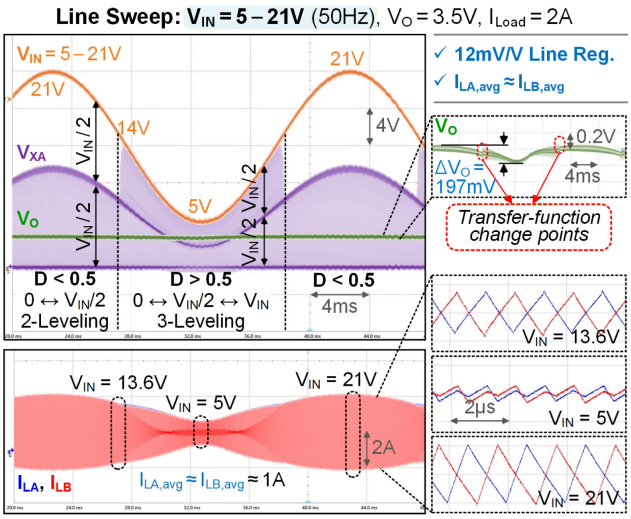


Fig. 9. Line-transient response during a wide V_{IN} sweep (5–21V).

Fig. 8 demonstrates seamless transitions during load steps. For V_{IN} = 9V (steady $D >$ 0.5), an 8A→1A load step drives D below 0.5. Conversely, at V_{IN} = 18V (steady $D <$ 0.5), a 1A→8A step momentarily pushes D above 0.5. These dynamic crossings around D = 0.5 verify robust single-duty control, as further evidenced by the load-transient waveform measured at a steady $D \approx$ 0.5. This single-duty control allows immediate I_L slope adjustment, improving output voltage recovery as seen in the response to a Δ7A load-step transient condition.

Fig. 9 shows the line-transient response as V_{IN} sweeps from 5V to 21V. V_{XA} exhibits 2-level switching between 0 and V_{IN}/2 for $V_{IN} >$ 14V (i.e., $D <$ 0.5) and transitions to 3-level switching (reaching V_{IN}) for $V_{IN} <$ 14V (i.e., $D >$ 0.5); in both regions, the intermediate rail remains at $V_{CF} \approx V_{IN}/2$. The inductor-current traces confirm $I_{LA} = I_{LB}$ throughout the sweep. The measured ΔV_O is 197mV over ΔV_{IN} of 16V: line regulation = 12mV/V.

Table I. PERFORMANCE SUMMARY OF THE PROPOSED E-DSD CONVERTER

	Battery Chargers			Multiphase Converters		This Work
	TI BQ25910 [6]	ISSCC'23 [5]	ISSCC'25 [7]	ISSCC'24 [10]	ISSCC'25 [2]	
Process	–	0.18µm BCD	0.13µm BCD	0.13µm BCD	0.18µm BCD	**0.18µm BCD**
Topology	3-Level Buck	Re-Cfg SIMS	3-Level Buck	AID	SI	**e-DSD**
Input V_{IN}	3.9 – 14V	5 – 24V	4.75 – 12V	3.3 – 5V	12V	**5 – 21V**
Output V_O	2 – 4.8V	2.8 – 4.2V	3.4 – 4.6V	0.3 – 4.7V	1 – 1.8V	**2.8 – 4.2V**
SW Freq. (f_{SW})	0.75MHz	0.6MHz	0.35MHz	2.5MHz	2MHz	**0.5MHz**
Components	1L 1C 4SW[(c)]	1L 2C 7SW	1L 1C 4SW[(c)]	2L 1C 6SW	3L 6C 15SW	**2L 1C 6SW**
Inductor	0.47µH	2.2µH	0.33µH	0.47µH x 2	0.6µH x 3	**1µH x 2**
Flying Capacitor	(2 x 10)µF	5.8µF, 10µF[(b)]	(2 x 10)µF	10µF	1µF x 6[(b)]	**10µF**
Die Area	5.9mm^2	9.4mm^2	18.5mm^2	2.3mm^2	6mm^2	**18.5**mm^2
Max I_{Load} / P_O	6A / 22.8W	5A / 21W	3A / 13.8W	1.5A / 5.4W	6A / 9W	**10A / 42W**
Peak Efficiency (V_{IN} / V_{OUT} / I_{Load}) [V / V / A]	95.4% (5 / 3.8 /1.5)	94.8% (5 / 3.6 / 0.9[(a)])	96.8% (5 / 4.6 / 1)	97.2% (4.2 / 3.6 / 0.5)	92.9% (12 / 1.8 / 2)	**95.7% (5 / 4.2 / 2)**
Eff. @ max I_{Load} (V_{IN} / V_{OUT} / I_{Load}) [V / V / A]	88.3%[(a)] (12 / 3.8 / 6)	87.8%[(a)] (24 / 4.2 / 5)	94.6%[(a)] (5 / 4.6 / 3)	84.0%[(a)] (4.2 / 3.6 / 1.5)	79.7%[(a)] (12 / 1 / 6)	**85.0% (21 / 4.2 / 10)**
Full VCR (0–1) Coverage	✓	✓	✓	✓	✗	✓
V_{CF} Self-Balance	✗	✗	✗	✓	✓	✓
C_F Soft-Charging	✓	✗	✓	✓	✓	✓
No Explicit Mode Control	✓	✗	✓	✗	✓	✓

[(a)] Estimated from figure, [(b)] Effective capacitance, [(c)] Counts only the devices in the power stage

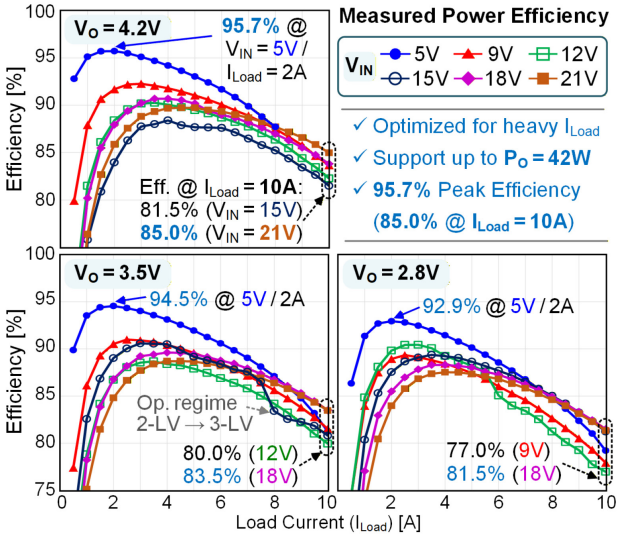


Fig. 10. Measured power conversion efficiency.

Fig. 10 plots the measured efficiency. A peak efficiency of 95.7% is achieved at V_{IN} = 5V and I_{Load} = 2A. Even at V_{IN} = 21V, the chip sustains 85% efficiency at I_{Load} = 10A (P_O = 42W). A slight efficiency drop can be observed at a nominal VCR just below 0.25, which is an expected behavior since the number of actively switching devices increases due to the load-induced transition from 2-level to 3-level switching operation.

Table I compares the performance of the proposed full-range e-DSD converter chip against state-of-the-art battery chargers and multi-phase converters. This work demonstrates the highest output power (42W) over a wide V_{IN} range (5 to 21V), making it well-suited for universal fast-charging battery chargers. Additionally, it inherently achieves both V_{CF} and I_L self-balancing across the entire 0-to-1 duty (and thus VCR) range.

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