A 250kHz BW PPD DT-DSM with Embedded Charge Sharing GES NSSAR-QTZ Achieving 92.0dB SNDR and 180.1dB FoMs

Yining Zhao, Lingxin Meng, Liang Zhao and Zhichao Tan
Institute of Very Large-Scale Integrated Circuit Design, Zhejiang University, Hangzhou, China
Email: zhichaotan@zju.edu.cn

***Abstract*—This paper presents a 4th-order DT-DSM with embedded noise-shaping SAR (NSSAR) quantizer, featuring a hybrid pseudo-pseudo-differential (PPD)/fully-differential (FD) structure and a 2-2 NS cascade for high resolution under low OSR. The loop utilizes auto-zeroing inverters in a PPD scheme to mitigate noise and area overhead while maintaining high efficiency. A simple and efficient charge sharing gain error shaping (CSGES) technique is proposed for the NSSAR, effectively mitigating open-loop gain variations and ensuring a robust and sharp NTF. Tri-level CDAC units are adopted for digital circuits simplicity, including DWA. Furthermore, high parallelism is achieved by introducing an early-release feedforward (ERF) operation, which enables simultaneous loop filter and NSSAR integration. Fabricated in 65nm CMOS, the prototype achieves 92.0 dB SNDR over a 250 kHz bandwidth with an OSR of 25 while consuming 385 µW, yielding a 180.1 dB Schreier FoM.**

***Keywords*—Pseudo-pseudo-differential, charge sharing GES, DT-DSM, NSSAR-QTZ**

I. Introduction

High-resolution, sub-MHz-bandwidth data converters with low power consumption are essential for medical imaging and sensor applications. While noise-shaping (NS) SARs offer a compact, energy-efficient solution with low OSR, their pursuit of high accuracy often necessitates calibration for mismatch errors [1,2]. High-order DT-DSMs offer high resolution but compromise speed and stability. Embedding an NSSAR within a DSM effectively enhances shaping order with reduced complexity. However, prior arts like DNC-based NSSAR-QTZ need complex digital logic and are limited by accuracy [3], while other designs suffer from limited parallelism, restricting speed [4]. As speed and precision scale, the loop integrator becomes a key bottleneck. Traditional OTAs require elaborate biasing, whereas low-power FIAs incur large area overhead from large reservoir capacitors, whose fast switching can induce severe supply fluctuations (Fig. 1, top). These limitations motivate a more optimized topology for high-resolution, high-speed operation.

To overcome the limitations of existing work, this paper introduces a PPD 4th-order DT-DSM with an embedded NSSAR-QTZ, achieving high resolution under low OSR via a 2-2 noise-shaping cascade. The design features a PPD loop filter with auto-zeroing amplifiers (for low-frequency noise suppression and efficiency), tri-level CDAC units for simplified logic including DWA, and a CSGES technique used in NSSAR for stable NTF, all while maintaining a fully-differential core signal path. High loop-quantizer parallelism is achieved, enabling a measured 92.0 dB SNDR over 250 kHz bandwidth with a OSR of 25, which corresponds to a 180.1 dB Schreier FoM.

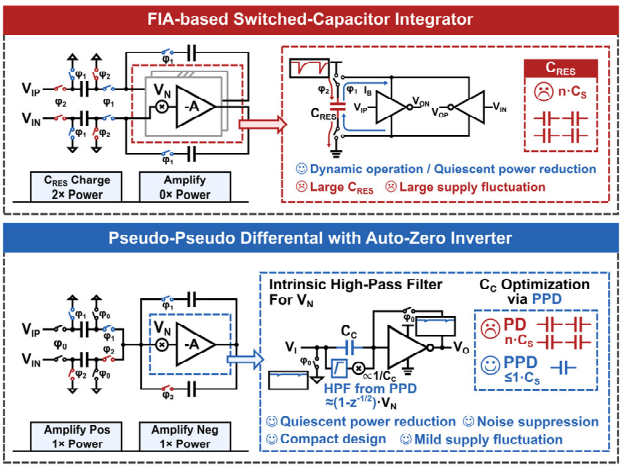


Fig. 1. Limitations of FD with an FIA and advantages of PPD with an auto-zeroing inverter.

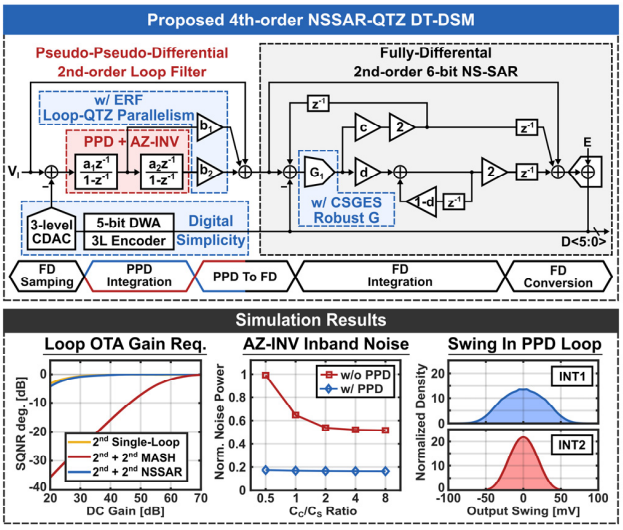


Fig. 2. Block diagram of the proposed DT-DSM and corresponding simulation results.

II. Fourth-order DT-DSM with CSGES NSSAR-QTZ

A. PPD with Auto-Zeroing Inverter Amplifiers

Inverter amplifiers offer a simple and efficient solution when using auto-zeroing technique for self-biasing, whereas the induced noise folding requires large auto-zeroing capacitor C_C for suppression [5]. To mitigate this, three-phase PPD structure is employed to reduce amplifier noise [6]. As shown in Fig. 1 (bottom), the input is first sampled

differentially at φ_0. Time-sharing the inverter amplifier during φ_1 and φ_2 inherently provides a high-pass filtering effect, shaping the noise. Consequently, C_C can be reduced to within the size of C_S, leading to significant area savings, reduced supply fluctuations and improved settling performance. Further, low quiescent current is achieved by prioritizing integration (φ_1/φ_2) over reset (φ_0).

B. Architecture Analysis

Fig. 2 (top) shows the block diagram of the proposed DT-DSM, which features a 2-2 NS cascade incorporating a 2nd-order 6-bit NSSAR-QTZ, yielding a sharper and robust NTF at low OSR, thereby improving both speed and resolution. Tri-level encoding and weight adjustment permit a 5-bit DWA, thus simplifying digital circuit complexity.

Unlike prior PPD implementations [6-8], this design isolates the PPD operation to the integrators, while preserving fully-differential operation elsewhere for robust integrity. This architecture operates effectively with a DC gain of only 30 dB, while both the noise suppression effect enabled by PPD in the inverter amplifier and the integrator swing are illustrated in Fig. 2 (bottom).

C. Proposed Charge Sharing GES NSSAR-QTZ

Even when used as a quantizer, handling non-idealities in the NSSAR NTF remains an issue. For open-loop integrator architectures targeting high-speed operation, gain variation dominantly affects the NTF, making efficient gain shaping essential (Fig. 3). Gain error shaping (GES) has proven effective for mitigating open-loop gain error by subtracting a reference voltage V_{EST} (e.g., the previous output) and injecting V_{EST}/G at the input, where G is the open-loop gain [9,10]. However, traditional implementations face challenges in architectural complexity and shaping effectiveness.

This work proposes an efficient charge sharing GES (CSGES) technique, as illustrated in Fig. 3 (bottom), derived from the insight that the delayed feedback summing is mathematically equivalent to an integration. Thus, a passive integrator can be used for significantly reducing power and complexity. Inherent attenuation (1/k) is compensated by scaling the open-loop gain by a factor of k, a feasible trade-off given the low initial gain. Finally, input feedback is realized via charge sharing across parallel capacitors.

Fig. 4 (left) shows the conventional open-loop topology performing 1st-order shaping. The proposed NS filter incorporating CSGES is shown in Fig. 4 (middle). Its implementation requires only a single additional capacitor, C_{GES}. After the amplification, a passive integration between C_{EX} and C_{GES} performs the GES operation at the output. The charge on C_{EX} is then passive integrated with C_{INT*}, where input feedback is inherently incorporated through the C_{EX}/C_{INT*} ratio, effectively realizing the required subtraction. It is straightforward to extend the 1st-order NS filter using the CSGES technique to a 2nd-order NS filter, as shown in Fig. 4 (right).

The simulated NTF and SQNR degradation versus gain variation is also shown in Fig. 4 (bottom), where k is chosen as 3 which is sufficient for shaping under 25 OSR. Thus, the proposed CSGES technique realizes highly efficient gain-error shaping using only one extra capacitor, achieving robust NTF with extreme circuit simplicity.

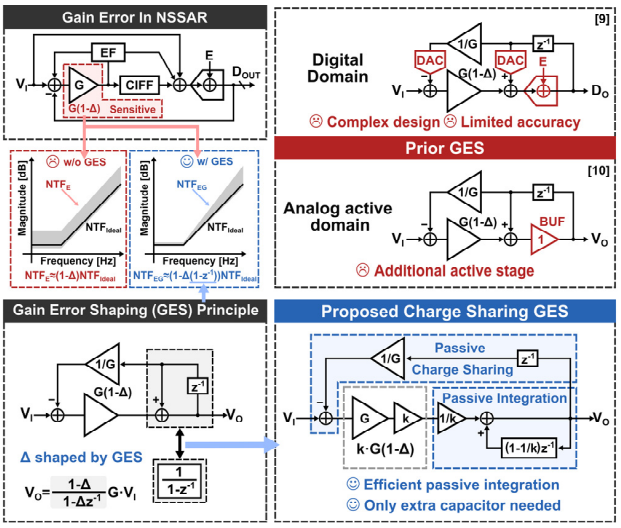


Fig. 3. Effect of gain error on NTF in NSSAR, GES principle, conventional GES, and the proposed CSGES.

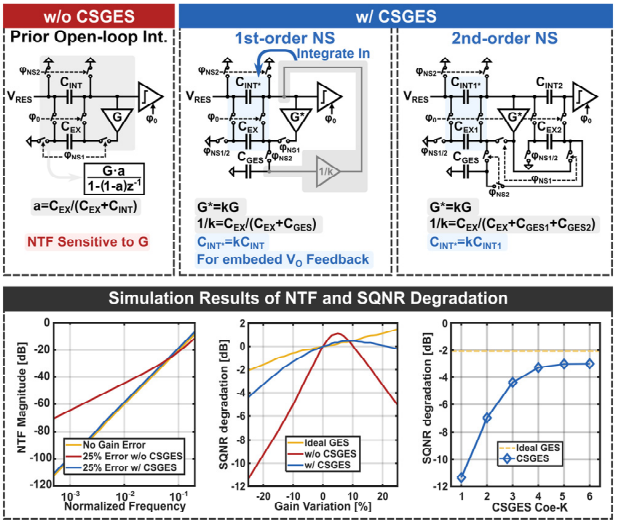


Fig. 4. Detailed implementation of the proposed CSGES in NS filter, along with simulated NTF and SQNR comparison.

D. Circuit Implementation with Clock Scheme

Fig. 5 shows the schematic of the proposed 4th-order DT-DSM with its timing diagram, featuring a hybrid PPD/FD operation. The PPD clock phases (φ_0, φ_1, φ_2) are allocated 1/5, 2/5, and 2/5 of the period to maximize integration time and reduce reset power. The feedback employs a tri-level C_{DAC}, where modified SAR weights (31,16,8,4,2,1) and tri-level encoding of the digital output allow the DWA to be restricted to a 5-bit operation operating only on the LSBs, thereby simplifying the digital logic [11]. A cascode inverter is employed as the amplifier in the loop filter integrators, chosen for its stable gain and lower input parasitic capacitance, which promotes faster integration. The NSSAR employs an FIA in an open-loop configuration, with cross-coupled capacitors C_C placed between the non-inverting input and output. A 5-pF C_{S1} is used to tackle thermal noise. Inherent phase delays between the positive and negative PPD paths are actively compensated by a ping-pong C_{F3} in one path, ensuring proper alignment.

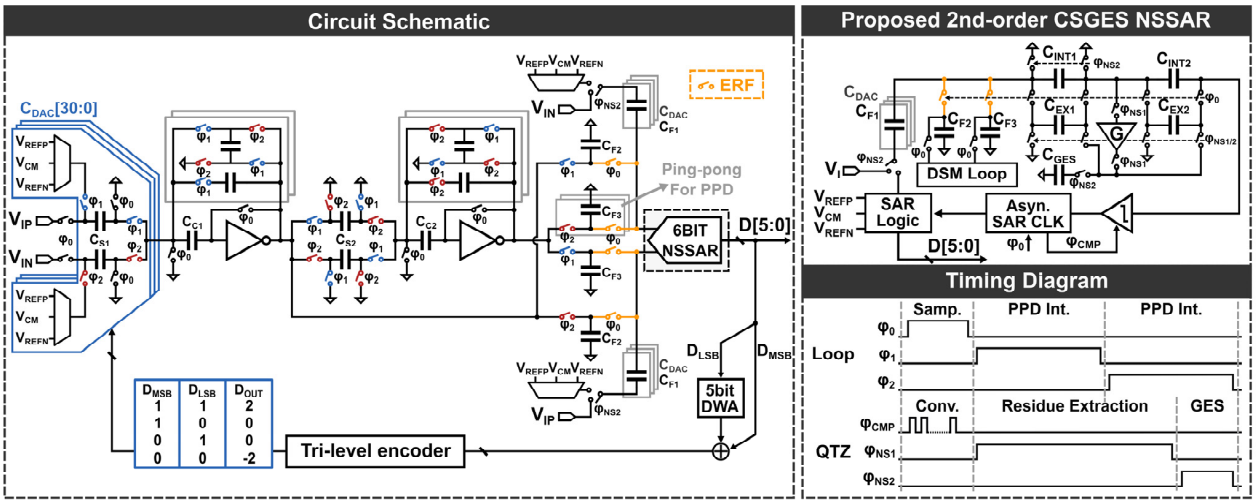


Fig. 5. Schematic of the proposed DT-DSM with NSSAR-QTZ and timing diagram.

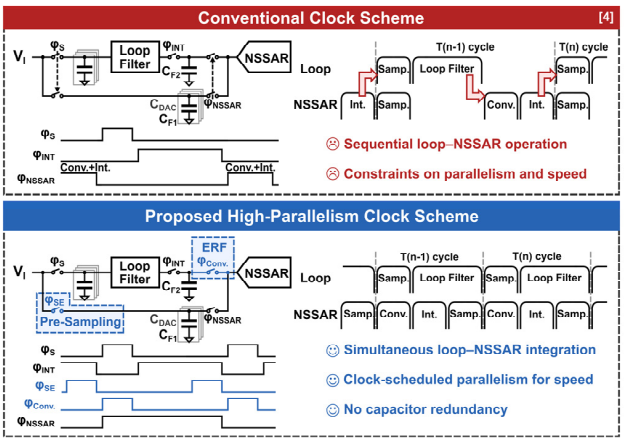


Fig. 6. Conventional and proposed clock schemes for NSSAR-QTZ DSM.

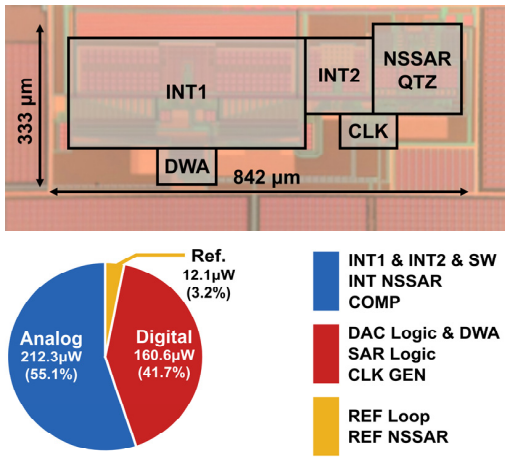


Fig. 7. Chip micrograph and power breakdown.

Unlike previous works (Fig. 6, top), this paper proposes an early-release feedforward (ERF) operation to enable simultaneous integration in both the loop filter and the NSSAR. Specifically, the feedforward capacitors switch back to the loop filter upon quantization to store the new voltage, leaving only C_{F1} to hold the residue for integration in NSSAR, as illustrated in Fig. 6 (bottom). The open-loop integration is unaffected for residue voltage unchanged. Critical timing conflicts are further resolved by pre-sampling C_{F1}. Thus, clock-scheduled parallelism is achieved for speed.

III. Measurement Results

The prototype ADC is fabricated in a 65nm CMOS, occupying an active area of 0.28mm^2. The chip micrograph is shown in Fig. 7. Clocked at 12.5MHz, the ADC consumes 385 µW at a 1.1V supply, with its power breakdown shown in Fig. 7. Fig. 8 shows the measured output spectrum with a 4kHz -0.8dBFS input. It reveals that the ADC achieves 92.0 dB SNDR, 93.2dB SNR with DWA on, resulting in a 180.1dB FoM_{SNDR}. Fig. 9 shows the measured DR of 93.4 dB, corresponding to a 181.5dB FoM_{DR}. The process and supply robustness of the ADC are shown in Fig. 10. Only 1dB SNR change is observes among the devices, for a ± 0.1V supply voltage variation.

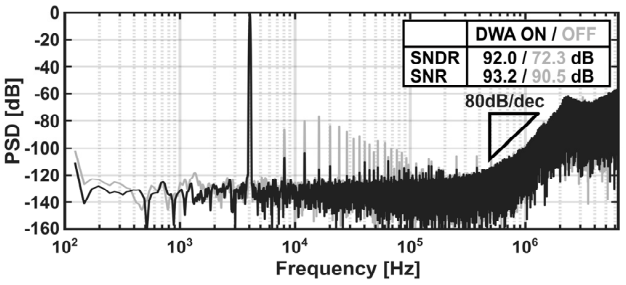


Fig. 8. Measured FFT spectrum (2^{19} points).

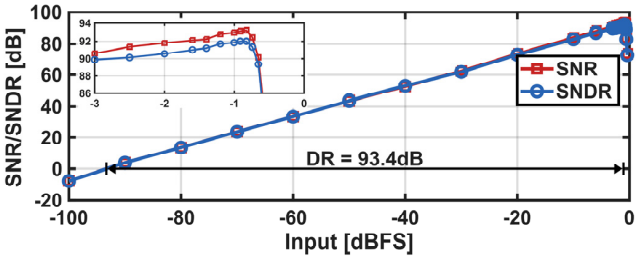


Fig. 9. Measured SNR/SNDR versus input amplitude.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

	This work	Fukazawa VLSI'23	Lozada VLSI'24	Yoon VLSI'25	Liu ISSCC'21	Wang ISSCC'22	Xie CICC'24
Architecture	**PPD DT-DSM NSSAR-QTZ**	DT-DSM NSSAR-QTZ	CT-DSM	CT-Zoom	NSSAR	NSSAR	NSSAR
Process [nm]	**65**	22	28	28	40	65	65
DAC Linearization	**DWA**	DWA		No	Foreground Calibration		
Supply [V]	**1.1**	1.0 / 0.9	1.1	1	1.1	1.2	1.2
OSR	**25**	24	32	40	10	5	8
BW [kHz]	**250**	500/2000	200	250	250	500	500
Power [μW]	**385**	320/1040	380	392	340	74	83
SNDR [dB]	**92.0**	80.4/80.1	89.0	91.2	93.3	84.1	82
DR [dB]	**93.4**	84.1/83.3	92.1	92.7	95	84.9	83.2
FoM_{SNDR} [dB]	**180.1**	172.3/172.9	176.2	179.2	182	182.4	179.8
FoM_{DR} [dB]	**181.5**	176.0/175.9	179.3	180.7	183.7	183.2	181.0

[a] $FoM_{SNDR} = SNDR + 10\times\log_{10}(BW/Power)$ [b] $FoM_{DR} = DR + 10\times\log_{10}(BW/Power)$

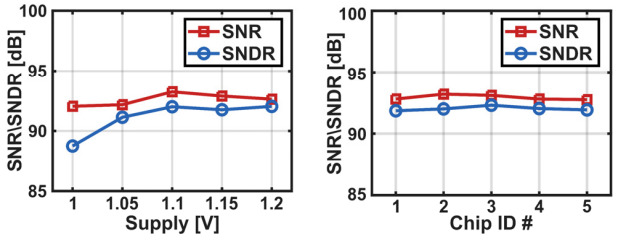
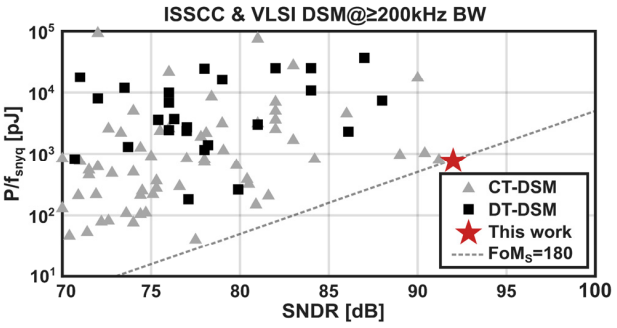


Fig. 10. Measured SNR/SNDR under different chip samples and supply variation.



[a] B.Murmann,"ADC Performance Survey 1997-2026" [Online].

Fig. 11. Performance comparison with the state-of-the-art (BW≥200kHz) DSM ADCs.

Table I summarizes the performance of the designed DSM. Compared with the prior DT-DSM [3], the proposed design achieves a higher SNDR with significantly improved energy efficiency in a 65-nm process, demonstrating the effectiveness of the proposed techniques. Overall, this work achieves the highest FoM_{SNDR} among DT-DSMs with a bandwidth above 200kHz, as shown in Fig. 11.

IV. CONCLUSION

This paper introduces a 250kHz BW 92.0dB SNDR 4th-order DT-DSM that embeds a NSSAR-QTZ in a 2-2 NS cascade. A PPD/FD hybrid structure confines PPD operation to the loop filter's auto-zeroing inverters, leveraging their noise suppression for efficiency without sacrificing differential signaling integrity. A CSGES technique is proposed to stabilize the NSSAR's NTF against open-loop gain variations. Digital complexity including DWA is reduced by tri-level CDAC units. An early-release feedforward operation is used for high parallelism. Combing these techniques, the ADC achieves 180.1dB FoMs.

REFERENCES

[1] J. Liu, D. Li, Y. Zhong, X. Tang and N. Sun, "27.1 A 250kHz-BW 93dB-SNDR 4th-Order Noise-Shaping SAR Using Capacitor Stacking and Dynamic Buffering," *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2021, pp. 369-371.

[2] T. Wang, T. Xie, Z. Liu and S. Li, "An 84dB-SNDR Low-OSR 4th-Order Noise-Shaping SAR with an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 418-42.

[3] M. Fukazawa and T. Matsui, "A 24-OSR to Simplify Anti-Aliasing Filter 2MHz-BW 83dB-DR 3rd-order DT-DSM using FIA-Based Integrator and Noise-Shaping SAR Combined Digital Noise-Coupling Quantizer," *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2023, pp. 1-2.

[4] L. Meng, J. Chen, M. Zhao and Z. Tan, "A Partially Feedback NSSAR Embedded Third-Order Delta–Sigma Modulator With Gain-Boosted Two-Stage FIAs," in IEEE Journal of Solid-State Circuits, vol. 59, no. 9, pp. 2735-2746, Sept. 2024.

[5] Chae, K. Souri and K. A. A. Makinwa, "A 6.3 μW 20 bit Incremental Zoom-ADC with 6 ppm INL and 1 μV Offset," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3019-3027, Dec. 2013.

[6] Z. Lu, H. Ji, W. Qu, L. Ye, M. Zhao and Z. Tan, "A 1 V 1.07 μW 15-Bit Pseudo-Pseudo-Differential Incremental Zoom ADC," in IEEE Journal of Solid-State Circuits, vol. 58, no. 9, pp. 2575-2584, Sept. 2023.

[7] C. Y. Lee and U. -K. Moon, "A 0.0375mm2 203.5μW 108.8dB DR DT Single-Loop DSM Audio ADC Using a Single-Ended Ring-Amplifier-Based Integrator in 180nm CMOS," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 412-414.

[8] Y. Luan *et al*., "18.2 A 12.2μW 99.6dB-SNDR 184.8dB-FOMs DT Zoom PPD ΔΣM with Gain-Embedded Bootstrapped Sampler," *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2025, pp. 308-310.

[9] C. -K. Hsu, T. R. Andeen and N. Sun, "A Pipeline SAR ADC With Second-Order Interstage Gain Error Shaping," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1032-1042, April 2020.

[10] T. Xie *et al*., "An 82dB-SNDR Input-Driving-Relaxed Noise-Shaping SAR with Amplifier-Reused In-Loop Buffering and NTF Leakage Reshaping," *2024 IEEE Custom Integrated Circuits Conference (CICC)*, Denver, CO, USA, 2024, pp. 1-2.

[11] J. Liu, Z. Lu, L. Qi, M. Zhao and Z. Tan, "A 100kHz-BW 95.3dB-DR SMASH CTDSM with RC Variation Robustness achieving +5.8dBFS MSA," *2025 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Daejeon, Korea, Republic of, 2025, pp. 109-111.