A Second-order IIR-DFE for a Bandwidth-Limited TIA in a 0.43-pJ/b 8×25-Gb/s/λ Optical Receiver

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***Abstract*—This paper presents an 8×25-Gb/s/λ monolithic optical receiver in GF 45-nm SOI CMOS that exploits a bandwidth-limited shunt-feedback transimpedance amplifier (SF-TIA) to enhance sensitivity while maintaining low power and compact area. By intentionally reducing the front-end bandwidth, the receiver increases effective transimpedance and suppresses integrated noise at the cost of increased inter-symbol interference (ISI). To efficiently compensate the resulting long ISI tail, a hybrid equalization scheme is employed, consisting of a single-tap discrete-time decision-feedback equalizer (DTDFE) and a novel second-order infinite impulse response DFE (IIR-DFE) matched to the intrinsic second-order dynamics of the SF-TIA. Due to measurement setup limitations, the prototype is experimentally characterized up to 22 Gb/s, achieving a sensitivity of -12.8 dBm at BER of 1e-10 with 0.43 pJ/bit energy efficiency. The proposed architecture demonstrates an efficient trade-off among sensitivity, power, and area for monolithically integrated optical receivers.**

***Index Terms*—Optical receiver, bandwidth-limited TIA, IIR-DFE, decision-feedback equalization, silicon photonics, monolithic integration, low-power high sensitivity receiver.**

I. Introduction

Monolithic optical receivers are attractive for short-reach links because they reduce photodiode interface parasitics, enable compact multi-channel integration, and improve receiver sensitivity by minimizing the capacitance seen at the front-end. These advantages are particularly important in data-center and high-performance computing interconnects, where receiver sensitivity directly impacts the required optical modulation amplitude and overall link energy. The challenge, however, is that monolithic photonic CMOS platforms typically provide weaker electrical performance than aggressively scaled electronic CMOS nodes, making it difficult to achieve high data rate, high sensitivity, low power, and small area simultaneously.

This work targets an 8×25-Gb/s/λ monolithic optical receiver architecture in GF 45-nm SOI CMOS, shown in Fig. 1. Rather than maximizing front-end bandwidth, the proposed receiver intentionally uses a bandwidth-limited shunt-feedback transimpedance amplifier (SF-TIA) to improve sensitivity. Reducing the front-end bandwidth lowers integrated noise and increases effective transimpedance, thereby improving the signal-to-noise ratio (SNR), but it also creates substantial postcursor inter-symbol interference (ISI). The key challenge is therefore not achieving the widest possible front-end, but recovering data efficiently from a deliberately bandwidth-limited one.

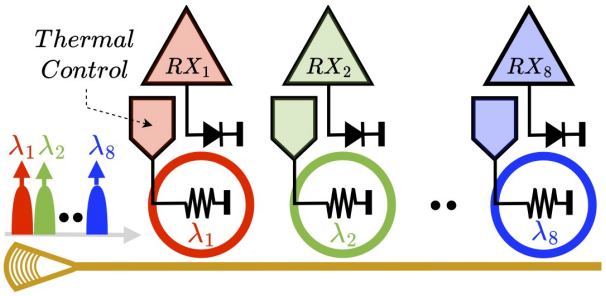

Fig. 1. Conceptual illustration of the 8×25-Gb/s/λ monolithic optical receiver arrayc.

Conventional equalization approaches are not well suited to this operating point. Multi-tap discrete-time DFE can compensate ISI, but at these speeds it increases comparator loading, loop latency, timing pressure, and area [1]. Conventional first-order IIR-DFE is more compact, but it does not accurately match the residual ISI arising from the second-order response of bandwidth-limited SF-TIAs commonly employed in optical receivers, motivating higher-order equalization [2]. To address this, the proposed receiver combines a 1-tap DTDFE with a novel second-order IIR-DFE. The DTDFE removes the dominant first postcursor, while the second-order IIR-DFE suppresses the remaining long ISI tail with much lower complexity than a multi-tap discrete-time equalizer.

The full 8×25-Gb/s/λ receiver array is implemented in GF 45-nm SOI CMOS. Due to available measurement equipment limitations, experimental characterization in this work is limited to a single receiver lane. The measured lane operates up to 22 Gb/s and achieves a sensitivity of -12.8 dBm at BER=10^{-10}, validating the proposed hybrid equalization approach as a practical solution for dense, low-power multi-channel monolithic optical receivers.

II. Receiver Architecture

Fig. 2 shows the architecture of the proposed receiver. A monolithic photodiode drives a bandwidth-limited TIA followed by a Cherry–Hooper post-amplifier. The post-amplified signal is digitized using a half-rate sampler to reduce clocking power. A 1-tap DTDFE is used to cancel the dominant first postcursor with minimal loop latency. The recovered half-rate outputs are then recombined by a clock-less full-rate

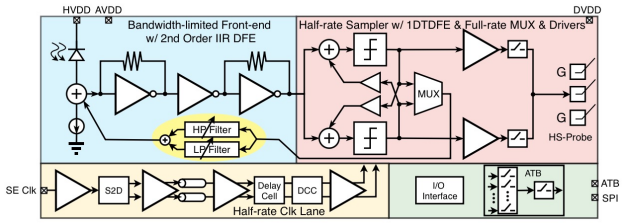

Fig. 2. Proposed receiver architecture with bandwidth-limited SF-TIA, DTDFE, and second-order IIR-DFE.

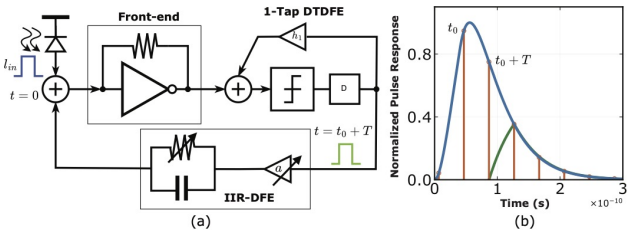

Fig. 3. Hybrid equalization concept: (a) architecture, (b) IIR-DFE matching and ISI suppression.

multiplexer, whose outputs drive a continuous-time second-order IIR-DFE filter.

The bandwidth-limited TIA exhibits a second-order response, producing a long ISI tail that cannot be accurately canceled by a first-order IIR-DFE. The proposed IIR-DFE uses parallel high-pass (HP) and low-pass (LP) paths to generate a feedback waveform matched to the front-end dynamics. The DTDFE cancels the dominant first postcursor, while the second-order IIR-DFE suppresses the remaining ISI components.

Fig. 3 illustrates the proposed hybrid equalization. Fig. 3(b) shows the TIA output pulse response, highlighting the long postcursor ISI tail from the bandwidth-limited front-end. As the sliced data is processed by the IIR-DFE and injected at the input, it is shaped by the same TIA, producing a response matched to the residual ISI tail. This enables effective cancellation of second and higher-order postcursors.

III. Circuit Implementation

The analog front-end and IIR-DFE implementation are shown in Fig. 4. The TIA uses a 16 kΩ feedback resistor and is intentionally designed for a bandwidth of 4.25 GHz, corresponding to approximately 0.17× the target data rate of 25 Gb/s. This operating point was selected to balance the sensitivity benefit of bandwidth reduction against increased ISI. The TIA is followed by a Cherry–Hooper post-amplifier providing additional gain.

The second-order IIR-DFE is realized using two parallel current-injection paths. The HP path provides a derivative-like response, while the LP path contributes a proportional component. Their outputs are summed in the current domain and injected into the TIA input summing node. Current-mode injection preserves the low impedance at the summing junction

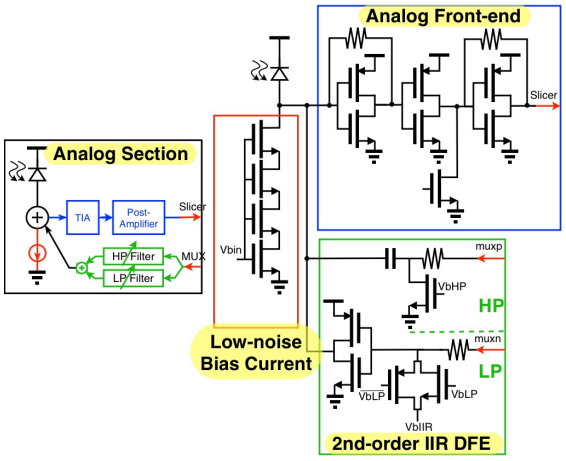

Fig. 4. Analog front-end and IIR-DFE implementation.

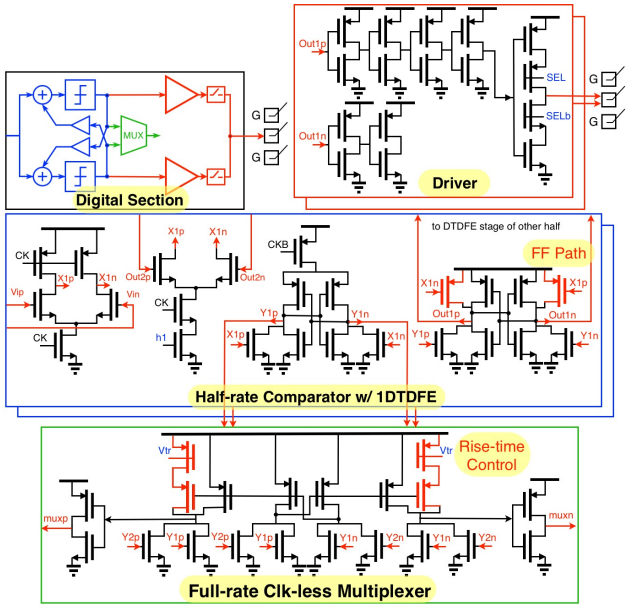

Fig. 5. Digital section with half-rate sampler, DTDFE, and multiplexer.

and minimizes added loop delay. The HP path uses a small coupling capacitor placed close to the injection node, while the LP path uses an inverter-based transconductance stage for symmetric operation and efficient tuning.

Fig. 5 shows the digital back-end. A half-rate double-tail dynamic comparator is employed to reduce the clock frequency. To meet the stringent timing requirements at 25 Gb/s in this technology, feedforward-assisted devices (highlighted in red) are incorporated in the latch to accelerate decision making. A clock-less full-rate multiplexer reconstructs the output data without requiring an additional clock phase. Rise-time control is used to balance the output transitions and improve the waveform driving the analog IIR-DFE.

Special attention was paid to physical implementation be-

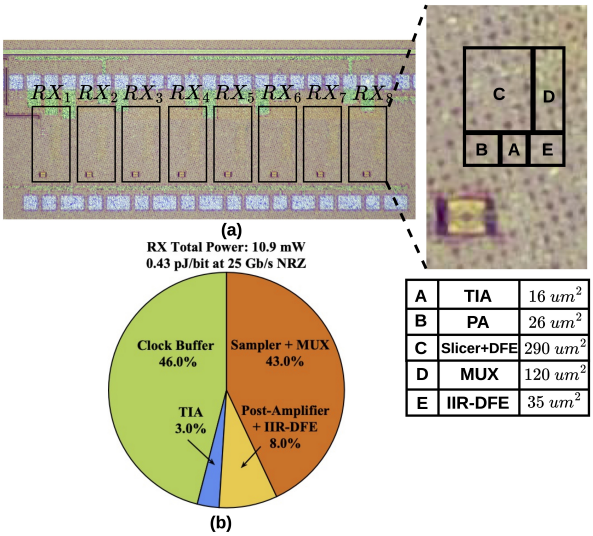

Fig. 6. (a) Chip micrograph. (b) Power breakdown.

cause both the DTDFE and IIR-DFE are loop-delay sensitive. The floorplan minimizes the loop length from TIA to post-amplifier, samplers, multiplexer, and IIR injection network. The HP capacitor and injection node are placed adjacent to the TIA summing node to reduce parasitic dilution and phase lag.

IV. Results and Discussion

The proposed optical receiver is fabricated in GF 45-nm SOI CMOS technology. The chip micrograph is shown in Fig. 6(a). The receiver occupies an active area of 0.005 mm^2, enabling high channel density suitable for multi-channel optical links. The estimated power consumption based on measurement is 10.9 mW, corresponding to 0.43 pJ/bit at 25 Gb/s. The power breakdown is shown in Fig. 6(b).

Fig. 7 illustrates the optical measurement setup. A Keysight M8194A AWG generates a high-speed NRZ signal to drive a Mach–Zehnder modulator (MZM). The optical carrier is provided by an O-band laser. A second laser is used for alignment through on-chip grating coupler loopback.

The optical signal is coupled into the chip through fiber arrays and polarization controllers. The electrical output is probed using high-speed RF probes. A Keysight DCA-X is used to observe both optical and electrical eye diagrams, while a SHF 11104 BERT measures the BER.

The receiver die is wire-bonded to a PCB, and a single-ended half-rate clock is externally supplied. The deserialized output data is captured for BER analysis. Due to signal integrity limitations in the externally delivered clock through PCB and wirebonding, operation is limited to 22 Gb/s while the architecture is designed for 25 Gb/s operation.

Fig. 8(a) shows the optical input eye from the MZM, exhibiting an extinction ratio of 10.77 dB. Fig. 8(b) shows the measured 11-Gb/s deserialized electrical eye corresponding to a 22-Gb/s optical input. The measured electrical eye

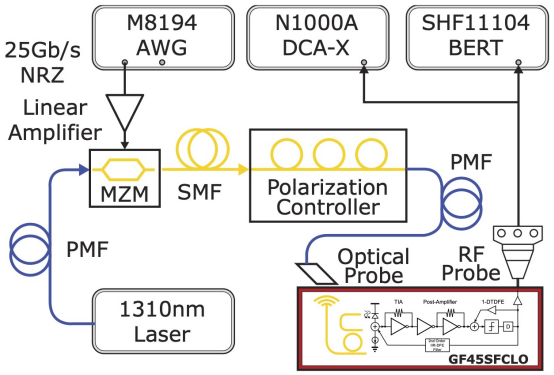

Fig. 7. Optical measurement setup.

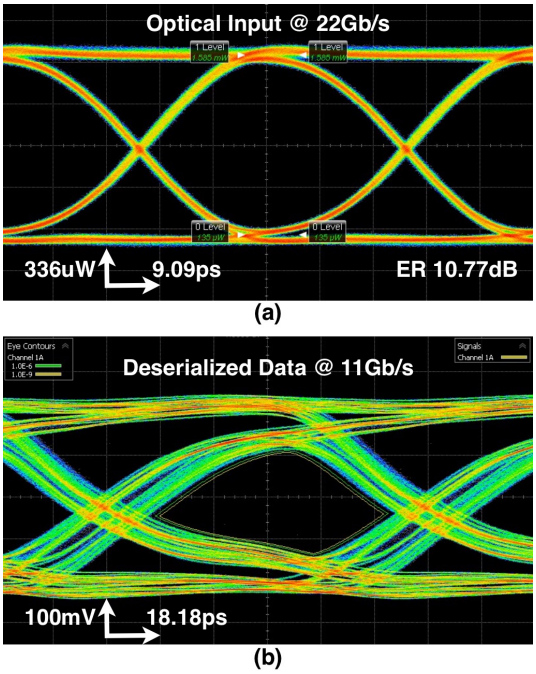

Fig. 8. (a) Optical input eye at 22-Gb/s. (b) Sliced electrical eye at 11 Gb/s.

demonstrates clear opening after equalization, validating the effectiveness of the proposed architecture.

Fig. 9 shows the measured electrical BER bathtub curves at 22 Gb/s. Without equalization, the receiver exhibits a high BER of approximately 8×10^{-1} due to severe ISI introduced by bandwidth limitation. Enabling the 1-tap DTDFE reduces the BER to approximately 2×10^{-2} by canceling the dominant postcursor. When the second-order IIR-DFE is activated in addition to the DTDFE, the BER is significantly improved, demonstrating effective suppression of the long ISI tail. The lower portion of the bathtub curve is obtained by interpolating between the measured data points shown and an additional measurement at a BER of 10^{-13}, not shown in the figure. A timing margin of approximately 0.1 UI at BER=10^{-10} is

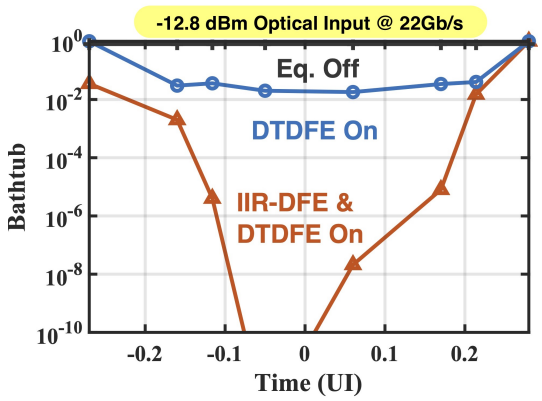

Fig. 9. Measured BER bathtub curves at 22 Gb/s.

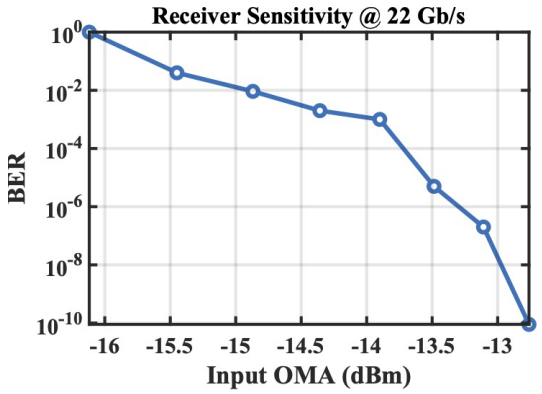

Fig. 10. Measured BER versus input OMA showing receiver sensitivity.

achieved, confirming robust operation.

While the receiver is designed for 25 Gb/s operation with a simulated sensitivity of -19.7 dBm, the measured sensitivity is degraded to -12.8 dBm. This degradation is primarily attributed to supply ringing caused by large digital switching currents coupled through wirebond inductance, which introduces interference at the low-amplitude analog front-end. This effect is not fundamental to the proposed architecture and is expected to be mitigated with improved packaging. Fig. 10 shows the measured BER as a function of input optical modulation amplitude (OMA), from which the receiver sensitivity is extracted.

As summarized in Table I, the proposed receiver achieves competitive energy efficiency, sensitivity, and area at 22 Gb/s. This performance is enabled by the bandwidth-limited architecture, whose associated ISI is effectively mitigated using the proposed second-order IIR-DFE in conjunction with a 1-tap DTDFE.

V. Conclusion

An 8×25-Gb/s/λ monolithic optical receiver employing a bandwidth-limited SF-TIA and a second-order IIR-DFE has been presented in GF 45-nm SOI CMOS. By intentionally reducing the front-end bandwidth, the receiver improves effective transimpedance and suppresses integrated noise, enhancing sensitivity. A hybrid equalization scheme consisting of a 1-tap DTDFE and a second-order IIR-DFE matched to the TIA dynamics efficiently compensates the resulting long ISI tail with low complexity. Due to limitations in external clock delivery through the PCB and wirebonding, the prototype is experimentally characterized up to 22 Gb/s, achieving a sensitivity of -12.8 dBm at BER=10^{-10} with 0.43 pJ/bit energy efficiency. The measured sensitivity is limited by packaging-induced interference, and is expected to improve significantly under optimized integration conditions. The proposed architecture achieves a favorable trade-off among sensitivity, power, and area, and is well suited for high-density monolithic optical interconnects.

TABLE I
Performance comparison with recently published optical RXs.

Metric	ISSCC'26 [6]	ESSERC '25 [5]	VLSI'23 [4]	ISSCC'23 [3]	This work
Process	7 nm	28 nm	28 nm	7 nm	**45 nm**
Data Rate (GBaud)	32	20-56	32	50	**22**
Modulation	NRZ	NRZ	NRZ	NRZ	**NRZ**
Integration	Hybrid	Hybrid	Hybrid	Hybrid	**Monolithic**
Energy Efficiency (pJ/b)	1.26 (TX+RX)	1.9	3.8	0.96	**0.43***
PD Responsivity (A/W)	NA	0.7	0.48	NA	**0.87**
Optical Sensitivity (dBm)	-16	-4.1	-10	-10.1 to -11.4	**-12.8**
RX Area (mm^2)	0.0064**	0.019*	0.5	0.031*	**0.005***

*RX core only: includes analog front-end, slicer, deserializer, and equalizers. For power, clock buffers are also included; **Estimated from figure

VI. Acknowledgement

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