A 1.36 fJ/conv-step 66.7-dB SNDR SAR ADC Using Noise-Critical Moment Auto-Detecting Latch

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***Abstract*—This paper presents an energy-scalable two-stage comparator assisted by a latch that automatically detects noise-critical small input differences and adaptively reconfigures the energy consumption of the pre-amplifier. In high-resolution SAR ADCs, the comparator encounters a wide range of input differences, which necessitates energy scalability to provide the required noise performance efficiently. The proposed comparator combines various merits of the floating-inverter amplifier (FIA) with those of voltage-controlled oscillator (VCO)-based comparators, thereby significantly reducing energy consumption and shortening the comparison time for noise-decent large input differences while preserving low-noise performance for noise-critical small inputs. The proposed comparator is implemented in a 12-bit SAR ADC in a 65-nm CMOS process. The ADC prototype achieves an SNDR of 66.7 dB at 5 MS/s while consuming 14.4 μW. Compared to a conventional FIA-based comparator, the proposed comparator saves energy consumption by 27.5% and achieves a Walden Figure-of-Merit (FoM) of 1.63 fJ/conversion-step, which is the best FoM among previously reported ADCs operating from 1 MS/s to 10 MS/s.**

***Index Terms*—ADC, comparator, energy scalability, floating-inverter amplifier (FIA)**

I. Introduction

Energy-efficient comparators have become a key requirement for high-resolution SAR ADCs because analog circuits increasingly dominate the overall ADC power consumption as the resolution increases, as shown in Fig. 1(a) [1]. SAR ADCs are widely used in sensors and wireline/wireless communication systems owing to their excellent energy efficiency over a broad range of bandwidths and resolutions [1], [2]. In high-resolution designs, both the comparator and the capacitive-DAC (C-DAC) consume substantial energy to satisfy thermal-noise constraints. Although the C-DAC energy can be reduced by energy-efficient switching schemes [3], [4] or by a kT/C noise-cancellation [5], comparator optimization faces a more fundamental limitation because the noise-efficiency factor (NEF) of recent inverter-based pre-amplifiers has already approached its theoretical limit [6]. Consequently, improving comparator efficiency is essential to further enhance the overall energy efficiency of high-resolution SAR ADCs.

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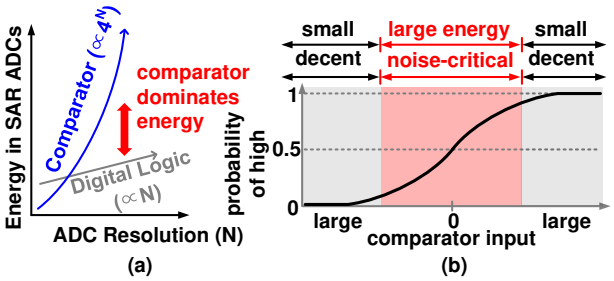

Fig. 1. (a) Trend of SAR ADC power breakdown against its resolution, and (b) probability of comparator outputs against its input difference, and its energy- and noise-critical regions.

FIA-based and VCO-based comparators are two representative approaches for improving comparator efficiency. The FIA-based comparators [7], [8] in Fig. 2(a), which are representative pre-amplifier-based designs, achieve enhanced current efficiency (g_m/I_D) through current reuse, while also features intrinsic common-mode rejection without requiring an additional common-mode feedback (CMFB) circuit. However, they consume nearly constant energy regardless of the input difference, which leads to redundant energy consumption when a larger input-referred noise (IRN) can be tolerated, as described in Fig. 1(b). In contrast, VCO-based comparators [9] in Fig. 2(b) inherently provide input-dependent energy scalability by converting the input voltage difference into a phase difference. However, the comparison time increases exponentially because the energy scalability depends on the number of oscillation cycles, which limits the achievable sampling rate near or below the MS/s range [9].

II. Noise-Critical Moment Auto-Detecting Latch

This paper proposes an energy-scalable FIA-based comparator that combines the high g_m/I_D and fast comparison speed of

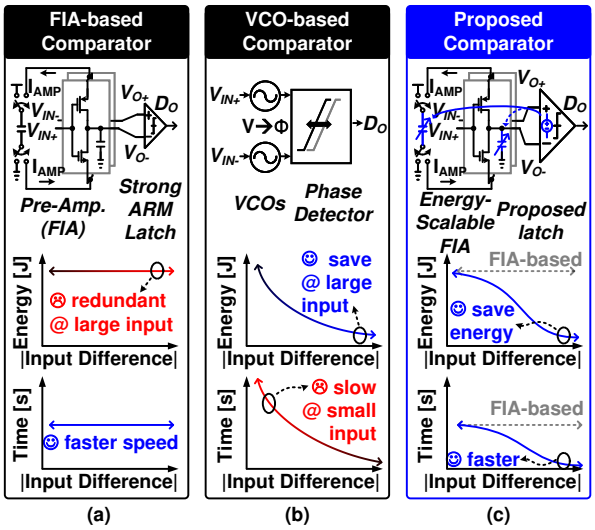

Fig. 2. Comparison of energy and decision time scalability in (a) FIA-based, (b) VCO-based, and (c) proposed energy-scalable FIA-based comparators.

the FIA with the input-dependent energy scalability of a VCO-based comparator, as described in Fig. 2(c), by employing a noise-critical moment auto-detecting (NCM-AD) latch. Fig. 3 describes the timing diagram and circuit implementation of the proposed two-stage comparator. During pre-amplification (phase #1), the NCM-AD latch determines the gate-to-source voltages (V_{GS}) of its input transistors according to the pre-amplified input difference, $V_{O+}-V_{O-} = A_V(V_{IN+}-V_{IN-})$, where A_V denotes the pre-amplifier gain. One input transistor is driven by $A_V(V_{IN+} - V_{IN-})$, while the other is driven by $-A_V(V_{IN+} - V_{IN-})$. When the magnitude of the pre-amplified signal becomes sufficiently large, one of the input transistors attains a sufficiently large positive V_{GS} and automatically triggers the latch (phase #2-1). The second-stage latch then completes quantization before the external trigger signal arrives, thereby quenching the pre-amplifier and preventing redundant energy consumption.

While the NCM-AD latch detects the magnitude of the pre-amplified signal, the FIA operates in two reconfigurable modes, namely a low-power mode and a low-noise mode. During pre-amplification (phase #1), the FIA starts in the low-power mode using a small reservoir capacitor (C_{R1}) and a small load capacitor (C_{O1}), which enable low energy consumption and high gain at high speed. If the input difference is large enough (phase #2-1), the latch self-triggers and terminates the FIA operation early, thereby reducing both energy consumption and comparison time. If the input difference is not large enough to trigger the latch (phase #2-2), the FIA transitions to the low-noise mode by engaging larger reservoir and load capacitances, $(C_{R1} + C_{R2})$ and $(C_{O1} + C_{O2})$, to preserve high SNR under noise-critical input conditions.

The proposed comparator therefore retains the advantages of the FIA while additionally providing the energy scalability of VCO-based designs. As shown in Fig. 4(a) and (b), for

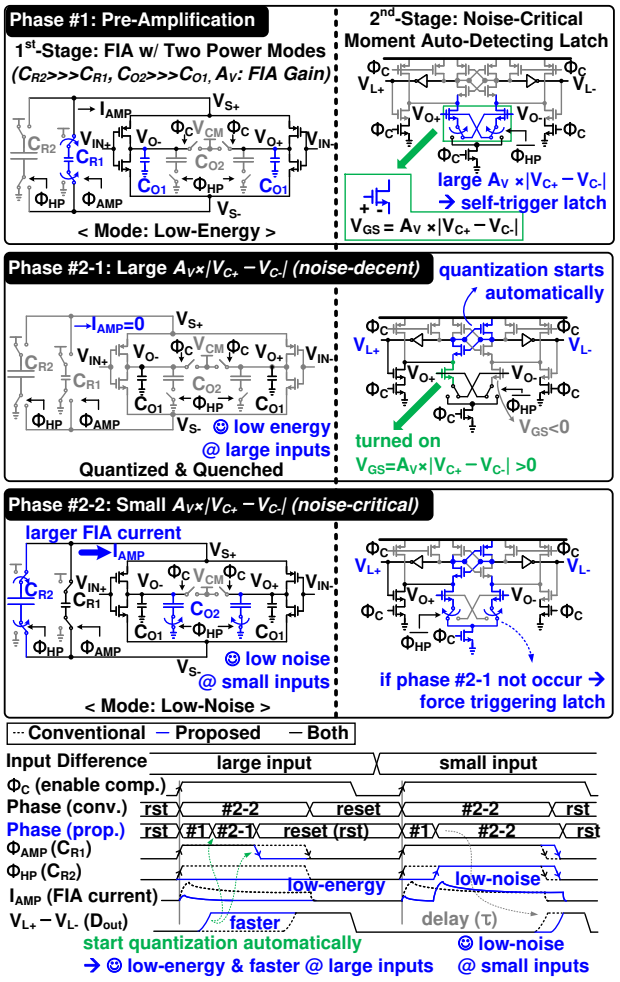

Fig. 3. Schematics and a timing diagram of the proposed energy-scalable comparator during pre-amplification (phase #1), quantization for large inputs (phase #2–1) and small inputs (phase #2–2).

large input differences, the proposed comparator reduces the comparison time and pre-amplifier energy consumption by 93% and 90%, respectively, relative to the smallest input-difference case. These correspond to reductions of 92% and 86%, respectively, compared with a conventional FIA-based comparator. Figure 4(c) and (d) show that the proposed comparator is robust against process, supply-voltage, temperature, and input common-mode variations. Figure 4(e) and (f) illustrate the effect of implementing the proposed comparator in the ADC prototype. The probability that the comparator sees an input difference exceeding 30 mV is 40.0% in a 12-bit SAR ADC with a 1.6 V_{PP} differential input swing and 10^7 random ADC inputs. Simulations of the 12-bit SAR ADC with 1-bit redundancy (a total of 13 SAR cycles) show that the conventional FIA-based and proposed comparators consume 1.42 pJ and 1.03 pJ, respectively, at V_{DD} = 0.8 V, where the proposed comparator saves 27.5% energy compared to the conventional one. Considering the small LSB of the

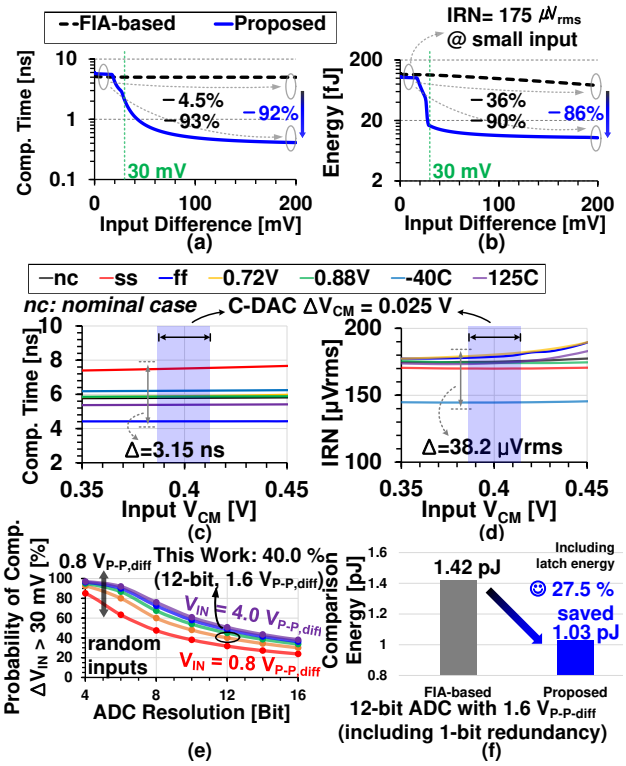

Fig. 4. Simulation results of (a) energy consumption and (b) comparison time of the proposed comparator against the conventional FIA-based one, the proposed one's (c) decision time and (d) IRN against PVT and input common-mode variations, (e) probability of comparator senses input difference more than 30 mV against ADC LSBs, and (f) the comparison of energy consumption of the comparators implemented in a 12-bit SAR ADC prototype.

high-resolution ADC and the 65-nm technology node, which determines the transition point (30 mV) between the comparator's two power modes, even greater energy savings are expected when the proposed comparator is implemented in lower-resolution ADCs using advanced technology nodes.

III. SAR ADC Circuit Implementation

The proposed energy-scalable comparator is implemented in a 12-bit SAR ADC prototype, as shown in Fig. 5. The transitions between the two power modes of the comparator pre-amplifier, as well as the timing for triggering the second-stage latch, are controlled by an asynchronous delay generator. The C-DAC is implemented with grounded-finger metal-oxide-metal (MoM) capacitors and LSB scaling to reduce the number of unit elements [10]. A 1-bit redundancy is included to mitigate decision errors caused by dynamic offset and comparator noise. To ensure a stable common-mode level and energy-efficient switching, a combination of bi-directional single-side [3] and split-capacitor switching [4] is adopted. The timing of each block is synchronously controlled by a timing controller.

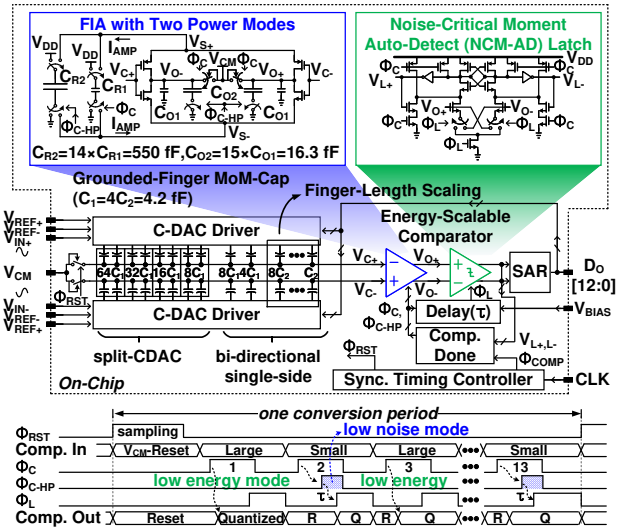

Fig. 5. Block and timing diagram of the 12-bit SAR ADC prototype using the proposed comparator.

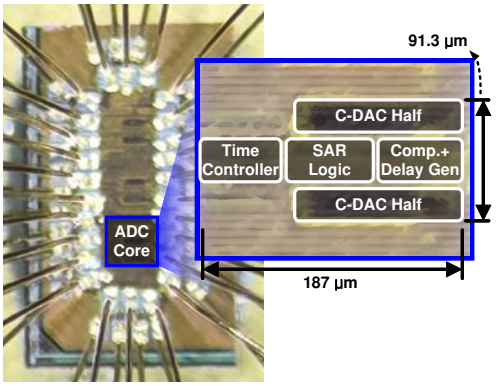

Fig. 6. Chip micrograph.

IV. Measurement Results

The fabricated ADC occupies 0.0171 mm^2 in a 65-nm CMOS process, as shown in Fig. 6. Figure 7 presents the measured dynamic performances of the ADC. At a sampling rate of 5 MS/s with a Nyquist input frequency of approximately 2.49 MHz (Fig. 7(a)), the ADC achieves an SNDR of 66.7 dB and an SFDR of 76.7 dB. At the same sampling rate with a non-Nyquist input frequency of approximately 0.797 MHz (Fig. 7(b)), the measured SNDR and SFDR are 67.4 dB and 79.7 dB, respectively. Figure 7(c) and (d) show the performance variations across different input frequencies, as well as chip-to-chip and supply-voltage variations. Over input frequencies from 0.5 MHz to 2.5 MHz, the SNDR varies by 0.8 dB. Across three chips and under ±10% supply-voltage variation (V_{DD} = 0.72–0.88 V), the ADC maintains robust operation with an SNDR variation of 3.0 dB. The static performances and power breakdown are shown in Fig. 8. The measured INL and DNL are -1.0/+1.1 LSB and -0.40/+0.69

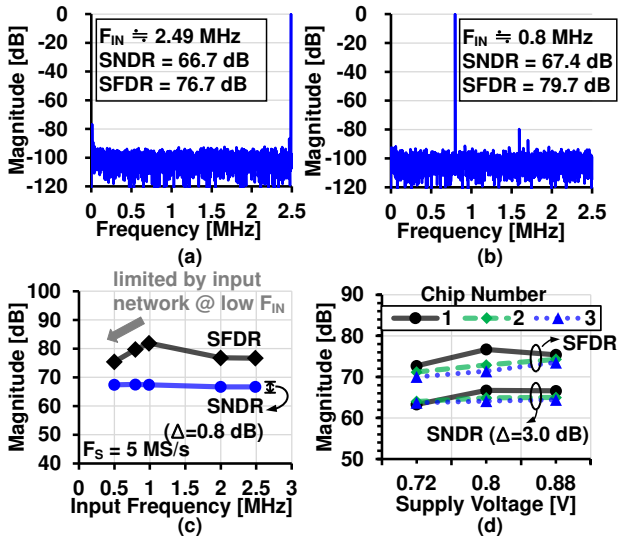

Fig. 7. Measured dynamic performances at (a) Nyquist and (b) non-Nyquist input frequencies at sampling rate of a 5 MS/s, and against (c) different input frequencies and (d) multiple chips and supply voltages.

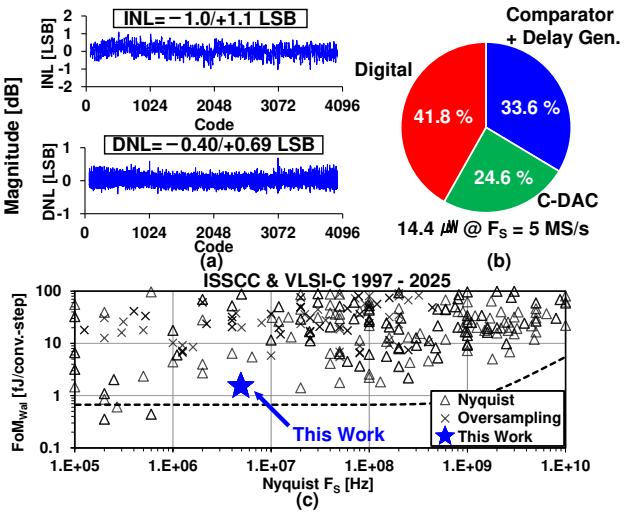

Fig. 8. Measured ADC (a) static performances, (b) power breakdown at sampling rate of 5 MS/s, and (c) its energy efficiency (Walden FoM) against prior arts published in ISSCC and VLSI-C.

LSB, respectively. At 5 MS/s with a 0.8 V supply, the ADC consumes 14.4 μW. The measured power breakdown indicates that the comparator including the delay generator, the C-DAC, and the digital logic (SAR logic, timing controller) account for 33.6%, 24.6%, and 41.8% of the total power, respectively.

Table I compares the prototype with prior SAR ADCs. The proposed ADC achieves a Schreier FoM ($\mathrm{FoM_{Sch}}$) of 179.1 dB and a Walden FoM ($\mathrm{FoM_{Wal}}$) of 1.63 fJ/conversion-step at 5 MS/s, representing the best reported Walden FoM among ADCs operating at comparable sampling rates from 1 MS/s to 10 MS/s, as shown in Fig. 8(c). Unlike the conventional energy-scalable FIA-based comparator in [8], which reconfigures its energy consumption against its number of SAR cycles, the proposed FIA-based one directly senses the input difference and adaptively adjusts its energy consumption accordingly. Furthermore, the merits of the proposed comparator can be further amplified in more advanced technology nodes, at lower resolutions, or with larger ADC input ranges.

TABLE I
ADC PERFORMANCE COMPARISON AGAINST PRIOR SAR ADCS

	This Work	**[8]**	**[10]**	**[9]**
Technology	**65 nm**	65 nm	65 nm	65 nm
Architecture	**SAR**	SAR	SAR	SAR
Resolution	**12b**	16b	13b	13b
Comparator Structure	**Energy-Scalable FIA-based**	Sequentially Charged FIA-based	Dynamic Cap.	VCO-based
Comparator Energy Scalability	**Yes (against input diff.)**	Yes (against SAR cycle)	No	Yes (against input diff.)
Area [mm^2]	**0.0171**	0.275	0.0372	0.027
Supply	**0.8 V**	1.2 V	0.75 V	0.85 V
Input Swing	**1.6 $V_{pp,diff}$**	1.8 $V_{pp,diff}$	1.5 $V_{pp,diff}$	1.4 $V_{pp,diff}$
F_S [MS/s]	**5**	1	2	1.024
SNDR @ Nyq.	**66.7 dB**	80.9 dB	70.6 dB	64.4 dB
SFDR @ Nyq.	**76.7 dB**	100 dB	89.6 dB	85.2 dB
Power	**14.4 μW**	290 μW	15.1 μW	45.2 μW
***$\mathrm{FoM_{Sch}}$**	**179.1 dB**	173.3 dB	178.8 dB	165.0 dB
****$\mathrm{FoM_{Wal}}$**	**1.63 fJ/c.-step**	32.0 fJ/c.-step	2.73 fJ/c.-step	32.5 fJ/c.-step

REFERENCES

[1] X. Tang, J. Liu, Y. Shen, S. Li, L. Shen, A. Sanyal, K. Ragab, and N. Sun, "Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 6, pp. 2249-2262, June 2022.

[2] X. Tang, X. Yang, J. Liu, Z. Wang, W. Shi, D. Pan, and N. Sun, "A 0.4-to-40MS/s 75.7dB-SNDR Fully Dynamic Event-Driven Pipelined ADC with 3-Stage Cascoded Floating Inverter Amplifier," in *IEEE International Solid-State Circuits Conference*, pp. 376-378, 2021.

[3] A. Sanyal and N. Sun, "SAR ADC architecture with 98 % reduction in switching energy over conventional scheme," in *IET Electronics Letters*, vol. 49, no. 4, pp. 248-250, Feb. 2013.

[4] B. Ginsburg and A. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC," in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 739-747, Apr. 2007.

[5] J. Liu, X. Tang, W. Zhao, L. Shen, and N. Sun, "A 13b 0.005mm2 40MS/s SAR ADC with kT/C Noise Cancellation," in *IEEE International Solid-State Circuits Conference*, pp. 258-260, 2020.

[6] D. Hall, K. Makinwa, and T. Jang, "Quantifying Biomedical Amplifier Efficiency: The noise efficiency factor," in *IEEE Solid-State Circuits Magazine*, vol. 15, no. 2, pp. 28-33, June 2023.

[7] X. Tang, L. Shen, B. Kasap, X. Yang, W. Shi, A. Mukherjee, D. Pan, and N. Sun, "An Energy-Efficient Comparator With Dynamic Floating Inverter Amplifier," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1011-1022, Apr. 2020.

[8] C. Yuan, X. Pan, Z. Zheng, Y. Song, R. Martins, Y. Zhu, C. Chan, "A Compact Low-Power 16 b SAR ADC Using Reservoir-Charge-Redistributed DAC and Configurable FIA-Based Comparator," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1011-1022, June 2025.

[9] K. Yoshioka, "A 13b SAR ADC with eye-opening VCO based comparator," in *IEEE European Solid State Circuits Conference*, pp. 411-414, 2014.

[10] S. Lee, H. Kang, M. Lee, "A 2.72fJ/conv 13b 2MS/s SAR ADC Using Dynamic Capacitive Comparator with Wide Input Common Mode," in *IEEE International Solid-State Circuits Conference*, pp. 184-186, 2024.