

A 73.8- μ W Self-Capacitance Touch Readout IC With Logarithmic Iterative Charge Approximation Achieving >1 -nF C_{Self} Sensing for 13.3-inch OCTA

*Jisu Kim¹, *Minkyu Song¹, Byoungseok Yoo¹, Taeho Lee², Soyoung Yang², Jun-Eun Park¹

¹Department of Electrical and Computer Engineering, ²Department of Semiconductor Convergence Engineering Sungkyunkwan University, Suwon, Republic of Korea, *Equally Contributed Author

Abstract—An ultralow-power self-capacitance touch readout IC (SC-TIC) for flexible on-cell touch AMOLED (OCTA) displays is presented. Flexible OCTA displays impose heavy capacitive loads of several hundred picofarads per electrode, posing challenges in achieving simultaneous low-power and high-speed self-capacitance sensing. To address these issues, a logarithmic iterative charge approximation combined with a regulated constant-charge subtraction enables fast per-channel conversion times of 20 μ s and precise self-capacitance sensing up to 1.2 nF, realizing a highly energy-efficient time-multiplexed single-channel SC-TIC architecture. A charge-reuse dynamic power reduction further minimizes power consumption by recovering residual charge across successive channel scans, while a multi-channel binning scan enhances both touch sensitivity and frame rate. The proposed SC-TIC, fabricated in a 180-nm CMOS process, achieves a 44.7-dB SNR and a 480-Hz frame rate while consuming only 73.8 μ W scanning 96 channels of a 13.3-inch flexible OCTA display. With a multi-channel binning configuration, the SC-TIC achieves a frame rate up to 2.88 kHz and a hovering detection SNR of 34 dB at 10-mm distance. The prototype achieves a figure of merit of 11 pJ/step, representing at least a 72 $\times$ improvement over prior state-of-the-art works.

Index Terms—Self-capacitance, touch readout IC, logarithmic iterative charge approximation, charge reuse, flexible OCTA.

I. INTRODUCTION

In flexible on-cell touch AMOLED (OCTA) displays, tight integration of touch sensors with the display increases the coupling capacitance to several hundred picofarads. This heavy capacitive load poses fundamental challenges to self-capacitance sensing: (1) increased dynamic power consumption due to repeated charging and discharging of large sensor nodes and (2) degraded touch sensitivity. These challenges become increasingly severe as panel sizes scale up, making ultralow-power and high-sensitivity self-capacitance sensing a critical design requirement for large-size OCTA displays.

As shown in Fig. 1, conventional self-capacitance sensing architectures based on charge amplifiers (CA) [1]–[3], [9] or current conveyors (CC) [5]–[8], [10] rely on dedicated analog-to-digital converters (ADCs) to digitize the sensed capacitance, resulting in substantial power overhead. Moreover, their restricted input capacitance range below 1 nF precludes reliable operation on large-size flexible OCTA panels [6], [8]. As a result, the fundamental tradeoff between power consumption,

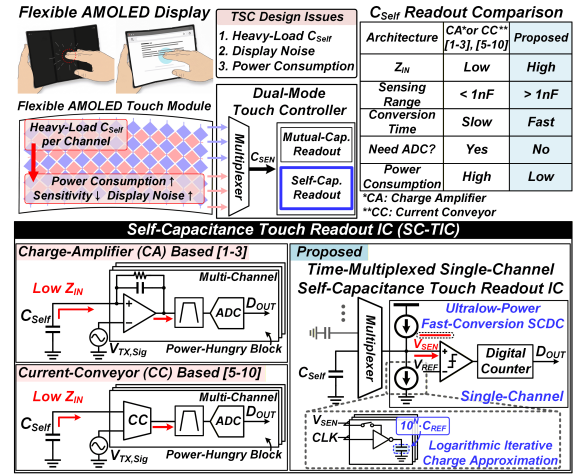


Fig. 1. Design issues of OCTA touch readout IC and comparison of self-capacitance readout architectures.

sensing range, and conversion speed under heavy capacitive loads remains unresolved.

This work presents a time-multiplexed self-capacitance touch readout IC (SC-TIC) that directly addresses these limitations. A logarithmic iterative charge approximation (LICA) combined with a regulated constant-charge subtraction (RCCS) enables fast per-channel conversion times and precise C_{Self} sensing up to 1.2 nF. A charge-reuse dynamic power reduction (CR-DPR) scheme further minimizes power consumption by recovering residual charge from inactive channels across successive scans. A multi-channel binning scan (MCBS) additionally enhances touch sensitivity and frame rate by leveraging the wide input capacitance range, enabling hovering detection and ultralow-power tap-to-wake operation.

II. PROPOSED ARCHITECTURE

Fig. 2 shows the overall architecture of the proposed SC-TIC. A single-channel, single-ended self-capacitance-to-digital converter (SCDC) scans all channels of a large, heavy-load touchscreen panel (TSP) using a time-multiplexed architecture, achieving fast per-channel conversion times down to 20 μ s even with channel capacitances above 1 nF. The single-ended sensing approach avoids RX-wise noise integration

Corresponding author: Jun-Eun Park (e-mail: juneun.park@skku.edu)

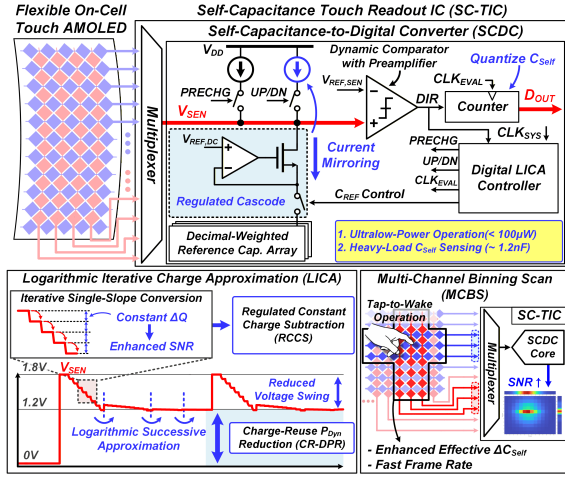


Fig. 2. Overall architecture of proposed SC-TIC with SCDC.

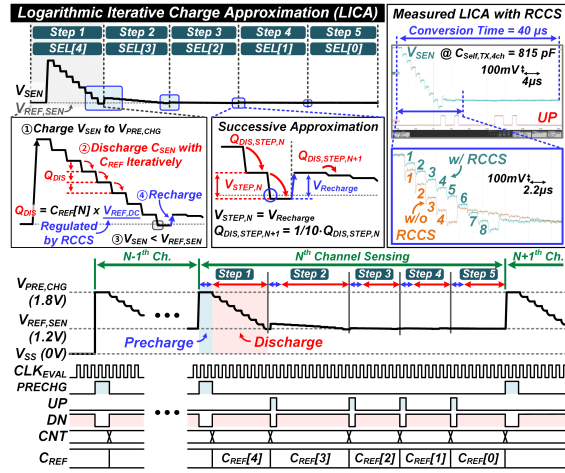


Fig. 3. Operation sequence of LICA with measured waveform during single conversion cycle.

required in differential sensing schemes [9]. Ultralow-power and fast self-capacitance sensing are enabled by a LICA that combines decimal-weighted successive approximation with iterative single-slope conversion, while accurate sensing is ensured by an RCCS that removes dependence on sensor node voltage. A CR-DPR scheme further reduces dynamic power by reusing residual charge in inactive channels. Leveraging its wide input capacitance range, the proposed SC-TIC also supports highly sensitive tap-to-wake and hovering detection through an MCBs.

Fig. 3 illustrates the operation sequence and timing diagrams of the LICA with the RCCS. The activated channel node V_{SEN} is first charged to a preset voltage $V_{PRE,CHG}$, after which the decimal-weighted $C_{REF}[N]$ iteratively discharges the self-capacitance until V_{SEN} crosses $V_{REF,SEN}$. During each iteration, the RCCS regulates the discharging voltage to $V_{REF,DC}$, ensuring a constant charge transfer of $Q_{DIS} = C_{REF}[N] \times V_{REF,DC}$ independent of V_{SEN} . To simplify

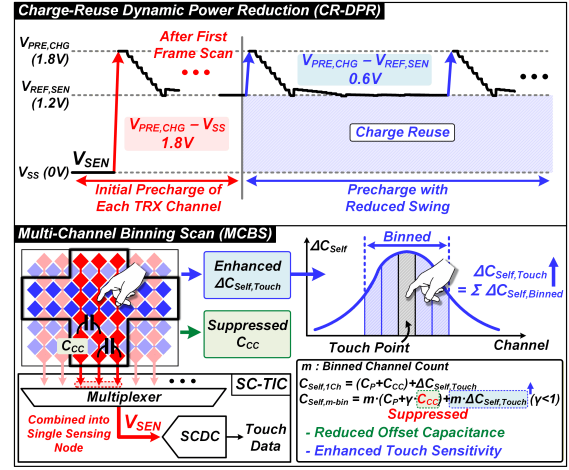


Fig. 4. Operational principles of CR-DPR for power reduction and MCBs for enhanced touch sensitivity.

digital mapping, $V_{REF,DC}$ is set to $V_{PRE,CHG} - V_{REF,SEN}$, allowing the iteration count at each decimal digit to directly represent the sensed capacitance. Owing to the logarithmic discharge process, the charge approximation at each digit is completed within fewer than ten cycles. Furthermore, the LICA and RCCS operate primarily with dynamic power, enabling highly energy-efficient sensing compared with conventional CA- or CC-based approaches.

Fig. 4 illustrates the CR-DPR principle. In the first conversion, each channel is fully charged to $V_{PRE,CHG}$ and then settles at $V_{REF,SEN}$. In subsequent conversions, only the reduced voltage swing of $V_{PRE,CHG} - V_{REF,SEN}$ is charged, reducing precharge dynamic power by up to one-third. The MCBs exploits the wide input capacitance range of the SCDC by combining multiple channels into a single sensing node, enhancing effective self-capacitance variation while suppressing inter-channel capacitive coupling [4]. This enables hovering detection and ultralow-power tap-to-wake operation with frame rate up to 2.88kHz under six-channel binning configuration.

III. CIRCUIT IMPLEMENTATION

Fig. 5 shows the detailed circuit implementation of the SCDC. The self-capacitance of the multiplexed TX or RX channel is processed by a current-mirror-based bidirectional charge subtractor (CM-BCS). With assistance from the RCCS, the discharging and recharging quantities Q_{DIS} and Q_{RE} are determined solely by the decimal-weighted reference capacitor array $C_{REF}[4:0]$ and $V_{REF,DC}$, enabling precise successive charge approximation. The floating-inverter-based preamplifier and offset-calibrated dynamic comparator detect the voltage crossing between V_{SEN} and $V_{REF,SEN}$ without static power consumption. A key advantage of the proposed SCDC is that C_{Self} is converted directly to a digital output using only a simple up/down counter, without requiring a separate ADC. In conventional CA- or CC-based architectures, the analog output voltage proportional to C_{Self} must be digitized by a

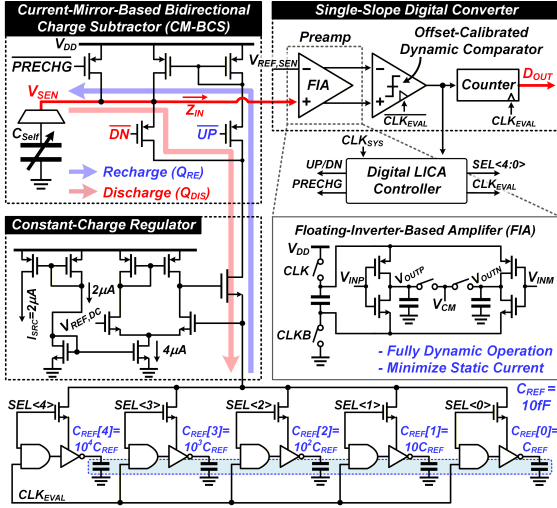


Fig. 5. Circuit implementation of proposed SCDC.

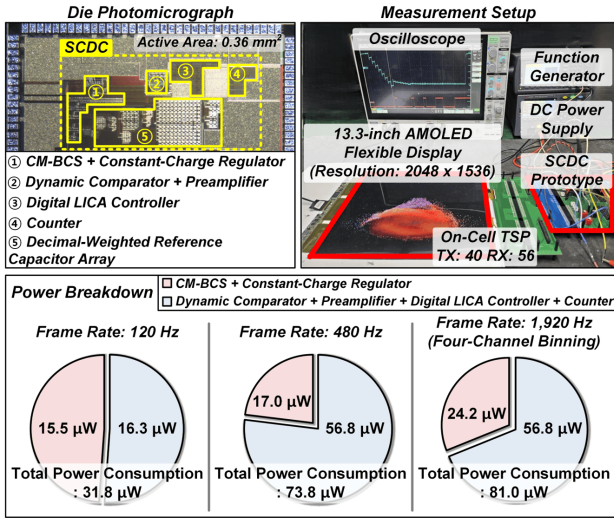


Fig. 6. Die photomicrograph of prototype, measurement setup, and measured power breakdowns.

dedicated ADC, which introduces substantial additional power overhead and circuit complexity. In contrast, the LICA encodes the sensed capacitance directly into the iteration count at each decimal digit, which is accumulated by the counter to produce the final digital output D_{OUT} . Since the power consumption of the counter is negligible compared to an ADC, this ADC-less architecture is a primary contributor to the ultralow-power operation, representing a fundamental power efficiency advantage over prior C_{Self} sensing approaches.

IV. MEASUREMENT RESULTS

The proposed SC-TIC prototype was fabricated in a 180-nm CMOS process and evaluated on a 13.3-inch flexible OCTA display comprising 40 TX and 56 RX channels. Fig. 6 presents the die photomicrograph and measurement setup. The measured power breakdown verifies the ultralow-power

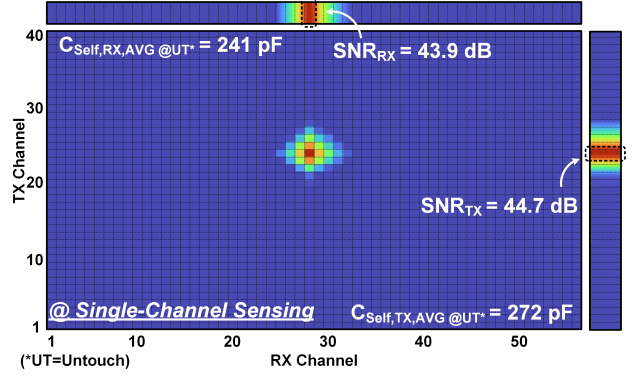


Fig. 7. Measured 2D heatmap of full-panel self-capacitance sensing obtained with single-channel sensing mode.

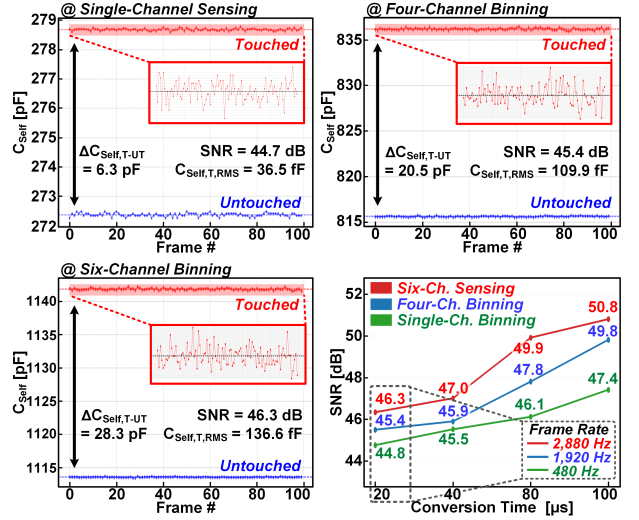


Fig. 8. Measured self-capacitance profiles over 100 frames and SNRs versus conversion time for single-channel, four-channel binning, and six-channel binning scan modes.

operation of the proposed SC-TIC. When scanning all 96 channels of the 13.3-inch flexible OCTA display, the SC-TIC consumes only 31.8 μ W at a frame rate of 120Hz and 73.8 μ W at 480Hz. As the frame rate increases, the dynamic power consumption rises due to the higher switching activity required for faster operation. However, the proposed CR-DPR effectively minimizes this increase by recovering residual charge across successive channel scans. As a result, even under the four-channel binning configuration, which demands C_{Self} sensing of 836pF per sensing node, the SC-TIC maintains efficient operation at only 81 μ W at a frame rate of 1.92kHz. Fig. 7 shows reconstructed self-capacitance map obtained with single-channel scan under finger touch, confirming full-panel sensing. Fig. 8 presents the measured self-capacitance profiles over 100 frames. The prototype achieves an SNR of 44.7dB at a 480-Hz frame rate. The four-channel and six-channel binning schemes demonstrate fast frame rates up to 2.88kHz and heavy-load sensing capability up to 1.2nF, respectively. Fig. 9

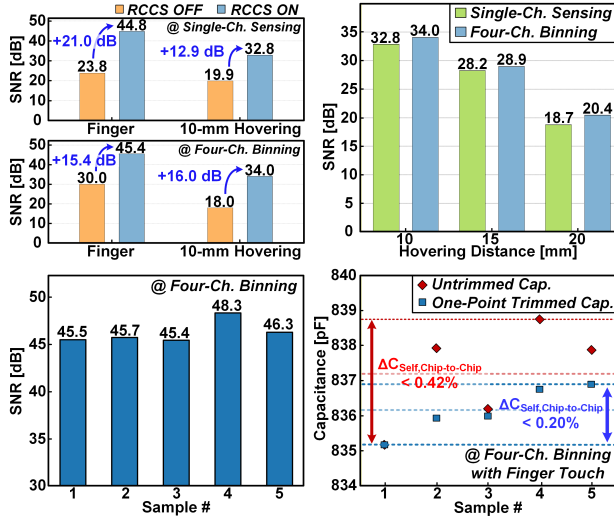


Fig. 9. Measured SNR as a function of RCCS operation and hovering distance. Measured SNR and touched capacitance precision across five prototype samples.

shows measured SNRs as functions of RCCS operation and hovering distance, demonstrating effective SNR enhancement and an extended hovering detection range of up to 20mm. Measured SNR and precision across five prototypes confirm robust and consistent performance. Table I summarizes performance comparisons, where the prototype achieves the lowest power consumption of $73.8\mu\text{W}$ and the best figure of merit (FoM) of $11\text{pJ}/\text{step}$, representing at least a $72\times$ improvement over prior state-of-the-art works.

V. CONCLUSIONS

This paper presents an ultralow-power self-capacitance touch readout IC for 13.3-inch flexible OCTA displays. The proposed LICA combined with an RCCS achieves fast per-channel conversion times of $20\mu\text{s}$ and precise C_{Self} sensing up to 1.2nF through direct capacitance-to-digital conversion, eliminating the need for a dedicated ADC. The CR-DPR and MCBS further minimize power consumption and enhance touch sensitivity, achieving a 480-Hz frame rate at $73.8\mu\text{W}$ and a figure of merit of $11\text{pJ}/\text{step}$, representing at least a $72\times$ improvement over prior state-of-the-art works.

ACKNOWLEDGMENT

This work was supported in part by the KEIT grant funded by the Korea government (MOTIE) (RS-2022-00144290), in part by the KIAT grant funded by the Korea Government (MOTIE) (RS-2025-02214408, HRD Program for Industrial Innovation), and in part by the NRF grant funded by the Korea government (MSIT) (RS-2025-16070403 and RS-2026-25491180) and in part by the BK21 Four Program in 2026.

REFERENCES

- [1] Y. Huh et al., "A 10.1 56-channel, $183\mu\text{W}/\text{electrode}$, $0.73\text{mm}^2/\text{sensor}$ high SNR 3D hover sensor based on enhanced signal refining and fine error calibrating techniques," 2017 Symposium on VLSI Circuits, Kyoto, Japan, 2017, pp. C308-C309.

TABLE I. Performance Summary and Comparison

		This Work		VLSI 2025 [10]	ISSCC 2024 [9]	ISSCC 2024 [8]	ISSCC 2023 [7]	ISSCC 2020 [11]
Type		LICA + RCCS		CC + CVS	CC	DCC + CRA	CC + NARS	Shunt Sense
Process [nm]		180		65	65	130, 350	45	80
Display Module		13.3-inch Flexible AMOLED		-	-	-	-	5.7-inch LCD
TSP (TX, RX)		On-Cell TX: 40 RX: 56		RC Model TX: 16 RX: 16	RC Model TX: 16 RX: 16	N/A TX: 12 RX: 25	RC Model N/A	In-Cell TX: 32 RX: 18
Input Range [pF]		~ 1,200		~ 820	~ 390	~ 620	~ 100	~ 200
Conversion Time/Ch. [μs]		20		520	520	950	N/A	N/A
Hovering?		O		X	X	X	X	X
Frame Rate [Hz]		480	1,920*	240	240	1,050	120	120
SNR [dB]	Finger	44.7 @ 278pF	45.4* @ 836pF	36.6 @ 390pF	20.9 @ 390pF	30.6 @ 530pF	45.8 @ 100pF	51
	10-mm Hovering	32.8 @ 278pF	34.0* @ 836pF	-	-	-	-	-
Power [μW]		73.8	81.0*	8,240	8,480	22,400	166,000	16,000
FoM [pJ/Step]		11	2*	38,852	243,763	20,831	240,202	798

*Four-channel binning scan mode (MCBS).

*Power Consumption

*FoM [pJ/Step] = $\frac{2^{(\text{SNR}-1.76)/6.02} \times \# \text{ of Channels} \times \text{Frame Rate}}{\text{Power Consumption}}$

*Based on a 216-channel configuration.

- [2] J. Choi et al., "A 1.08ms Ultrafast Scanning Capacitive Touch-Screen Sensor Interface with Charge-Interpolated Common-Mode Compensation and Host-Based Adaptive Median Filtering," 2023 IEEE Asian Solid-State Circuits Conference (A-SSCC), Haikou, China, 2023, pp. 1-3.
- [3] S. H. Ko and B. D. Yang, "An Ultra-Compact Low Power Self-Capacitive Touch Screen Readout IC Embedding Reconfigurable Noise Immunity and Current-Driven Capacitance Compensation," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 8, pp. 1321-1325, Aug. 2019.
- [4] L. Du et al., "A 2.3mW 11cm-range bootstrapped and correlated-double-sampling (BCDS) 3D touch sensor for mobile devices," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, USA, 2015, pp. 1-3.
- [5] J. Choi, I. Jeong, S. -W. Jung and J. -E. Park, "A 92.8% Power Reduction Event-Driven Dual-Mode Touch Analog Front-End IC Featuring $620\mu\text{W}$ Self-Capacitance Sensing and 500fps Mutual-Capacitance Sensing," 2024 IEEE Symposium on VLSI Technology and Circuits, Honolulu, HI, USA, 2024, pp. 1-2.
- [6] S. Moon, J. Choi and J. -E. Park, "A 10.5mW Automotive Touch AFE IC Featuring Radiated EMI Reduction Based on Pipelined Dual-Frequency Modulation and Sine2 Waveform Shaping for CISPR 25 Class 5 Compliance," 2025 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2025, pp. 132-134.
- [7] S. Byun et al., "A 45.8dB-SNR 120fps 100pF-Load Self-Capacitance Touch-Screen Controller with Enhanced In-Band Common Noise Immunity Using Noise Antenna Reference," 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2023, pp. 386-388.
- [8] J. Lee et al., "A 620pF-Compensated Dual-Mode Capacitance Readout IC for Sub-Display TSP with VRR Scan," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 438-440.
- [9] J. Y. An et al., "Noise Immunity in Capacitive Sensing: Single-Ended AFE Design with Common-Current Subtraction for Mutual- and Self-Capacitance Sensing in 390pF Load," 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2024, pp. 436-438.
- [10] S. H. Choi et al., "A Hybrid Touch Sensing AFE with Common-CVQ (Currents, Voltages, and Charges) Subtraction to Improve Display Noise Immunity for Large Sensing Load up to 820pF," 2025 Symposium on VLSI Technology and Circuits, Kyoto, Japan, 2025, pp. 1-3.
- [11] H. Jang et al., "A 51dB-SNR 120Hz-Scan-Rate 32×18 Segmented-VCOM LCD In-Cell Touch-Display-Driver IC with 96-Channel Compact Shunt-Sensing Self-Capacitance Analog Front-End," 2020 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2020, pp. 432-434.