A 0.367 pJ/b 18-Gb/s PAM-3 Transmitter Using a Middle-Level-Activated Reverse CMOS Output Driver for Short-Reach Links

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***Abstract*—This paper presents a 0.367 pJ/b, 18-Gbps PAM-3 single-ended transmitter for short-reach interfaces employing a middle-level-activated reverse CMOS output driver (RCOD). Unlike P-over-N output driver for PAM-3 transmitters, the proposed design reduces power consumption using half of the gate-source voltage, achieving a 20.2 % energy efficiency improvement, while maintaining eye margins of 19 mV and 11 ps under 100mV, 60 Hz supply noise by decoupling the source voltage from V_{DD}. The proposed design occupies 0.00843 mm^2 in a 14-nm FinFET technology.**

Keywords—PAM-3, transmitter, output driver, short-reach interface

I. Introduction

Chiplet-based architectures and high-bandwidth memory (HBM) employ a massive number of parallel short-reach links to achieve high I/O density and aggregate bandwidth. To further improve I/O density and reduce power consumption, terminationless single-ended signaling is adopted in short-reach interfaces, particularly in HBM I/O systems [1-2]. Furthermore, multi-level modulation schemes such as pulse amplitude modulation (PAM)-3 are employed to increase the per-lane data rate [3-5].

Compared to non-return-to-zero (NRZ) signaling, PAM-3 exhibits a lower Nyquist frequency, improving tolerance to channel attenuation. However, PAM-3 requires accurate generation of the intermediate voltage level. In conventional P-over-N output drivers, generating the middle level inevitably turns on both pull-up and pull-down transistors, leading to excessive static current and degraded energy efficiency [6-7]. To improve energy efficiency, prior works have investigated N-over-N output drivers for PAM-3 transmitters [8-11]. However, these approaches require an additional supply voltage (V_{DDQ}) for the output driver and suffer from a reduced output voltage swing. In addition, single-ended transmitters are susceptible to supply noise, making it challenging to achieve robust signal integrity.

To address these limitations, this paper proposes a PAM-3 transmitter in which the RCOD is activated during middle-level transmission. Compared to conventional P-over-N output drivers [1-7], the proposed output driver achieves a 47.7% reduction in total current. In addition, it does not require a dedicated V_{DDQ} supply and does not impose any limitation on the voltage swing. Furthermore, the power-decoupled nature of the RCOD, in which the transistor source node is isolated from the supply rails, enhances robustness to supply noise and improves the SNR.

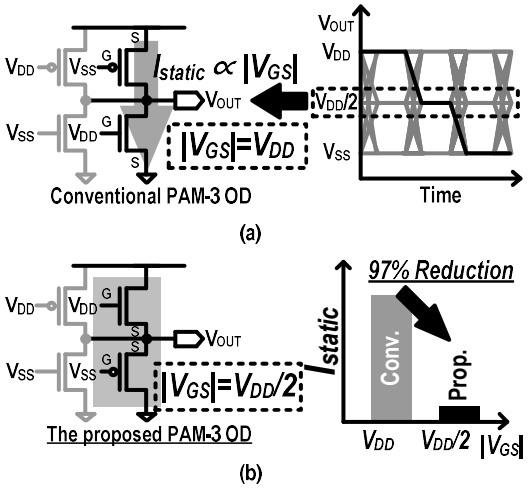


Fig. 1. (a) Middle level operation of conventional PAM-3 OD, (b) same operation of the proposed PAM-3 OD with static current comparison.

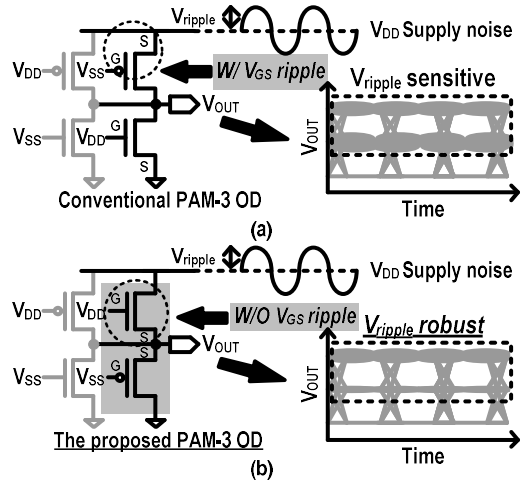


Fig. 2. (a) The conventional PAM-3 output driver with supply noise, (b) the proposed PAM-3 output driver with supply noise.

II. The Proposed Transmitter With RCOD

A. Static current comparison and supply noise robustness

Fig. 1 illustrates the middle-level operation of (a) a conventional PAM-3 output driver and (b) the proposed PAM-3 output driver. The figure also compares the resulting

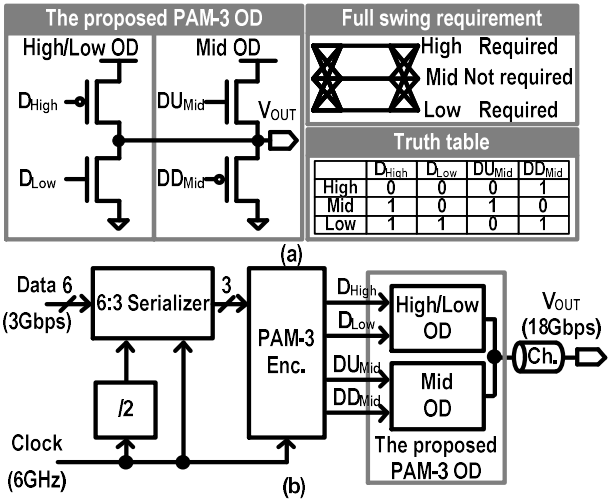


Fig. 3. (a) The proposed PAM-3 output driver, the full-swing requirements, and truth table, (b) top structure of the proposed transmitter.

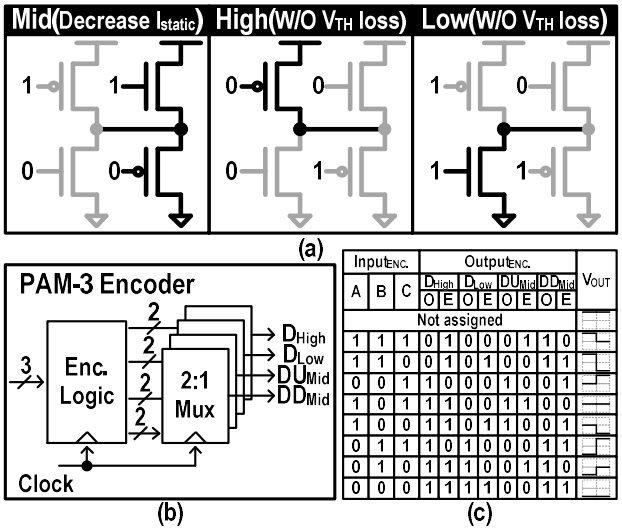


Fig. 4. (a) Operation of the proposed PAM-3 output driver for each signal level, (b) block diagram of the PAM-3 encoder, (c) truth table of encoder logic.

static current in each case. In a conventional PAM-3 output driver, the middle level (typically $V_{DD}/2$) is generated using a PMOS for pull-up and an NMOS for pull-down, which results in a gate-to-source voltage of V_{DD} and induces static current. This static current is the primary cause of power consumption during middle-level generation in a conventional PAM-3 output driver.

In contrast, the proposed PAM-3 output driver swaps the PMOS and NMOS devices in the pull-up and pull-down paths during middle-level generation, reducing the V_{GS} to $V_{DD}/2$. Consequently, a 97% reduction in static current is achieved compared to the conventional output driver, as explained in Fig. 5, indicating that the proposed structure can improve the energy efficiency of PAM-3 transmitter.

Fig. 2(a) and (b) present the eye diagrams of the conventional and proposed PAM-3 output under V_{DD} supply noise. In the conventional PAM-3 output driver, ripple on V_{DD} couples to both the high level and the middle level, reducing the upper and lower eye margins of the PAM-3

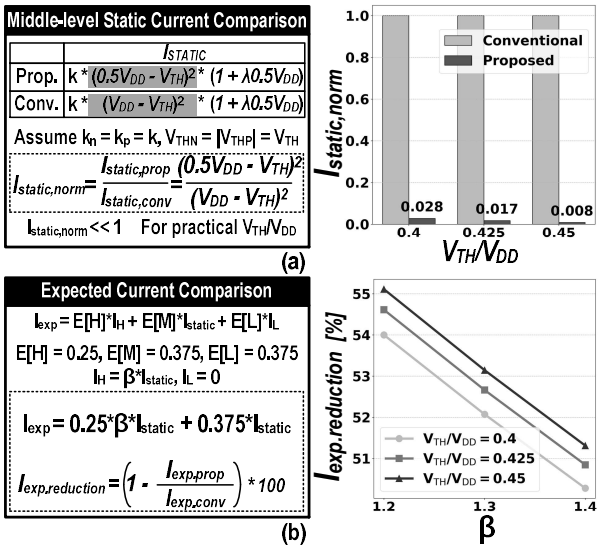


Fig. 5. (a) Middle-level static current comparison of the proposed output driver and conventional output driver with normalized static current versus V_{TH}/V_{DD}, (b) expected current reduction ratio versus I_H/I_{static}.

output eye diagram. In contrast, in the proposed PAM-3 output driver, the source of the pull-up MOSFET is isolated from the power rail during middle-level generation, making the middle level less sensitive to V_{DD} ripple. Consequently, the proposed driver achieves a wider eye margin than the conventional output driver, improving the SNR performance of PAM-3 signaling.

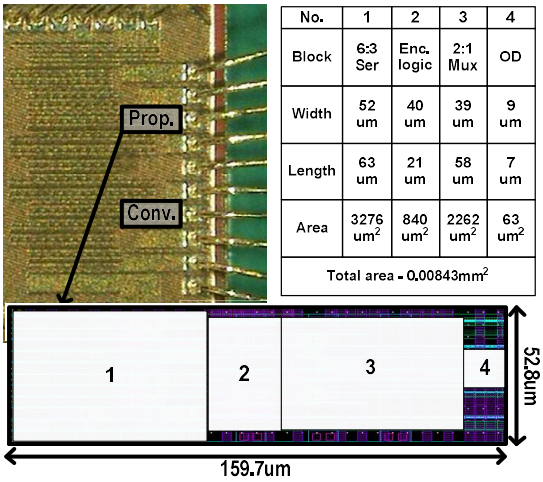
B. Proposed PAM-3 transmitter and output driver

Fig. 3(a) shows the schematic of the proposed PAM-3 output driver and its corresponding truth table, including the full-swing requirements. The proposed driver employs a conventional CMOS driver for the high and low levels to ensure full-swing operation without threshold-voltage loss, while the RCOD is used for the middle level, which does not require full-swing operation. As shown in Fig. 3(b), the transmitter utilizes a 6:3 serializer and a PAM-3 encoder to implement a 3-bit/2-UI signaling scheme [9], [11]. A 6-GHz clock and six 3-Gbps parallel data inputs are used, resulting in an output data rate of 18-Gbps.

Fig. 4(a) shows the operation of the proposed output driver for the three PAM-3 levels. In the proposed output driver, the right branch operates during the middle-level signaling, where the NMOS in the pull-up path and the PMOS in the pull-down path are turned on. During the high and low level operations, the PMOS and NMOS in the left branch are turned on to generate the corresponding output levels. As a results, the proposed structure reduces current consumption at the middle level compared to conventional P-over-N architectures, while achieving full-swing high and low levels, unlike N-over-N structures that suffer from threshold-voltage loss. Fig. 4 (b) and (c) show the encoder block diagram and truth table, implementing 3-bit/2-UI operation via multiplexing [11].

C. Analysis of current consumption

To quantify the static current reduction mentioned in Section II-A, the static current of the proposed and conventional output drivers is analyzed in this subsection.



No.	1	2	3	4
Block	6:3 Ser	Enc. logic	2:1 Mux	OD
Width	52 um	40 um	39 um	9 um
Length	63 um	21 um	58 um	7 um
Area	3276 um^2	840 um^2	2262 um^2	63 um^2
Total area - 0.00843mm^2				

Fig. 6. Die micrograph with area breakdown.

Fig. 5(a) shows a comparison of the middle-level static current between the conventional and the proposed architectures. During the generation of the middle-level signal, both the proposed output driver and the conventional P-over-N output driver consume current according to the MOSFET saturation current equation. In the proposed driver, however, the V_{GS} is reduced to half of V_{DD} rather than V_{DD}. To compare the current consumption, k_n and k_p are assumed to be equal($k_n = k_p = k$), and the threshold voltages of the NMOS and PMOS devices are assumed to be identical. By normalizing the current with respect to that of the conventional output driver, the following expression is obtained.

$$I_{static.norm} = (0.5V_{DD} - V_{TH})^2 / (V_{DD} - V_{TH})^2 \quad (1)$$

The normalized static current obtained from (1) is shown in Fig. 5 (a). In the employed CMOS process, the ratio of V_{TH} to V_{DD} ranges from 0.4 to 0.45. Under this condition, the proposed output driver reduces the static current by 97% compared to the conventional P-over-N output driver.

However, a PAM-3 signal consists of three levels, rather than only the middle level, Since the occurrence probabilities of levels are determined by the encoder truth table, the overall current consumption cannot be evaluated solely based on the middle-level current. Therefore, the expected current must be estimated by considering the transition probabilities of each signal level as shown in Fig. 5(b). The expected current (I_{exp}) can be expressed as follows.

$$I_{exp} = E[H]*I_H + E[M]*I_{static} + E[L]*I_L \quad (2)$$

E[H], E[M], and E[L] denote the expected probabilities of the high, middle, and low level outputs of the PAM-3 signal, respectively. Based on the encoder truth table in Fig. 4(c), the probability of the high level is 4 out of 16 cases (0.25), while the probabilities of the middle and low levels are each 6 out of 16 cases (0.375). I_H, I_{static}, and I_L represent the current consumption at high, middle, and low level outputs, respectively. To quantify the expected current high-level current I_H is $\beta*I_{static}$, where β is the current ratio reported in prior works [7], [11], while the low-level current I_L is assumed to be negligible based on ratio reported in prior works. Substituting these values into (2), the expected current can be obtained as

$$I_{exp} = 0.25*\beta*I_{static} + 0.375*I_{static}. \quad (3)$$

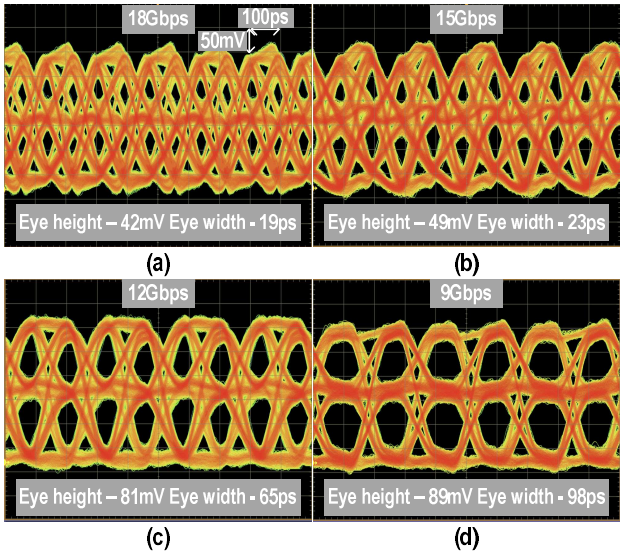


Fig. 7. Eye diagrams of the proposed transmitter at (a) 18 Gbps, (b) 15 Gbps, (c) 12 Gbps, (d) 9 Gbps.

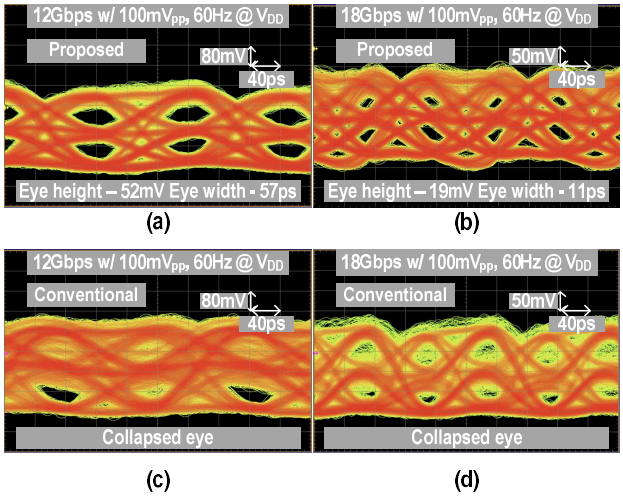


Fig. 8. Eye diagrams under 100 mVpp, 60 Hz supply : (a) proposed design at 12 Gbps, (b) proposed design at 18 Gbps, (c) conventional design at 12 Gbps, and (d) conventional design at 18 Gbps.

By substituting (1) into I_{static} in (3) and applying the normalized static current of the proposed output driver and the conventional P-over-N output driver, the final expression for the current reduction ratio is obtained as follows.

$$I_{exp.reduction} = (1 - I_{exp.prop} / I_{exp.conv}) * 100 \quad (4)$$

The expected current reduction ratio derived from (4) is shown in Fig. 5(b). Considering the employed process, the current reduction is estimated to be 51% when β is 1.33 [7], [11]. This result is consistent with the 97% reduction in static current during middle-level generation and can be explained by E[M] in (2) and the absence of current consumption during the low-level state.

III. Measurement Results

The proposed PAM-3 transmitter was implemented in a 14-nm FinFET process. For power consumption comparison, a transmitter employing the proposed output driver and

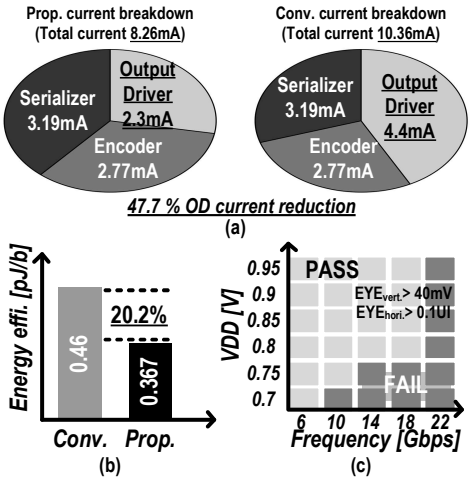


Fig. 9. Measured (a) current breakdown of the proposed transmitter with conventional transmitter (b) comparison of energy efficiency (c) shmoo plot of the proposed design.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	ISSCC, 24[3]	TCAS2, 24[5]	TCAS1, 25[10]	ISSCC, 19[9]
Technology	*14nm*	65nm	28nm	65nm	28nm
Data Rate	*18 Gb/s*	25.2 Gb/s	12 Gb/s	22.5 Gb/s	27 Gb/s
Signaling	*PAM-3*	PAM-3	PAM-3	PAM-3	PAM-3
Energy Efficiency	*0.367 pJ/b*	1.13 pJ/b	1.26 pJ/b	***0.75 pJ/b	**0.395 pJ/b
Supply noise Immunity	*100mVpp @ 60 Hz*	N	N	N	N
Output Driver type	*P-over-N with reverse CMOS*	P-over-N	P-over-N	N-over-N with floating mid	N-over-N
Supply	*0.8 V*	1 V	1 V	1/*0.6 V	-/*0.6 V
Power Consumption	*6.608 mW*	28.48 mW	15.12 mW	***16.97 mW	**10.69 mW
Area	*0.0084 mm²*	0.0196 mm²	0.007 mm²	0.0184 mm²	0.0091 mm²

*An additional VDD supply is used for V_{DDQ} **TX only ***Exclude FFE

another transmitter using a conventional P-over-N output driver were designed together. The die micrograph and area breakdown are shown in Fig. 6.

Fig. 7 shows the PAM-3 eye diagrams of the proposed transmitter at data rates of 18, 15, 12, and 9-Gbps. At 18 Gbps, the vertical and horizontal eye margins are 42mV and 19 ps, respectively. Fig. 8 shows the eye diagram under applied supply noise. Fig. 8(a), (b) correspond to the proposed design, while Fig. 8 (c), (d) show a conventional output driver. The proposed design maintains vertical and horizontal eye margin of more than 15 mV and 0.1 UI, respectively, at 12-Gbps and 18-Gbps under a 100m V_{pp}, 60 Hz supply noise, whereas the conventional design shows no observable eye margin.

Fig. 9(a) shows the measured current breakdown of the proposed and conventional design, where both transmitter were measured using the same channel and output swing for a fair comparison. While the other blocks consume the same current, the proposed output driver achieves a 47.7% current reduction, consistent with Fig. 5(b). As shown in Fig. 9(b), this reduction results in 20.2% improvement in energy efficiency. Fig. 9(c) presents the shmoo plot, showing operation from 6 to 18 Gbps at a nominal V_{DD} of 0.8 V. Table I summarizes the performance comparison with prior works. The proposed design achieves the highest energy efficiency among transmitters using P-over-N drivers and demonstrates robust immunity to supply noise. With an energy efficiency of 0.367 pJ/b, it also achieves higher efficiency than N-over-N-based transmitters without requiring an additional V_{DDQ}.

IV. Conclusion

This paper presents a PAM-3 transmitter employing a low-power output driver that is robust to V_{DD} ripple. The proposed output driver reduces the static current by 97%, resulting in a 47.7% reduction in the total driver current. Consequently, a 20.2% energy-efficiency improvement is achieved over a conventional transmitter. In addition, the mid-level generation transistors are decoupled from the power rail, enhancing robustness against V_{DD} ripple. The proposed design was implemented in a 14-nm FinFET process and achieved an energy efficiency of 0.367 pJ/b with an active area of 0.00843 mm^2.

Acknowledgment

This work was supported in part by Samsung Electronics Company Ltd. The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

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