A Tunable 30–124 GHz Frequency Divider-by-4 in 22 nm FDSOI CMOS

Victor Lasserre, Sarah Koop-Brinkmann, Vadim Issakov
Institute for CMOS Design, Braunschweig University of Technology, Germany
v.lasserre@tu-braunschweig.de

***Abstract* — This work describes design of a CML frequency divider-by-4 combining dynamic latches using load modulation and inductive peaking techniques. Dynamic CML latch realization helps achieving higher input frequencies at cost of a narrower locking range for a given bias setting. We show that the shunt inductive peaking technique, widely used in static CML latches, is also applicable to the *dynamic* CML latch realization with load modulation. It helps extending the highest input frequency in our realization by 30%, yet *without reduction* of locking range. The presented chip achieves a measured locking range of 49 GHz and a 94 GHz operating range. The maximum input frequency is 124 GHz, which is to the best of authors' knowledge the highest reported frequency for a CML divider in CMOS. It consumes only 8.2 mW from a single 0.8 V supply.**

I. Introduction

Frequency divider is an essential component in the local oscillator (LO) signal generation distribution network. If used as a pre-scaler in a phased-locked-loop (PLL), a divider needs to operate at the highest frequency in a system. Frequency range around 122 GHz is of interest primarily because of the industrial, scientific, medical (ISM) band, used for consumer and industrial radar applications [1]. A frequency divider operating up to 122 GHz is needed in a system having a VCO with a fundamental tone generation f_{O} around 122 GHz. Alternatively, in a 60 GHz radar, one can distribute f_{O} at 60 GHz, while a flip-flop-based frequency divider around $2f_{\mathrm{O}}$ at 120 GHz can be used to generate 0° and 90° phases for an I/Q radar operation [2].

Flip-flop based static dividers based on current-mode logic (CML) offer robust division over a wide frequency range, enabling good design margins. Yet, achieving such high operating frequency by a flip-flop-based divider is a challenge. Division frequencies beyond 100 GHz have been demonstrated in BiCMOS technologies, yet at cost of a higher power consumption [3]. Alternatively, dynamic dividers, e.g. Miller, can reach even higher frequencies, but lack I/Q phases.

Classical static CML-based dividers in CMOS typically show frequencies below 70 GHz [4]. The operation speed is limited by the time constant τ at the node between the data and latch pairs. $f_{\mathrm{in,max}}$ can be increased by an asymmetric operation of the D-latch [5] or even by fully omitting the hold stage [6]. However, this narrows the locking range, as the node is discharged more rapidly throughout the hold period. To counteract this, [7] modulates the resistive load of the dynamic latch to optimize the time constant τ both in read and in hold phase. In this way, in [8] a maximum frequency of 100 GHz is achieved. However, at higher self oscillation frequencies f_{osc} the locking range decreases to about 4 GHz only.

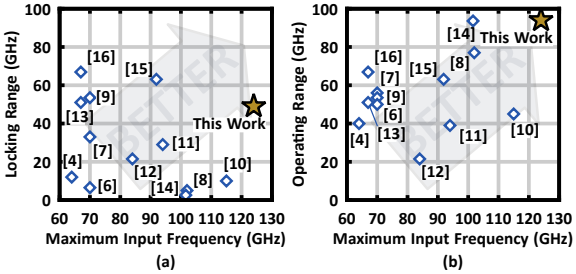

Fig. 1. Comparison of locking range and maximum input frequency with state of the art CMOS frequency dividers.

In this work, we combine load modulated dynamic CML latches with an inductive shunt peaking technique to achieve the highest reported $f_{\mathrm{in,max}}$ of 124 GHz in CMOS, while keeping a wide locking range of 49 GHz, as shown in Fig. 1.

II. Circuit Design

Fig. 2 shows the block diagram of the designed frequency divider. Each block represents a dynamic D-latch. For an even frequency division factor N, one can use N D-latches cascaded in a single feedback loop with a cross-connection. Our observations show that a direct divide-by-4 realization ($N = 4$) achieves a higher self-oscillation frequency f_{osc} and higher DC efficiency as opposed to realizing :4 by two cascaded divide-by-2 stages (each with $N{=}2$).

The speed of a dynamic CML stage, specifically the maximum input frequency $f_{\mathrm{in,max}}$ and minimum input frequency $f_{\mathrm{in,min}}$, result from the charging and discharging time of the output nodes Q and $\overline{Q}$ (Fig. 2). In data mode (*CLK* high), a small time constant τ increases $f_{\mathrm{in,max}}$; conversely, in latch mode (*CLK* low), a large τ leads to a low $f_{\mathrm{in,min}}$ [7]. In order to increase the operating speed, the transistor dimensions of M_{1-3} were optimized such that the time constant $\tau = R_{\mathrm{P}}C_{\mathrm{P}}$ is minimized in data-mode, where R_{P} and C_{P} are values of an equivalent parallel RC circuit at nodes Q, $\overline{Q}$. Thus, the length of transistors M_{1-3} is set to the minimum of $L = 18$ nm, while the gate widths are set to 10 μm, 8 μm and 6 μm, respectively.

To further increase the speed of the divider, we analyze the impact of inductive peaking on a dynamic load-modulated CML stage. We added a shunt peaking inductor L_{Peak} in series to the load-modulated PMOS transistors M_3, as shown in Fig. 2. As a simplified analytical model, the real part and the imaginary part of the admittance Y_{L} at the nodes Q and $\overline{Q}$ are first determined, where ω denotes the angular frequency, C_{L} the capacitive load at the node, L_{Peak} the shunt inductance, R_{ind} its associated losses, R_{ch} the modulated channel resistance

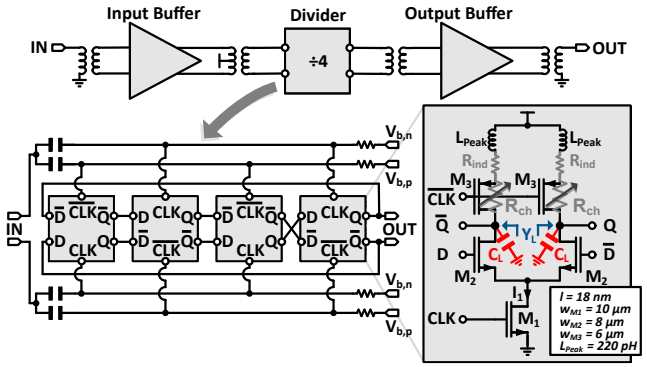

Fig. 2. Block diagram and schematic of the implemented dynamic frequency divide-by-4.

of transistor M_3, and R_{out,M_2} the equivalent output resistance looking into the drain of transistor M_2

$$\Im\{Y_L\} = \omega \left[C_L - \frac{L_{\text{Peak}}}{(R_{\text{ch}} + R_{\text{ind}})^2 + (\omega L_{\text{Peak}})^2} \right] , \quad (1)$$

$$\Re\{Y_L\} = \frac{1}{R_{\text{out,M2}}} + \frac{R_{\text{ch}} + R_{\text{ind}}}{(R_{\text{ch}} + R_{\text{ind}})^2 + (\omega L_{\text{Peak}})^2} . \quad (2)$$

From these, the equivalent parallel capacitance can be calculated as $C_P = \Im\{Y_L\}/\omega$, and the equivalent parallel resistance follows as $R_P = 1/\Re\{Y_L\}$. As can be seen from Eq. 1, the equivalent load capacitance for $L_{\text{Peak}} = 0$ consists solely of the parasitic C_L at the output node. With the inclusion of L_{Peak}, this capacitance can be reduced. However, an excessively large L_{Peak} diminishes this effect. For a more detailed analysis, the upper four plots in Fig. 3 show the simulated C_P and R_P in both data mode ($|V_{GS,M_3}| = 600\,\text{mV}$) and latch mode ($|V_{GS,M_3}| = 200\,\text{mV}$), and compare them with the analytical results calculated from Eqs. 1 and 2. The simulation results and the analytical calculations show good agreement. Only in data mode, for large inductance values, the influence on the equivalent resistance R_P is overestimated. While in the data mode the inclusion of L_{Peak} has only a minor effect on the parallel resistance R_P, the parallel capacitance can be reduced *by a factor of 1.9* for $L_{\text{Peak}} = 220\,\text{pH}$. Subsequently, as indicated by the color shading in the figures, the effective time constant τ is *minimized*. In latch mode, the channel resistance is high. Hence, the effect of the series inductance becomes negligible and τ remains high. To sum up, with inductive peaking, τ is reduced in data mode and results in a higher $f_{\text{in,max}}$; τ is unaffected in latch mode, thus $f_{\text{in,min}}$ is not reduced. This results in an effective *extension of the locking range*.

Fig. 4a and 4b underline the impact of the added peaking inductors. Fig. 4a shows the self oscillation frequency versus L_{Peak}. For small inductor values, the oscillation frequency of the divider increases linearly. At around 200 pH, f_{osc} starts to saturate, until above 300 pH the oscillation frequency begins to drop again, showcasing the ideal inductance value of 220 pH. While Fig. 4b illustrates the bandwidth extension of a single latch stage in data-mode.

To further visualize the operating principle, Fig. 3 (bottom) shows the equivalent capacitance C_P versus the gate-source

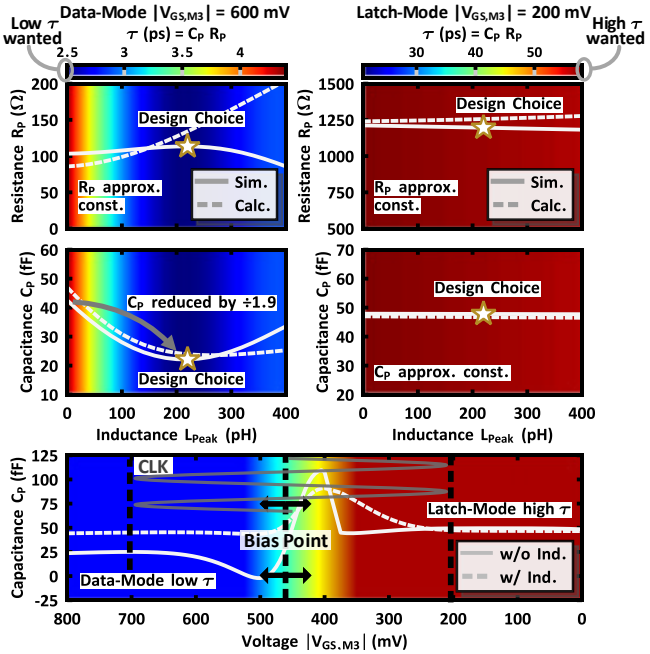

Fig. 3. Top: Effective parallel resistance R_P, parallel capacitance C_P, and resulting time constant τ versus peaking inductance L_{Peak} in data-mode ($|V_{GS,M_3}| = 600\,\text{mV}$) and latch-mode ($|V_{GS,M_3}| = 200\,\text{mV}$), comparing simulation and analytical model. Bottom: Effective capacitance C_P versus $V_{b,p}$, with and without peaking inductor.

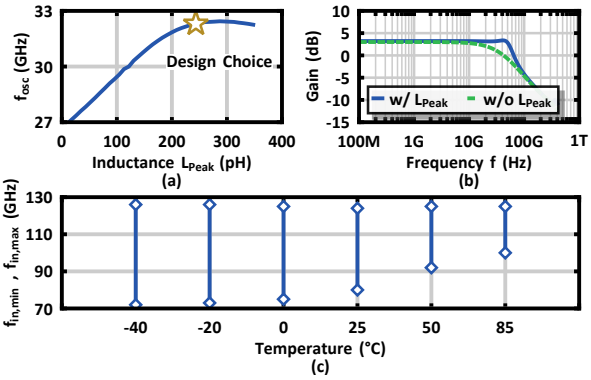

Fig. 4. Inductance L_{Peak} versus self-oscillation frequency (a), bandwidth extension of single stage latch gain in data-mode (b) and simulated locking range versus temperature range for industrial grade -40 to +85 °C (c).

voltage $|V_{GS,M3}|$ of transistor M_3. When a CLK signal is applied, $|V_{GS,M3}|$ is modulated around the operating point, and, consequently, both C_P and R_P are varied accordingly. Thus, the operating point determines the duty cycle for which transistor M_3 remains in data mode and in latch mode. In this way, the self-oscillation frequency of the divider can be adjusted.

In addition to the bias voltage $V_{b,p} \approx V_{DD} - |V_{GS,M3}|$, which sets the operating point of M_3, the circuit behavior also depends on $V_{b,n}$, which sets the bias point of M_1 and determines the current I_1. Both bias voltages can be used to tune the circuit characteristics. Fig. 5 shows the self-oscillation frequency f_{osc} (a), and the DC consumption P_{DC} (b) of the divider core for different bias voltages $V_{b,n}$ and $V_{b,p}$.

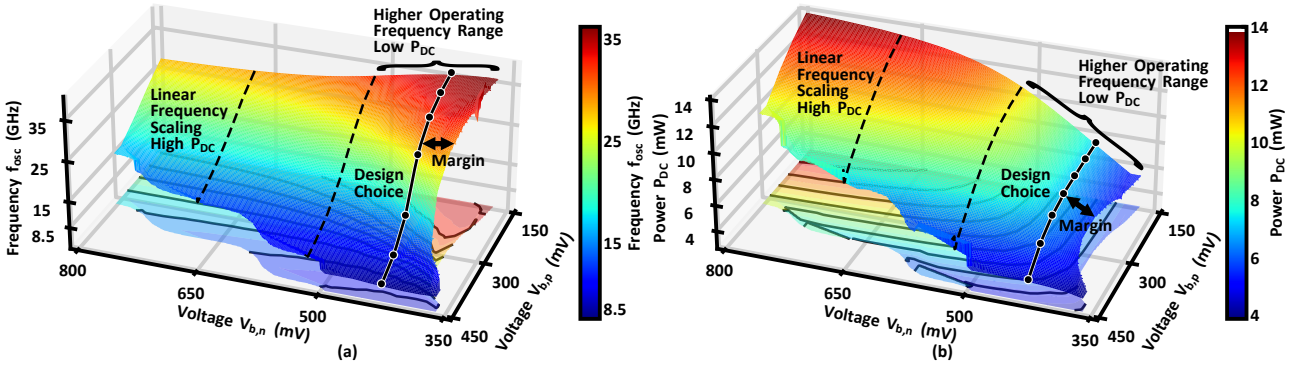

Fig. 5. Simulated self oscillation frequency (a), and power consumption of the divider core (b) versus bias voltages $V_{\mathrm{b,n}}$ and $V_{\mathrm{b,p}}$.

Tuning $V_{\mathrm{b,n}}$ exhibits less impact compared to $V_{\mathrm{b,p}}$. For high $V_{\mathrm{b,n}}$ values (e.g. $> 650\,\mathrm{mV}$), the self-oscillation frequency can be tuned linearly via the voltage $V_{\mathrm{b,p}}$. However, this is achieved at the expense of a smaller operating region and increased power consumption. Thus, it is advisable to use lower $V_{\mathrm{b,n}}$ values (i.e. $425\,\mathrm{mV}$), as this allows both a higher maximum oscillation frequency and a lower minimum oscillation frequency, while reducing the DC power consumption by about a factor of two, as shown in Fig. 5. The highest simulated f_{osc} is $35\,\mathrm{GHz}$, which would result in a maximum input frequency of $140\,\mathrm{GHz}$. On the other hand, the lowest simulated f_{osc} is approximately $7\,\mathrm{GHz}$.

Fig. 4c shows the simulated locking range of the divider over the industrial-grade temperature range $-40\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$. While $f_{\mathrm{in,max}}$ remains nearly constant over the entire range, $f_{\mathrm{in,min}}$ increases towards higher temperatures, effectively resulting in a narrower locking range. However, it remains above $20\,\mathrm{GHz}$. The degradation is likely related to reduced CML stage gain and thus lower swing at higher temperatures.

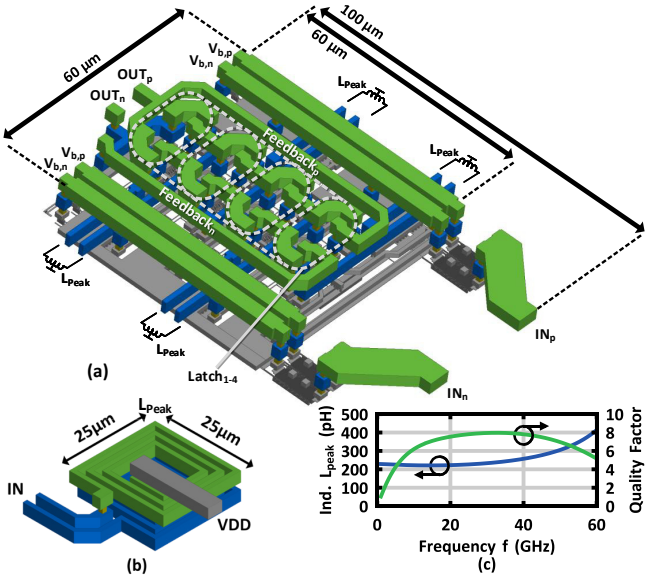

Fig. 6. 3D model of the divider core layout.

The layout of the divider core is crucial for the circuit performance. At high frequencies (with input frequencies extending up to the D-band and output frequencies up to $35\,\mathrm{GHz}$), the interconnects add additional capacitances and resistances at the output nodes and thus also affect the time constant τ. Consequently, the layout was kept as compact as possible and, where feasible, the upper metal layers were used, since these exhibit a significantly higher thickness (Fig. 6a).

The inductors L_{Peak} are realized in the highest copper metal layers (both having a thickness of $2.95\,\mu\mathrm{m}$). To save chip area, two rectangular inductors with three windings and identical dimensions are stacked on top of each other. At the output, both inductors are connected by vias. The same node is also used to connect the supply voltage, as shown in Fig. 6b. The simulated single inductor L_{Peak} exhibits an inductance of $220\,\mathrm{pH}$ and a quality factor Q of 8, as illustrated in Fig. 6c.

A single-stage neutralized differential CS buffer is added to the input and output of the divider core to increase the input voltage swing and to drive the $50\,\Omega$ measurement equipment.

III. Measurement Results

The proposed dynamic frequency divider is fabricated in $22\,\mathrm{nm}$ FDSOI CMOS. Fig. 7 illustrates the annotated chip micrograph and measurement setup. The core area of the divider is $0.0143\,\mathrm{mm}^2$. The input signal is provided by a Keysight E8257D signal generator. Above $67\,\mathrm{GHz}$, frequency extensions for the E-, W-, and D-band are used in combination with programmable attenuators to generate a tunable input signal. The output signal and PN are measured by FSWP-50.

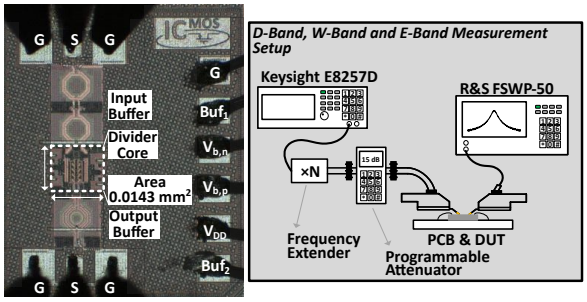

Fig. 7. Annotated chip micrograph and measurement setup.

Table 1. Comparison with state-of-the-art CMOS mm-wave Frequency divider designs.

Reference	This work	[4]	[8]	[10]	[14]	[15]	[16]
Technology	22 nm FDSOI	90 nm CMOS	28 nm CMOS	22 nm FDSOI	28 nm CMOS	40 nm CMOS	28 nm CMOS
Topology	Dyn. CML Ind. peaking	CML Ind. peaking	Dyn. CML	Dyn. CML	RO-ILFD	LC-ILFD	RO-ILFD auto tuning
Division Factor	4	2	4	4	5	2	6
Locking Range (GHz)	75 - 124	24 - 43	44.3 - 68.2	77 - 94	53.9 - 69.1	28.8 - 91.9	0.1 - 67
Operating Range (GHz)	30 - 124	24 - 64	25 - 102	75 - 110	8 - 101.6	28.8 - 91.9	0.1 - 67
P_{DC} (mW)	8.2[a]	30.1	2.8	7.5	5.6	5.8	11.9
FOM[b] (GHz/mW)	740	27.1	582.1	213.1	187.6	999.8	376.7
Core Area (mm^2)	0.014	0.04	0.00064	0.12	0.0013	0.02	0.0029

[a] Divider core only. [b] FOM $= \frac{\mathrm{LR\,(GHz)} \cdot f_{MAX}\,\mathrm{(GHz)}}{P_{DC}\,\mathrm{(mW)}}$ [17].

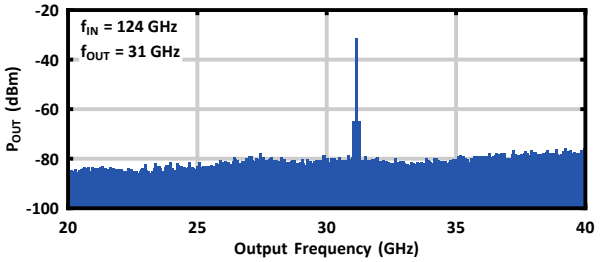

Fig. 8. Measured output spectrum without loss correction.

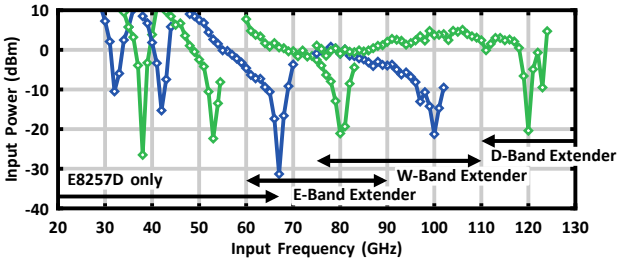

Fig. 9. Measured sensitivity curve.

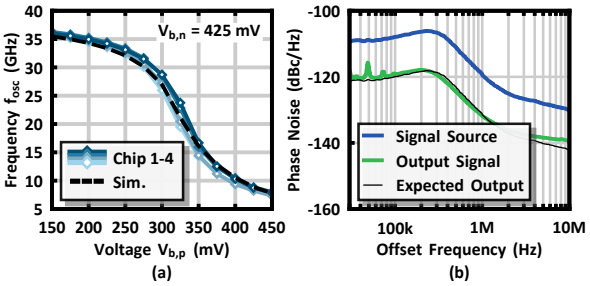

Fig. 10. (a) Comparison of measured self oscillation frequency f_{osc} for multiple dies and simulation results, and (b) phase noise comparison of divider output and input signals.

The measured DC power consumption of the divider core amounts to 8.2 mW at a supply voltage of 0.8 V. As visualized in Fig. 8, a single output peak is measured at $\frac{1}{4}$ of the input frequency. The maximum locking range of 49 GHz from 75–124 GHz with a f_{osc} of 120 GHz is measured (Fig. 9).

For various bias settings, the operating range spans 94 GHz from 30–124 GHz. As shown in 10a, the self-oscillation frequency exhibits only small differences at the chosen bias setting of $V_{b,n} = 425$ mV. Fig. 10b illustrates the output phase noise scaling by $20\log(4)$ with respect to the input signal.

References

[1] V. Issakov *et al.*, "A Highly Integrated D-Band Multi-Channel Transceiver Chip for Radar Applications," in *BCICTS*, 2019, pp. 1–4.

[2] S. Koop-Brinkmann *et al.*, "A Low Conversion Loss 120 GHz Passive IQ Down-Conversion Subharmonic Mixer with Multiphase LO Distribution in 28 nm CMOS," in *RFIC*, 2024, pp. 371–374.

[3] L. Polzin *et al.*, "A 142-GHz 4/5 Dual-Modulus Prescaler for Wideband and Low Noise Frequency Synthesizers in 130-nm SiGe:C BiCMOS," *MWTL*, vol. 33, no. 6, pp. 867–870, 2023.

[4] A. Patnaik *et al.*, "A 24–64 GHz Wideband Static CML Frequency Divider in a 90-nm CMOS Technology," *MWTL*, no. 1, pp. 71–74, 2025.

[5] V. Issakov *et al.*, "Low-voltage flip-flop-based frequency divider up to 92-GHz in 130-nm SiGe BiCMOS technology," in *INMMiC*, 2017.

[6] A. Ghilioni *et al.*, "A 6.5mW inductorless CMOS frequency divider-by-4 operating up to 70GHz," in *ISSCC*. IEEE, 2011, pp. 282–284.

[7] A. Ghilioni *et al.*, "Analysis and Design of mm-Wave Frequency Dividers Based on Dynamic Latches With Load Modulation," *JSSC*, vol. 48, no. 8, pp. 1842–1850, 2013.

[8] M. Vigilante *et al.*, "A 25–102GHz 2.81–5.64mW tunable divide-by-4 in 28nm CMOS," in *A-SSCC*. IEEE, 2015, pp. 1–4.

[9] Z. Tibenszky *et al.*, "A 0.35-mW 70-GHz Self-Resonant E-TSPC Frequency Divider With Backgate Adjustment," *TMTT*, no. 4, 2022.

[10] N. Saquib *et al.*, "A 75–110 GHz Wide Band Dynamic Latch Frequency Divider in 22nm FDSOI Technology," in *MWSCAS*, 2025, pp. 932–935.

[11] D. D. Kim *et al.*, "A 94GHz Locking Hysteresis-Assisted and Tunable CML Static Divider in 65nm SOI CMOS," in *ISSCC*, 2008, pp. 460–628.

[12] D. D. Kim *et al.*, "A Low-Power mmWave CML Prescaler in 65nm SOI CMOS Technology," in *CSICS*. IEEE, 2008, pp. 1–4.

[13] A. I. Hussein *et al.*, "Design and Self-Calibration Techniques for Inductor-Less Millimeter-Wave Frequency Dividers," *IEEE JSSC*, vol. 52, no. 6, pp. 1521–1541, 2017.

[14] A. Garghetti *et al.*, "Analysis and Design of 8-to-101.6-GHz Injection-Locked Frequency Divider by Five With Concurrent Dual-Path Multi-Injection Topology," *JSSC*, vol. 57, no. 6, pp. 1788–1799, 2022.

[15] Q. Jiang *et al.*, "Analysis and Design of Tuning-Less mm-Wave Injection-Locked Frequency Dividers With Wide Locking Range Using 8th-Order Transformer-Based Resonator in 40 nm CMOS," *JSSC*, vol. 57, no. 9, pp. 2812–2828, 2022.

[16] M. Baert *et al.*, "A PVT-Compensated 0.1–67 GHz Injection-Locked Frequency Divider with Replica-based Automatic Tuning," in *2021 RFIC*. IEEE, 2021, pp. 75–78.

[17] T.-N. Luo *et al.*, "A 0.8-mW 55-GHz Dual-Injection-Locked CMOS Frequency Divider," *TMTT*, vol. 56, no. 3, pp. 620–625, 2008.