Revealing the True Thermal Limits of Oxide-Channel FeFETs: Gate Stack versus Channel

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***Abstract*—We present a first systematic study of the impact of thermal budgets on tungsten- and gallium-doped In_2O_3 oxide-channel ferroelectric field-effect transistors (OS-FeFETs) employing a laminated ferroelectric gate stack. The devices utilize an 8 nm HZO / 3 nm Al_2O_3 / 8 nm HZO (8/3/8) laminated stack and are capped with a 3 nm HfO_2 + 3nm Al_2O_3 layer to enable post-channel thermal processing. We show that channel capping is essential for high-temperature annealing after channel deposition; uncapped devices become non-conductive, whereas capped devices remain operational under identical thermal conditions. In addition, a comparison between a conventional 12 nm HZO / 3 nm Al_2O_3 (G-IL) stack and the laminated 8/3/8 stack on IGO channels shows that the laminated structure sustains significantly longer annealing durations at 650 ^oC. Despite aggressive thermal processing, the laminated FeFETs exhibit robust multi-bit retention with minimal degradation even at 125 ^oC up to the maximum thermal budget limit prior to channel failure, while the ferroelectric stack remains functional beyond the channel degradation. These results highlight the importance of channel capping and ferroelectric stack + channel engineering for enabling thermally robust oxide-channel FeFETs with stable retention for 3D NAND applications.**

I. Introduction

Oxide-semiconductor (OS) channels integrated with fluorite-based HfO_2 ferroelectric materials have recently emerged as a promising approach for next-generation 3D vertical NAND flash (3D-NAND) technologies as scaling continues (Fig. 1a)[1], [2], [3]. Incorporating ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) enables lower write voltages, faster program/erase operation, and reduced cell-to-cell interference [4], [5], [6]. In parallel, the use of OS channels offers several advantages compared to conventional poly-Si channels, including the potential elimination of the channel interfacial layer and a reduction in process thermal budgets [7], which in conventional poly-Si NAND technologies can exceed 800°C.

Despite these advantages, post-channel fabrication steps in 3D-NAND integration can still involve thermal processes exceeding 400°C. Therefore, understanding the impact of such elevated thermal budgets on the electrical performance and reliability of OS-channel FeFET devices is critical for practical implementation.

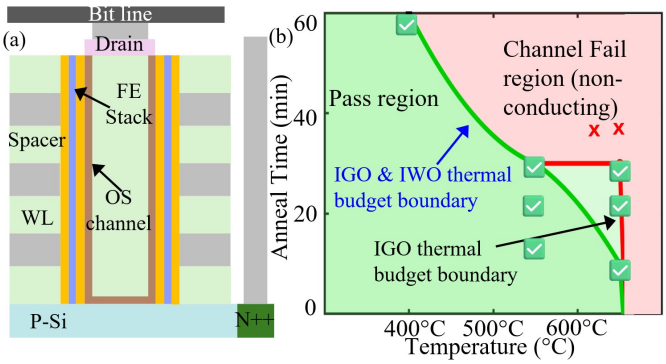

Fig. 1. (a) Schematic of a 3D Fe-NAND architecture with an oxide-semiconductor (OS) channel (b) Thermal-budget phase map defining the viable integration window for laminated OS-channel FeFETs in vertical NAND: IGO channel survives up to 650 °C for 30 min, while IWO survives only up to 650 °C for 10 min of post capping annealing (PCA).

In this work, we present a comprehensive investigation of OS-channel FeFETs subjected to high-temperature annealing conditions relevant to 3D-NAND processing. Devices employing indium–tungsten oxide (IWO) and indium–gallium oxide (IGO) channels are evaluated with two gate-stack configurations: a laminated ferroelectric stack (8/3/8) and a gate-side interlayer (G-IL) stack. We establish the thermal survivability limits (Fig. 1b) of OS-channel FeFETs (IWO Vs. IGO) and analyze their memory window and retention behavior before and after thermal treatments. Notably, the retention characteristics remain largely unchanged even after high-temperature annealing, demonstrating thermally robust data retention up to 125°C. These results provide important insights into the thermal stability, memory window evolution, and retention reliability of OS-channel FeFETs under post-channel thermal budgets relevant for future 3D-NAND integration.

II. Results and Discussion

A. Capping requirement for PCA immunity of FeFET

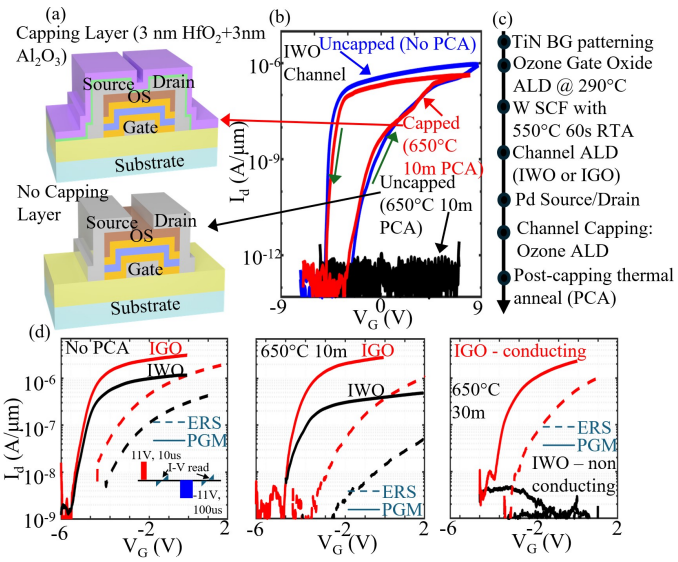

Fig. 2. (a) 3D Schematic of OS-FeFET used in this work with and without optimized capping layer (b) DC-IV characteristics showing capping-enabled high-T PCA immunity on laminated IWO FeFET, while uncapped FeFETs become non-conductive after high-T anneal (c) Fabrication process flow for capped OS-FeFET (d) Pulsed I_d-V_g characteristics for laminated stack IWO and IGO FeFET without PCA and after 650°C PCA for 10 minutes and 30 minutes respectively.

The devices were annealed after capping the channel with a 3 nm HfO_2 / 3 nm Al_2O_3 layer, as illustrated in Fig. 2a (Post-Capping Anneal, PCA). Channel capping reduces the sensitivity of OS channels to thermal processing effects [8]. To highlight the importance of this capping layer, the capped and uncapped laminated (8/3/8) IWO FeFET devices were annealed at 650°C for 10 minutes under PCA conditions. The results show that the capped device remains conductive after PCA, whereas the uncapped device becomes non-conductive under the same thermal conditions. Fig. 2d presents the pulsed I_d-V_g characteristics at 650°C annealing conditions. The laminated stack IWO FeFET becomes non-conductive (indicative of channel failure) when the annealing duration exceeds 10 minutes, while the laminated IGO FeFET maintains channel conductivity for annealing times up to 30 minutes.

B. Thermal Survivability for different Ferroelectric Oxide stacks

To understand how different gate stack configurations respond to identical PCA conditions, laminated and G-IL (gate-side interlayer) stacks were fabricated on the same IGO channel, as shown in Fig. 3a. Since the channel material and the process flow is identical, any differences observed in the electrical characteristics pertaining to channel failure arise from the gate stack configuration itself. Fig. 3b presents the DC I_d–V_g and I_g–V_g characteristics for both stacks before PCA and after PCA at 650°C on the IGO channel. The laminated 8/3/8 stack maintains a clear memory window (MW)

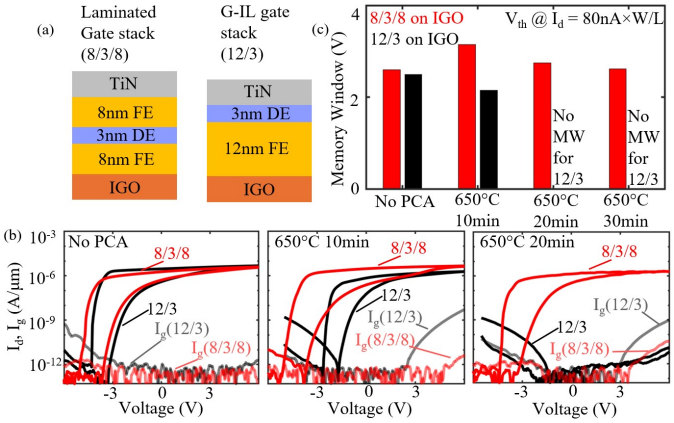

Fig. 3. (a) Schematic of the two FeFET gate stack configurations studied: laminated stack (8 nm FE / 3 nm DE / 8 nm FE) and gate-side interlayer (G-IL) stack (12 nm FE / 3 nm DE) on IGO channels. (b) DC I_d-V_g and I_g-V_g comparing the laminated (8/3/8) and G-IL (12/3) stacks measured under different post-capping anneal (PCA) conditions: no PCA, 650°C for 10 min, and 650°C for 20 min. (c) Extracted memory window (MW) for the two stacks under the different PCA conditions.

and conductive I–V behavior for annealing times up to 30 min (Fig. 2d and Fig. 3b), whereas the G-IL (12/3) stack fails to exhibit a measurable MW or standard I–V characteristics beyond 10 min of PCA. These results indicate that, despite having the same channel, the laminated stack OS-FeFET demonstrates superior thermal robustness and delayed channel failure compared to the G-IL stack under identical annealing conditions. Furthermore, the 12/3 stack exhibits a significantly larger increase in gate leakage after PCA compared to the 8/3/8 stack. Fig. 3c shows the extracted MW, confirming that the 12/3 stack exhibits no measurable MW after 650°C for 20 min due to device failure, while the laminated stack retains a finite MW.

C. Retention comparison for different channels before and after PCA for laminated stack OS-FeFET

To understand the impact of thermal annealing on device retention, retention measurements (Fig. 4a) were performed before and after PCA under various annealing conditions on the laminated stack. Fig. 4(b–c) shows the retention characteristics of laminated OS-FeFETs with IWO and IGO channels, demonstrating robust retention at 25°C both before PCA and after the maximum PCA conditions of 550°C and 650°C prior to device failure. Fig. 4d summarizes the retention results by plotting the change in memory window (MW) at 1000 s for all PCA conditions studied in this work. At 550°C, increasing the PCA time initially causes a slight degradation in retention; however, further increase in annealing time lead to an improvement in retention (red line in Fig. 4d). At 650°C, retention degradation is observed as the devices approach device failure for both channel materials (blue line in Fig. 4d). For the 400°C anneal with a duration of 60 minutes, the retention behavior remains comparable to the no-PCA condition.

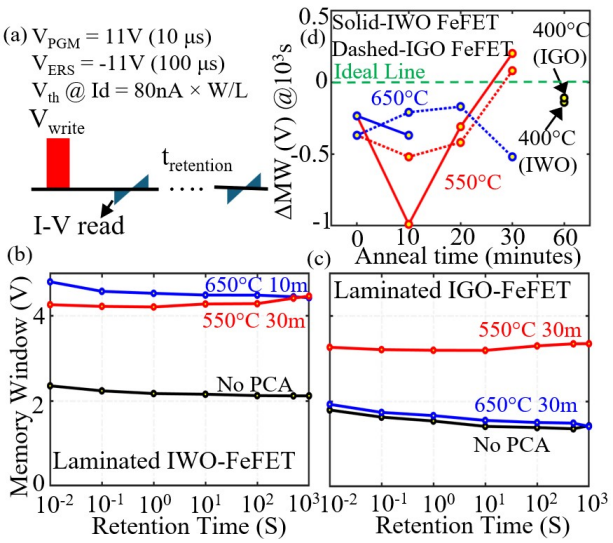

Fig. 4. (a) Retention measurement scheme and parameters used in this work. (b–c) Memory window as a function of retention time at room temperature for laminated stack (8/3/8) IWO and IGO FeFETs under the maximum annealing duration at different temperatures prior to device failure. (d) Summary of the memory window change at 1000 s for IWO and IGO FeFETs under various annealing conditions.

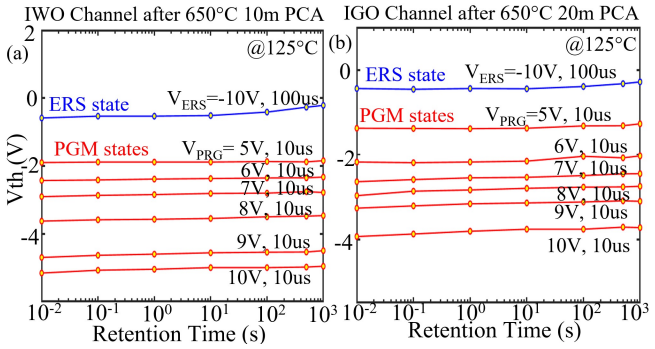

Fig. 5. Demonstration of robust multi-state retention at 125°C for (a) Laminated stack IWO and (b) IGO OS-FeFET after 650°C PCA

Fig. 5 shows robust multi-state retention at 125°C for both IGO and IWO FeFETs after 650°C PCA, with minimal retention degradation up to 1000 s.

D. Decoupling PCA Impacts on Ferroelectric oxide and Channel material

To understand the origin of device failure, it is necessary to decouple the degradation of the ferroelectric gate oxide from that of the OS channel. C–V_g measurements were performed on laminated stack IWO and IGO devices with the source and drain shorted under different PCA conditions, as shown in Fig. 6(a–c). At 650°C, the IGO channel exhibits electron accumulation at higher gate bias for PCA durations up to 30 min, whereas the IWO channel shows electron accumulation only up to 10 min of PCA similar to no-PCA case. The presence of electron accumulation at high gate bias indicates

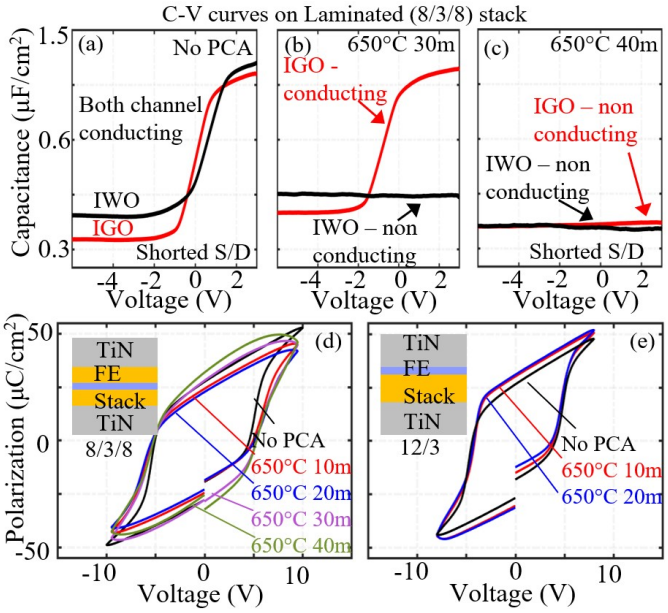

Fig. 6. (a–c) Before and Post-650°C PCA C–V shows flat response for laminated stack IWO (beyond 10 min) and IGO (beyond 30 min), indicating no electron accumulation and loss of channel conductivity (channel failure). (d-e) MFM P–V shows for laminated and G-IL stack showing minimal ferroelectric degradation at 650°C, even beyond the channel failure time for respective stack.

a conductive channel, consistent with the observed conductive I–V behavior.

However, beyond 10 min for IWO and 30 min for IGO, a flat C–V response is observed (Fig. 6(b–c)), indicating channel depletion and the absence of electron accumulation. The lack of electron accumulation suggests a loss of channel conductivity, leading to non-conductive I–V characteristics and ultimately channel failure.

In contrast, polarization–voltage measurements performed on MFM capacitors show no degradation in ferroelectric properties at 650°C (Fig. 6(d-e)), which is even beyond the channel failure time for the respective gate stack (30 min and 10 min for 8/3/8 and 12/3 respectively). This confirms that device failure originates from the loss of channel conductivity, rather than degradation of the ferroelectric gate stack, regardless of the gate stack configuration.

E. ISPP Performance of OS-FeFETs Before and After PCA on laminated stack (8/3/8) OS-FeFET

Incremental step pulse programming (ISPP) performance was measured for laminated stack IWO and IGO channel devices before and after PCA, as shown in Fig. 7(a–b). ISPP characteristics under increasing thermal budgets show minimal change in average ISPP slope, albeit being consistently lower for IGO than IWO FeFETs (Fig. 7c)

F. DFT Insights into Channel Conductivity Degradation

O_2 linkage defects in In-rich oxides promote the formation of oxygen vacancies (V_O), which act as donor states and enhance channel conductivity. When the O_2 bond breaks, the

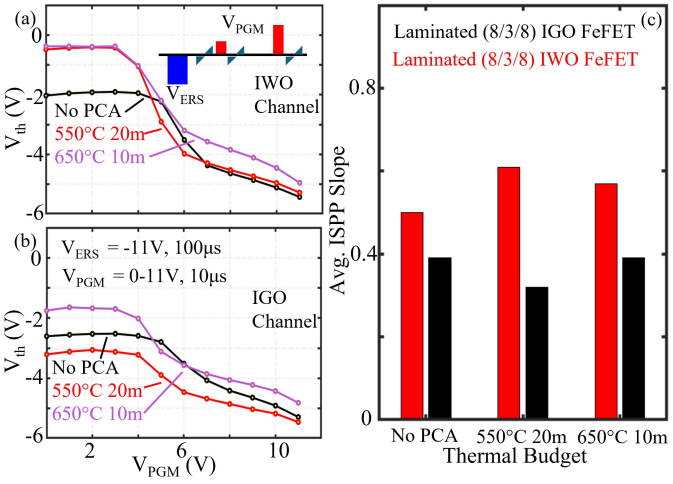

Fig. 7. (a–b) ISPP characteristics of laminated stack IWO- and IGO-channel FeFETs without PCA and after 550 °C/20 min and 650 °C/10 min PCA (c) Average ISPP slope, showing minimal PCA impact and consistently higher ISPP slope for IWO than IGO.

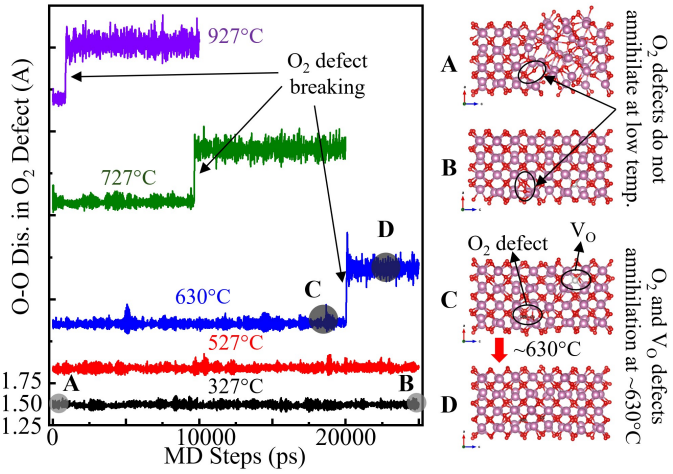

Fig. 8. Molecular Dynamics (MD)-tracked O–O linkage distance versus time at different temp. A stable O_2 linkage persists for longer time up to 530°C, whereas at 630°C the O–O bond ruptures in a shorter time scale and the resulting O_i recombines with V_O.

resulting oxygen interstitial (O_i) can recombine with V_O, thereby quenching vacancy donors and suppressing conduction. Temperature-dependent molecular dynamics (MD) simulations predict that the O_2 bond remains stable for longer durations up to approximately 550°C, but dissociates on a much shorter timescale at around 630°C (Fig. 8). This dissociation initiates a chain-like oxygen exchange pathway that ultimately leads to O_2–V_O annihilation, consistent with the experimentally observed loss of channel conductivity. Furthermore, the time required for O_2 bond dissociation decreases as the temperature increases.

III. Conclusion

In this work, the performance and retention of oxide-semiconductor (OS) channel FeFETs were systematically investigated under post-capping annealing (PCA) conditions relevant to 3D-NAND integration. Devices employing IWO and IGO channels with laminated (8/3/8) and gate-side interlayer (12/3) ferroelectric gate stacks were evaluated under high-temperature annealing up to 650°C. The laminated stack demonstrated superior thermal robustness, maintaining conductive channel behavior and a finite memory window even after 650°C PCA for 30 min, whereas the G-IL stack failed under identical conditions. Moreover, IGO channel survives longer PCA time than IWO channel for similar laminated stack at 650°C. Retention measurements confirm thermally robust memory characteristics with minimal degradation even after high-temperature annealing. Electrical characterization and C–V analysis reveal that device failure originates from loss of channel conductivity rather than degradation of ferroelectric properties. Supported by first-principles and molecular dynamics simulations, the conductivity loss is attributed to O_2 linkage dissociation and subsequent annihilation of oxygen vacancy donors in In-rich oxide channels. These results provide critical insights into the thermal stability limits of OS-channel FeFETs and highlight the importance of gate stack engineering and channel for enabling reliable FeFET-based 3D-NAND technologies.

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