A 225.6 nW CMOS Stress Sensor Achieving a 0.05 nJ·MPa² FoM with a Time-Domain Readout

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***Abstract*— This work presents a time-domain stress sensor interface in 180 nm CMOS for energy-constrained IoT systems. By encoding stress-induced current directly into frequency via a current-controlled oscillator (CCO), the proposed architecture overcomes the conventional trade-off between sensitivity and dynamic range of voltage-domain approaches while enabling programmable sensitivity through digital accumulation time. The fabricated sensor achieves a measured power consumption of 225.6 nW, a resolution of 0.27 MPa (1σ) with a 3 ms conversion time, and a state-of-the-art resolution FoM of 0.05 nJ·MPa². This corresponds to a 15× improvement in FoM and more than three orders of magnitude reduction in power consumption compared to prior art.**

Keywords—CMOS stress sensor, piezoresistive, silicon, time-domain readout, current-controlled oscillator, ultra-low power

I. Introduction

The proliferation of IoT and edge computing demands energy-efficient sensor nodes capable of long-term battery or energy-harvesting operation [1-2]. Silicon piezoresistive stress sensing, which transduces mechanical deformation into resistance variation [3], is a critical modality for diverse applications, ranging from robotic tactile feedback [4] to biomedical force tracking [5], and structural health monitoring [6] (Fig. 1). These IoT stress sensors must satisfy three key requirements: 1) ultra-low power consumption to minimize battery drain; 2) high sensitivity to detect small deformations; 3) a wide dynamic range for diverse IoT use cases. However, conventional architectures suffer from inherent trade-offs between sensitivity and dynamic range, and milliwatt-level power making them unsuitable for IoT applications.

Conventional stress sensor interfaces primarily rely on voltage-domain sensing. As shown in Fig. 1, previous designs include an open-loop integrator structure with a SAR ADC [4], and a closed-loop implementation with DAC feedback [7]. However, increasing amplifier gain to enhance sensitivity leads to voltage saturation at either the amplifier output or ADC input, fundamentally constraining the measurable stress range. Although adjustable gain and DAC feedback can alleviate this, they cannot fully eliminate the inherent trade-off between sensitivity and dynamic range.

This work addresses this trade-off by shifting to time-domain processing. Instead of converting the stress-induced current change into a voltage, the proposed design directly modulates the frequency of a current-controlled oscillator (CCO) with the sensor current. The stress information is thus encoded in the time domain, addressing the voltage saturation issue that limits the dynamic range under high-sensitivity operation [4,7]. By decoupling sensitivity from dynamic range, a wide dynamic range is achieved while maintaining high sensitivity. Sensitivity can be adjusted by controlling the accumulation time of the digital counter, trading sensitivity for energy rather than dynamic range. Further, extending the measurement over time reduces power consumption, enabling low-power IoT operation.

This work is supported by the NRF (RS-2024-00408040, RS-2025-00562391 and IITP (IITP-2026-RS-2020-II201821), Korea. The EDA tool was supported by IC Design Education Center (IDEC), Korea. The authors used Gemini to generate the graphical elements on top of Fig. 1.

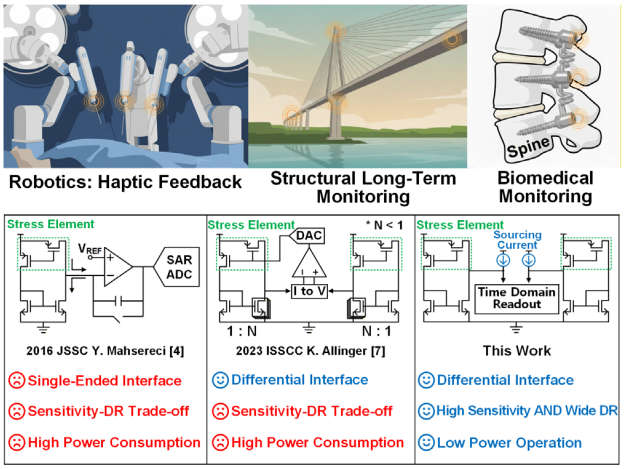


Fig. 1. Conceptual illustration of the stress sensing application and comparison of the state-of-the-art and the proposed stress sensor interface.

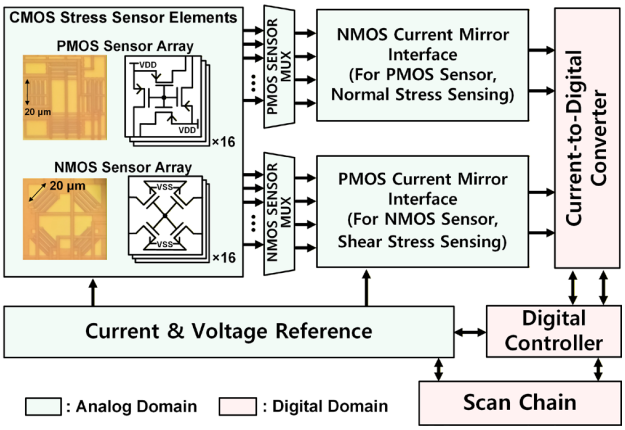


Fig. 2. Top-level architecture of the stress sensor, including CMOS PMOS/NMOS sensor element array, sensor multiplexer, current mirror interface, current and voltage references, and digital domain.

II. The Proposed CMOS Stress Sensor Interface

A. System Architecture

Fig. 2 shows the system diagram of the proposed stress sensor interface. One of multiple sensors, distributed across the chip, is selected using a multiplexer and connected to a current mirror (CM) interface. An NMOS CM interface with a PMOS sensor is used for normal stress sensing, and a PMOS CM interface with an NMOS sensor is used for shear stress sensing. Then, a current-to-digital converter digitizes the stress-induced current difference. Additionally, voltage and current references [8] are supplied for system biasing.

B. Stress Sensing Front-End Interface

Fig. 3 shows the proposed differential readout partitioned into analog and digital sections. When normal stress is applied, currents in the PMOS stress element pair (I_1/I_2 and I_3/I_4) vary in opposite directions. The NMOS CM then replicates this

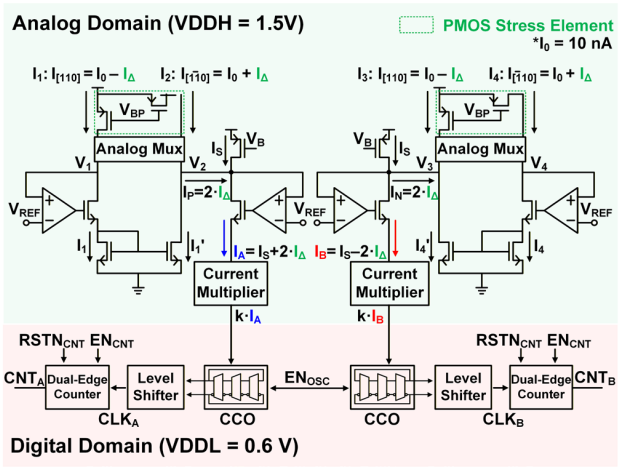


Fig. 3. Detailed circuit of the proposed stress sensor interface integrating PMOS sensors and an NMOS CM interface with sourcing current (I_S) into a current multiplier and a current-to-digital converter.

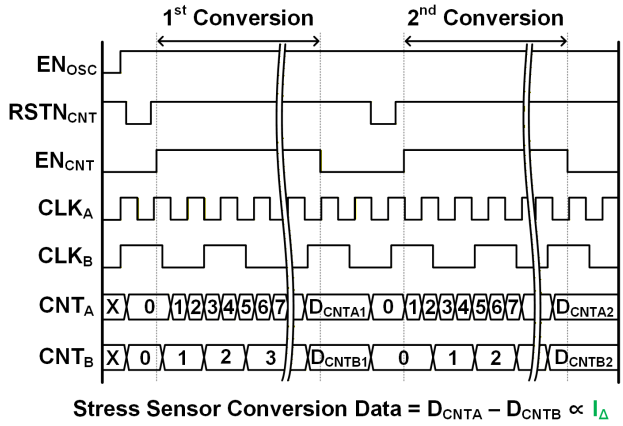


Fig. 4. Timing diagram of the conversion process for the stress sensor using a differential frequency-to-digital converter.

differential current (I_1' and I_4'), producing twice the stress-induced current difference ($2I_\Delta$) at I_P and I_N. However, a significant current imbalance due to large stress—e.g., when I_1 and I_3 are much larger than I_2 and I_4 with large positive I_Δ—can lower the voltages at nodes V_2 and V_3, degrading NMOS mirror operation and restricting dynamic range. To mitigate this, a sourcing current (I_S) is injected at V_2 and V_3 to sustain the node voltages, ensuring proper mirror functionality under large current differences, thereby extending the dynamic range.

In addition, I_S introduces a DC offset that enables measurement of negative I_Δ by preventing output clipping at zero. I_S is set to approximately half the base current (I_0) to ensure the CM functions effectively across the full stress range. The resulting output currents (I_A, I_B) are digitized through a 3-stage CCO [9] and asynchronous dual-edge counters. Under zero-stress conditions (current multiplier factor k = 1), the CCO operates at a nominal frequency of 54.4 kHz. This circuit is optimized for ultra-low-power operation, with each current path (I_1–I_4) biased at I_0 = 10 nA.

Since stress proportionally affects current, significant stress causes an increase or decrease in current of I_1–I_4. To guarantee stable operation, four voltage regulators maintain constant voltage at the $V_{1\text{-}4}$ nodes (Fig. 3), ensuring a fixed V_{DS} for sensor elements. These regulators employ four amplifiers with combined power consumption of < 1 nW.

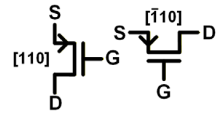
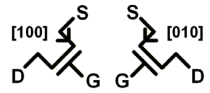
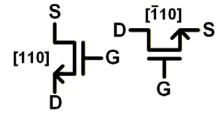
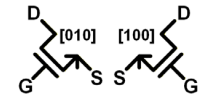
Type	Orthogonal Layout	Diagonal Layout
PMOS	 - Normal Stress Sensitive - Shear Stress Insensitive - For PMOS Sensor	 - Normal Stress Insensitive - Shear Stress Less-Sensitive - For Peripheral Circuits
NMOS	 - Normal Stress Less-Sensitive - Shear Stress Insensitive - For Peripheral Circuits	 - Normal Stress Insensitive - Shear Stress Sensitive - For NMOS Sensor

Fig. 5. Dependence of normal and shear stress sensitivities on crystallographic orientations for PMOS and NMOS devices.

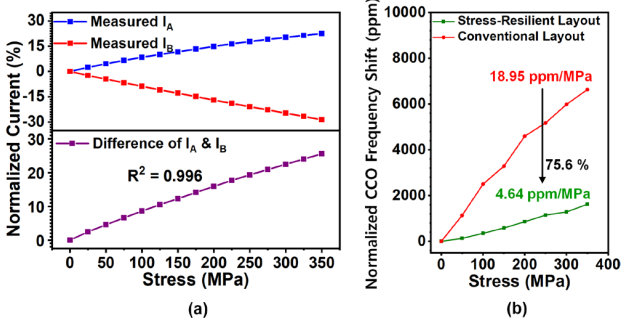


Fig. 6. (a) Measured results of the sensor interface output current excluding digital domain (b) Measured layout-dependent oscillator frequency variation.

C. Readout Operation and Digitization

The timing diagram in Fig. 4 shows the digital operation. An EN_{OSC} signal activates CCOs to generate clocks (CLK_A and CLK_B) proportional to currents ($k \cdot I_A$ and $k \cdot I_B$). Dual-edge counters, gated by EN_{CNT} and $RSTN_{CNT}$ signals, produce outputs CNT_A and CNT_B. The code difference (CNT_A - CNT_B) is linearly proportional to the applied stress. The conversion time, set by the pulse width of the EN_{CNT}, determines the measurement sensitivity. Consequently, the dynamic range is less constrained by the readout interface, and sensitivity can be dynamically tuned via conversion time, providing programmable sensitivity across the entire stress range to accommodate diverse application requirements.

D. Stress-Resilient Layout and Front-End Verification

One of the challenges in stress sensor interface design is ensuring that peripheral circuits remain unaffected by the mechanical stress being measured. Fig. 5 illustrates the stress dependence of CMOS devices under different layout orientations. To mitigate this effect, the peripheral circuits employ a stress-resilient layout strategy using orthogonal NMOS and diagonal PMOS devices, applied to all non-sensing blocks to reduce errors caused by mechanical stress.

Fig. 6 summarizes the silicon verification of both the sensing front-end and the layout strategy. The normalized differential outputs I_A and I_B and their difference show linearity with R^2 = 0.996, confirming the front-end performance (Fig. 6 (a)). The stress-resilient layout reduces CCO frequency variation under applied normal stress by 75.6% compared to a conventional layout with all MOSFETs aligned along the [110] direction (Fig. 6 (b)).

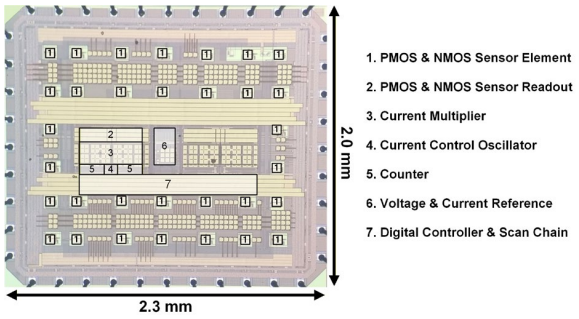


Fig. 7. Die micrograph.

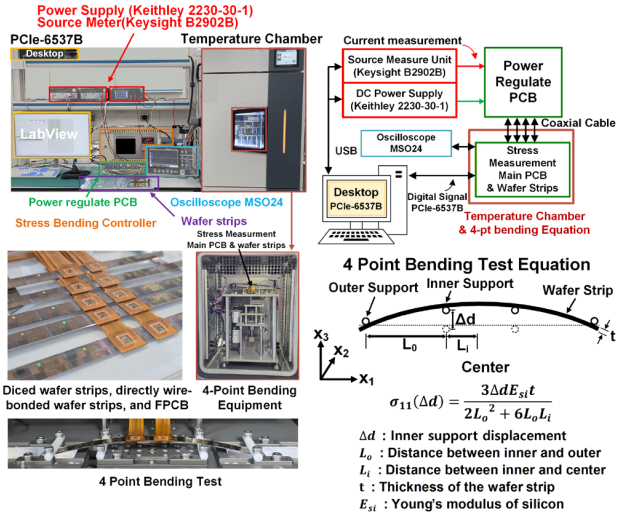


Fig. 8. Overall measurement setup showing the 4-point bending system and diced wafer strips for the stress measurement.

III. Measurement Results and Comparison

The stress sensor interface was fabricated in a 180 nm process, operating at 1.5 V (0.6 V digital). Fig. 7 shows the die micrograph with the sensor array and peripheral circuit. The measurement setup (Fig. 8) uses a 4-point bending system, where diced wafer strips are wire-bonded to a Flex-PCB to apply normal stress (σ_{11}-σ_{22}). Such a setup only provides normal stress, precluding any shear components, hence the proposed interface has been mechanically characterized exclusively under normal stress.

As shown in Fig. 9(a), the system achieves linearity comparable to a stand-alone MOSFET sensor, measured at 5 MPa intervals over a range of 0-375 MPa. Fig. 9(b) shows the measured resolution as a function of the current multiplier factor (k) and conversion time without stress. The sensitivity can be enhanced by increasing either k or the conversion time. The resolution converges to approximately 0.2 MPa (1σ) once the sensitivity surpasses a threshold, irrespective of which parameter is adjusted. In this work, k is fixed at 4 to maintain low-power operation, as a higher k increases current multiplication and thus power consumption, and the sensitivity is controlled by varying the conversion time. Fig. 10 illustrates the relationship between sensitivity and resolution, measured across a sensitivity range of 8.9-889.6 kPa/LSB under 0-300 MPa, showing the ability to tune sensitivity with conversion time without incurring a significant trade-off with resolution. Notably, with longer conversion times, the resolution is bounded by a 1/f noise floor of approximately 0.2 MPa. As shown in Fig. 11, the measured inaccuracy across 10 chips from 2 wafers was ±0.28 MPa (3σ) after a 2-point calibration (50, 250 MPa) and removing systematic nonlinearity.

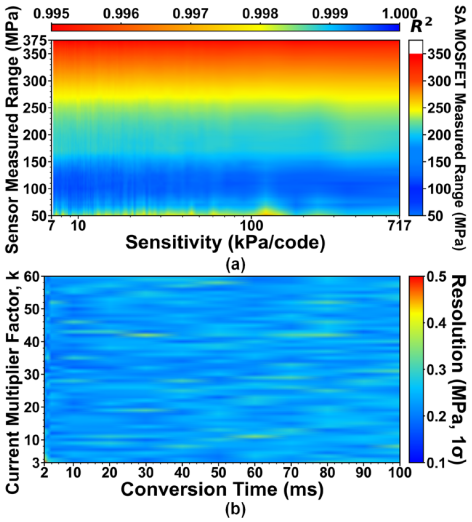


Fig. 9. Measurement results of (a) system linearity comparable to a stand-alone reference sensor and (b) resolution (1σ) based on conversion time versus current multiplier factor k.

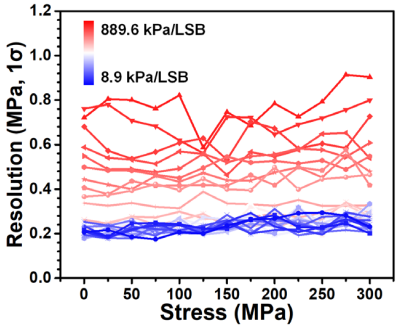


Fig. 10. Measurement result of resolution (1σ) across the sensitivity range tuned via conversion time.

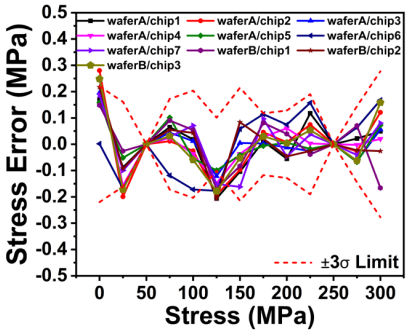


Fig. 11. Measurement result of inaccuracy across 10 chips from 2 wafers after 2-point calibration (50 and 250 MPa).

Fig. 12 shows the stability of the stress sensor interface under varying temperature and supply conditions. Measured across 0-80°C, the sensor interface exhibits a stable coefficient (α) of +0.003/K (Fig. 12(a)). After 2-point calibration, the temperature-induced error was -0.71 / +0.66 MPa with no stress applied. The maximum supply-induced error (Fig. 12(b)) is -1.4/+1.4 MPa over 1.4-1.6 V supply range across 0-300 MPa without use of LDO regulation, which could further reduce this error. Fig. 12(c) shows the sensor's stability, with consistent measurements under repeated normal stress. Fig. 13 details the power distribution across the analog sensing front-end, current-to-digital converter, and reference circuits within the total 225.6 nW power consumption.

Table I summarizes the performance of this work and compares it with prior designs. This work successfully

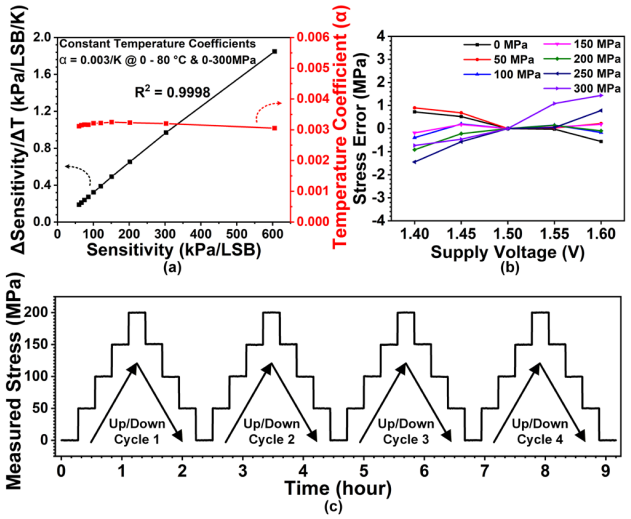


Fig. 12. Measurement results of (a) temperature coefficient, (b) supply error, and (c) measured stress over repeated up/down bending cycles.

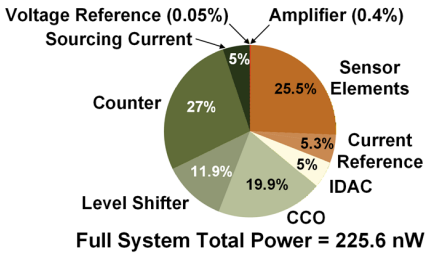


Fig. 13. System power breakdown.

overcomes the trade-off between sensitivity and dynamic range of conventional interfaces. It operates at an ultra-low power consumption of 225.6 nW with an energy per conversion as low as 0.68 nJ, translating to the best Resolution FoM of 0.05 nJ·MPa². Notably, even at a sensitivity similar to the finest region of prior art (11 kPa/LSB), the interface maintains a state-of-the-art Resolution FoM of 0.48 nJ·MPa², demonstrating top-tier performance across all sensitivity settings. Furthermore, unlike prior works restricted to single-die verification, the extensive multi-die and multi-wafer measurements reported herein thoroughly validate the reliability and robustness of the proposed architecture.

IV. Conclusion

Conventional voltage-domain stress sensor interfaces suffer from an inherent trade-off between sensitivity and dynamic range, limiting their use in energy-constrained IoT systems. In this paper, we presented a time-domain sensor interface that encodes stress-induced currents into frequency via a CCO, decoupling sensitivity from dynamic range and enabling programmable sensitivity through digital accumulation time. Fabricated in a 180 nm CMOS process, the sensor consumes only 225.6 nW and achieves a resolution FoM of 0.05 nJ·MPa². These results represent a 15× FoM improvement and over three orders of magnitude power reduction compared to state-of-the-art implementations. Comprehensive multi-die measurements across 10 chips from two distinct wafers confirm the reliability of the proposed architecture. The proposed design provides a high-precision, ultra-low-power stress sensing solution well-suited for industrial automation and energy-constrained IoT sensor nodes.

Table I. Performance summary and comparison with state-of-the-art

	This Work			ISSCC 2023 K. Allinger [7]	JSSC 2020 U. Nurmetov [10]	JSSC 2016 Y. Mahsereci [4]	JSSC 2013 M. Kuhl [11]
Process	180nm CMOS			180nm CMOS	130nm CMOS	500nm CMOS	350nm CMOS
Sensor Type	32 piezoresistive FET			32 piezoresistive FET	7 n- and p-doped resistors	2 piezoresistive FET	24 piezoresistive FET
Readout Principle	Frequency to Digital Converter			Current Mirror based SAR	ΣΔ ADC	Current Mirror based SAR ADC	Adaptive DDA Gain SAR ADC
Supply Voltage (V)	1.5 / 0.6			-	-	4	3.3
Power (W)	225.6 n			1.28 m[b]	357 µ	1.5 m	1.75 m
Stress Range (MPa)	-375 – 375[a]			-365 – 365[a]	-100 – 360	-200 – 400	-390 – 390 (0 – 100)[c]
Conversion Time (s)	0.5 m	3 m	40m	44.6 µ / 125 µ	65 µ	20.5 µ	15.2 m
Energy/Conversion (J)	0.11 n	0.68 n	9.03n	56.9 n / 160n	23.3 n	30.7 n	26.5 µ
Sensitivity (kPa/LSB)	890	148.8	11.1	178	175	600	11
Resolution (MPa, 1σ)	1.02[d]	0.27[d]	0.23[d]	0.58[e] / 0.22[e]	0.18[f]	-	-
Resolution FoM (J·MPa²)	0.12 n	0.05 n	0.48 n	19.14 n / 7.74 n	0.76 n	-	-
Inaccuracy (MPa, 3σ)	± 0.28 (10 chips from 2 wafers)			-	-	-	-
Temperature (°C)	0 – 80			15 – 50	5 – 90	20 – 40	-
Temperature Error (MPa)	-0.71/+0.66[g]			-	-3.5/+0.875[g]	-	-
Supply Error (MPa)	-1.4/+1.4			-	-	-	-

a : limited stress range by wafer stripe broken b : including SPI c : calculated based on ADC reolustion & sensitivity
d : averaged value over 0 - 300 MPa stress range e : estimated from the measurement graph
f : calculated based on sensitivity & resolution(code) g : with no stress applied over temperature
* Resolution FoM = Energy Conversion × Resolution² - : Not Reported

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