A Compact D-Band LNA Achieving 8.6-dB/Stage Gain and 7.35-dB NF Enabled by Complex Embedding Network in 28-nm CMOS

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***Abstract*—This paper presents a highly compact and gain-efficient D-band low-noise amplifier (LNA) in 28-nm bulk CMOS. To overcome the severe intrinsic gain degradation of transistors at sub-THz frequencies, which typically forces bulky multi-stage cascaded designs, a novel complex embedding network (CEN) featuring a hybrid transmission line (TL) and cross-coupled capacitor (C_c) topology is presented. The proposed TL-based CEN topology approaches the theoretical maximum power gain (G_{max}) near the stability boundary while maintaining a low port impedance, significantly facilitating broadband inter-stage matching and noise suppression. The fabricated differential 2-stage LNA achieves a peak gain of 17.2 dB with a 3-dB bandwidth of 17 GHz (123–140 GHz). Consuming 22 mW of DC power, the LNA demonstrates a minimum noise figure (NF) of 7.35 dB. Notably, occupying an ultra-compact core area of only 0.041 mm², the proposed design achieves a record-high single-stage gain of 8.6 dB and the smallest footprint among the reported state-of-the-art D-band CMOS LNAs.**

***Keywords*—*D-Band, complex embedding network, high gain, area-efficient, low noise amplifier*.**

I. Introduction

The escalating demand for high-throughput data rates in emerging applications such as 6G wireless communications, high-resolution imaging, and advanced radar systems has driven the exploration of higher frequency spectra. The sub-terahertz (sub-THz) regime, particularly the D-band (110-170 GHz), offers outstanding bandwidth advantages that can potentially support over 100 Gbps data transmission, addressing the ever-growing need for faster wireless connectivity, making it a promising candidate for next-generation communication systems [1].

However, the transition to D-band frequencies introduces significant technical challenges that impede practical implementation [2]. A primary bottleneck lies in the fundamental limitations of transistors at these frequencies, where transistors exhibit substantially reduced intrinsic gain due to severe parasitic effects. To meet the stringent signal-to-noise ratio (SNR) requirements amidst pronounced atmospheric path loss, conventional D-band low noise amplifiers (LNAs) are typically forced to adopt bulky 4- or 5-stage cascaded architectures. This inevitably incurs substantial power overhead and excessively large footprints, which strictly limit their practical integration into multi-channel and large-scale phased arrays.

To address this gain insufficiency, embedding network techniques have emerged as a crucial research focus [3], [4].

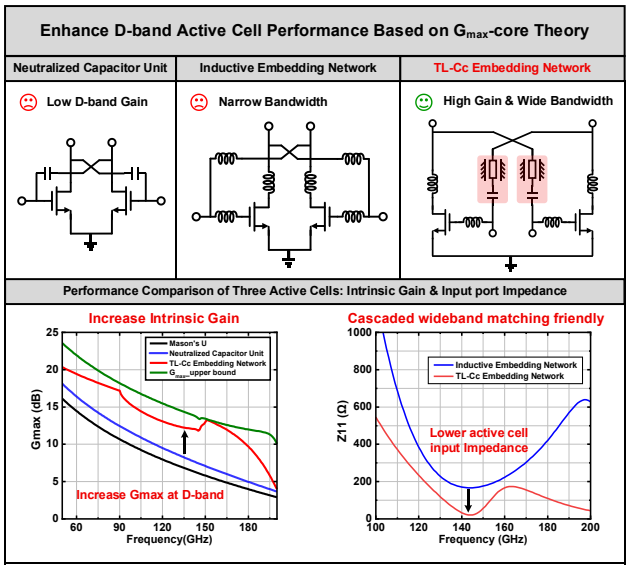

Fig. 1. The active cells in D-band circuits and the proposed TL-Cc Embedding network structure.

While the conventional neutralized differential capacitor pair (NDP) is widely used, its gain-boosting capability significantly deteriorates at D-band, leaving a substantial gap to the upper bound of the maximum power gain, as shown in Fig. 1. Alternatively, applying pure inductive embedding in [5] can track the upper bound, however, it inherently results in an excessively high port impedance and high-Q resonances. This severe impedance mismatch greatly restricts broadband cascaded designs, as the parasitic losses in inter-stage matching networks often counteract the boosted gain.

In this work, a complex embedding network (CEN) comprising transmission lines (TLs) and cross-coupled capacitors (C_c) to realize high gain and low port impedance. is proposed. By synthesizing a high-order feedback mechanism, the TL-based CEN approaches the stability boundary to enhance G_{max} while dramatically lowering the port impedance for favorable broadband matching. The proposed differential LNA utilizes only two stages to achieve a single-stage gain of 8.6 dB (17.2 dB in total) and a 17-GHz bandwidth. Consequently, the LNA achieves a competitive 7.35-dB minimum noise figure (NF) while occupying an ultra-compact core area of only 0.041 mm², demonstrating state-of-the-art area and gain efficiency.

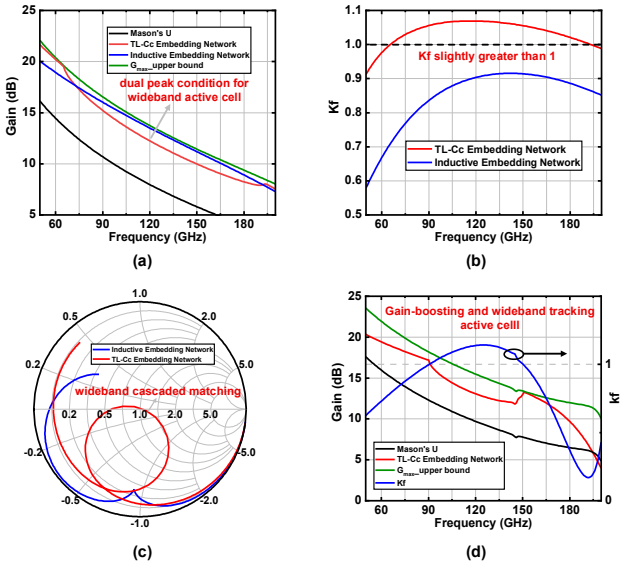

Fig. 2. Operating conditions and performance comparisons of the TL-Cc embedding network and conventional inductive embedding network.

II. Circuit Design

A. Complex TL-Cc Embedding Network Active Cell Design

Fig. 1 depicts the D-band active cell designs based on the embedding network theory. The active cell based on the NDP is currently the predominant structure in system designs. Nevertheless, at D-band frequencies, more complex electromagnetic parasitic effects significantly degrade its gain, intensifying front-end design challenges. To enable efficient D-band active cell design, embedding network technology has garnered substantial research interest [10], [11], [12]. Through carefully designed embedding networks, the transistor's G_{max} can approach its theoretical upper limit (U as Mason's Unilateral power gain) [6]:

$$\max\{G_{max}\}=(2U-1)+2\sqrt{U(U-1)} \quad (1)$$

As shown in Fig. 1, the inductive embedding network is a reported effective gain-boosting implementation based on the embedding network theory. However, due to its extreme instability design and simplistic inductive embedding structure, this architecture results in port impedance as high as several hundred ohms when approaching the theoretical gain limit, which severely restricts broadband cascaded design at D-band. To achieve effective gain enhancement while maintaining favorable broadband impedance characteristics, this paper introduces an active cell based on a TL-Cc embedding network.

Fig. 2 compares the implementation conditions and performance of the inductive embedding network and the TL-Cc embedding network. As shown in Fig. 2 (a), the TL-Cc embedding network exhibits a dual-peak gain tracking curve, demonstrating the higher-order characteristics of our design compared to the inductive embedding network. As derived from the G_{max} realization condition [6], a stability factor $K_f = 1$ defines the boundary for achieving maximum G_{max}. Fig. 2 (b) compares the K_f characteristics of the two structures. The conventional inductive embedding network operates in the unstable region with $K_f < 1$, indicating strong potential oscillation tendencies and inherently high port impedance. In contrast, through higher-order feedback network design, the TL-Cc embedding network maintains its K_f at the stability boundary (K_f slightly above 1), ensuring high gain performance while avoiding excessively high port impedance characteristics. To illustrate the effect of port impedance, we compare the matching trajectory for the inductive embedding network and the TL-Cc embedding network when they are configured as a cascaded design. As shown in Fig. 2 (c), the high-order TL-Cc feedback structure exhibits the broadband matching characteristics compared with the narrow matching result of the inductive feedback structure. Fig. 2 (d) presents the post-simulation of power gain and K_f curves adopting the TL-Cc embedding network. The condition $K_f = 1$ defines the upper and lower boundaries for broadband realization, while the region where K_f is slightly greater than 1 constitutes the target gain-boosting region for this work.

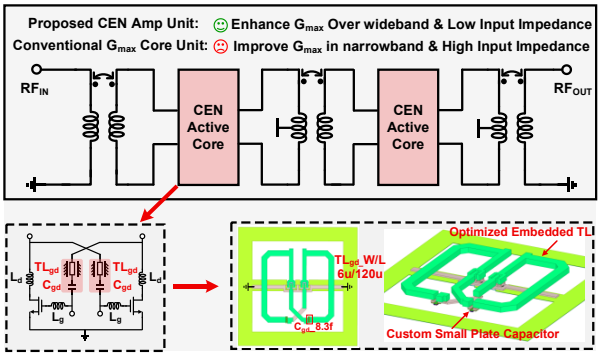

Fig. 3. Proposed two-stage LNA using a complex TL-Cc embedding network structure.

B. D-band LNA Design Implementation

Fig. 3 presents the schematic of the proposed two-stage LNA employing the TL-based CEN structure. To achieve the high gain and low port impedance design, the feedback of the active unit is realized using a combination of transmission lines and capacitors. The layout of the TL-based CEN is depicted in Fig. 3, comprising customized cross-coupled transmission lines and capacitors between the gate and drain, along with small inductors at the gate and drain terminals, collectively forming the CEN unit. As shown in Fig. 4 (a) and (b), the TL and capacitor design effectively pushes the operating point of the active unit toward the K_f instability boundary to optimize the single-stage G_{max}.

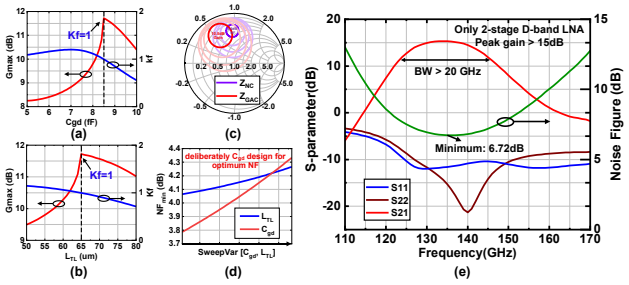

Fig. 4. CEN parameters simulation: (a) C_{gd} vs G_{max}, K_f, (b) L_{TL} vs G_{max}, K_f, (c) gain and noise contours, (d) L_{TL} and C_{gd} vs NF, (e) cascaded simulation results.

To achieve optimal noise performance, the impact of the embedding TL and C_c on the NF of the active cell was investigated alongside their effects on G_{max}. As depicted in Fig. 4(d), the NF exhibits a significantly higher sensitivity to C_c variations than to the TL dimensions. Consequently, the cross-coupled capacitors are deliberately implemented using a metal-stacked parallel-plate topology to facilitate precise capacitance tuning. Furthermore, a meandered routing strategy is adopted for the embedding TLs, which not only compacts the active core footprint but also mitigates unwanted electromagnetic coupling with the adjacent gate and drain inductors. To ensure rigorous design accuracy, the surrounding ground wall of the active unit and the thick-metal (M8) source-to-ground connections are comprehensively incorporated into the 3-D electromagnetic (EM) simulations to account for parasitic effects.

The noise and gain matching of the single-stage active unit are illustrated in Fig. 4 (c). Thanks to the TL-based CEN, the single-stage active unit achieves simultaneous matching with 10.5 dB gain and 4.5 dB NF_{min}, validating the CEN's efficacy in substantially boosting the D-band single-stage gain while suppressing noise degradation. Beyond maximizing single-stage gain performance, the designed CEN lowers the port impedance, thereby alleviating the severe inter-stage matching bottlenecks typically encountered in broadband cascaded designs. As shown in Fig. 4 (e), the simulated input return loss (S_{11}) achieves a matching bandwidth exceeding 45 GHz, and the small-signal gain (S_{21}) bandwidth surpasses 20 GHz. The two-stage cascaded gain exceeds 15 dB, with a simulated noise figure of 6.72 dB, demonstrating a highly competitive D-band LNA with noise, bandwidth, and gain efficiency.

III. Measurement Results

The proposed two-stage D-band LNA is fabricated in a 28 nm bulk CMOS process. As shown in Fig. 5, the LNA occupies a core area of 0.351 mm × 0.117 mm. The LNA comprises three transformer-based passive matching networks and two active amplifying units using the TL-based CEN. The small-signal S-parameter measurement setup is shown in Fig. 6 (a). A vector network analyzer and two D-band VNA extenders are

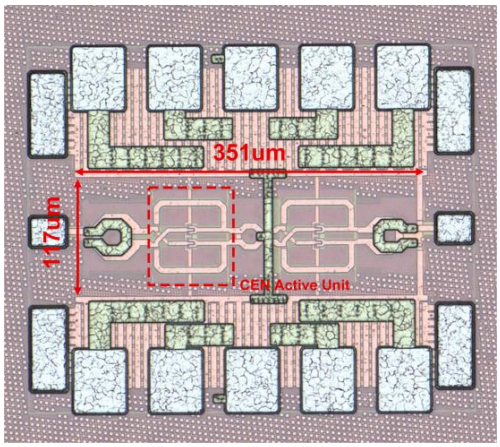

Fig. 5. Chip micrograph of the proposed LNA.

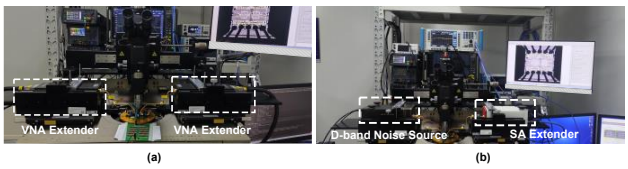

Fig. 6. Measurement setup for (a) small signal test and (b) noise figure test.

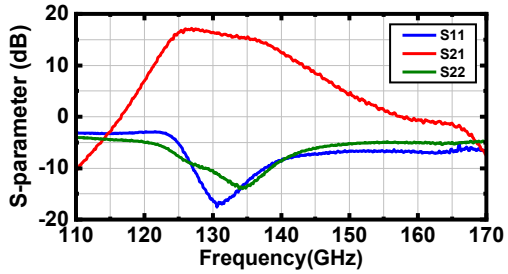

Fig. 7. Measured small-signal S-parameters.

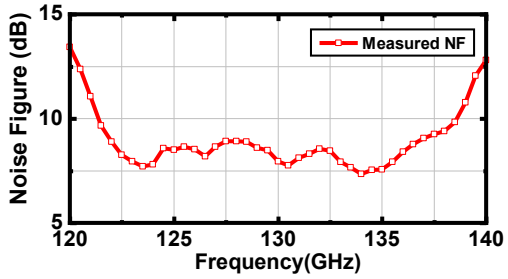

Fig. 8. Measured NF of the proposed LNA.

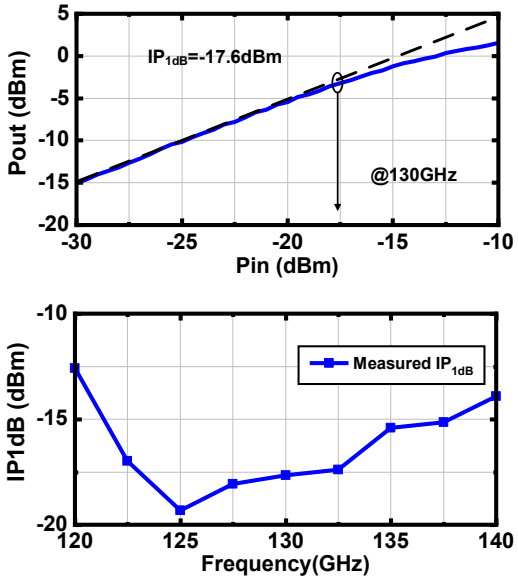

Fig. 9. Measured IP_{1dB} of the proposed LNA.

Table 1. Performance summary and comparison with prior LNAs.

	This work	RFIC'24 [3]	JSSC'24 [4]	IMS'23 [7]	MWTL'23 [8]	IMS'22 [9]
Topology	**Differential 2-stage CS**	Single-ended 3-stage CS	S2D 4-stage CS	Differential 5-stage CS	Single-ended 5-stage CE	Differential 4-stage CS
Process	**28 nm CMOS**	40 nm CMOS	40 nm CMOS	40 nm CMOS	90 nm SiGe BiCMOS	22 nm FDSOI CMOS
Frequency (GHz)	**130**	140	150.2	134.8	139.8	153.5
Peak Gain (dB)	**17.2**	18.4	20.0	19.7	26.5	18.0
Gain/stage (dB)	**8.6**	6.13	5	3.94	5.3	4.5
BW (GHz)/(%)	**17/13.1**	16.5/11.8	18.8/12.5	24/17.8	37.6/26.9	10.8/7
NF_{min} (dB)	**7.35**	6.52	4.9	7.9	7.2	7.5*
IP_{1dB} (dBm)	**-17.6**	-16.7	-22.4	-24.8	-31	-17
P_{DC} (mW)	**22**	17.1	19.6	17.8	20.6	27.5
Core Area (mm^2)	**0.041**	0.057	0.22	0.07	0.25^	0.094

*Simulation results ^Estimated from reported chip photo

used. The chip is characterized on a probe station by probing with waveguide GSG probes at D-band. The measured small-signal S-parameters of the proposed two-stage LNA are shown in Fig. 7. The LNA achieves a 17.2 dB peak gain with a 3-dB bandwidth of 17 GHz (123-140 GHz). Benefiting from the TL-based CEN structure in the active units, the two-stage differential D-band LNA achieves a power gain of 17.2 dB, corresponding to a per-stage gain of 8.6 dB. It should be noted that this per-stage gain includes the insertion loss of the passive matching networks. With a reasonable estimation of 1.5 dB for this passive matching loss, the actual gain of the active amplifying unit exceeds 10 dB, effectively demonstrating the capability of the TL-based CEN structure to enhance the power gain of D-band active units. It is also worth noting that the discrepancy between the small-signal measurement results and the simulated results in Fig. 4 (e) is mainly caused by inaccuracies in transistor modeling and imperfections in the passive EM simulation environment.

The D-band LNA noise measurement setup is shown in Fig. 6 (b). The noise characterization was performed using the Y-factor method, with the test setup comprising a D-band noise source and a signal spectrum analyzer with a frequency extension module. The minimum measured in-band NF of 7.35 dB, as shown in Fig. 8, is slightly higher than the simulated minimum of 6.72dB. The large-signal continuous-wave measurement results are shown in Fig. 9. The measured IP_{1dB} of the proposed LNA is -17.6 dBm at 130 GHz. The measured IP_{1dB} versus frequency curve exhibits that the best IP_{1dB} is -13.9 dBm.

Table 1 summarizes the performance of the proposed LNA and compares it with recent state-of-the-art D-band works. Notably, the proposed LNA exhibits the highest single-stage power gain and occupies the smallest core area among the reported designs. Enabled by the superior per-stage gain and favorable broadband matching characteristics of the designed CEN structure, the front-end attains a substantial cascaded gain utilizing fewer amplifying stages. Consequently, the proposed LNA achieves a highly competitive noise figure, bandwidth, and linearity, while drastically reducing the overall footprint.

IV. Conclusion

This paper presents a high-gain, area-efficient D-band LNA leveraging a novel complex embedding network (CEN). By integrating customized transmission lines and cross-coupled capacitors, the TL-based CEN enables the active core to operate near the stability boundary. This approach delicately resolves the fundamental trade-off between tracking the theoretical G_{max} upper bound and maintaining a manageable port impedance for broadband cascaded matching. Implemented in a 2-stage differential architecture with transformer-based matching networks, the fabricated LNA achieves a 17.2-dB total gain, a 17-GHz bandwidth, and a minimum NF of 7.35 dB. Notably, it delivers a record-high per-stage power gain of 8.6 dB among state-of-the-art CMOS LNAs. Finally, this remarkable stage-reduction methodology yields an ultra-compact circuit footprint, making the proposed LNA highly compelling for integration in the large-scale sub-THz phased-array systems.

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