A 1.25-mW 10.3–14.3-GHz Area-Efficient Dual-Mode Oscillator using Asymmetric Nested Transformers Achieving −216.4-dB $\text{FOM}_{\text{TA@1MHz}}$

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***Abstract*—We propose an area-efficient, dual-core, dual-mode oscillator featuring an asymmetric nested transformer architecture. By embedding an 8-shaped auto-transformer within a primary outer auto-transformer, the design merges two distinct cores into a single, highly compact passive network. The orthogonal nature of the 8-shaped inner geometry minimizes magnetic coupling to the outer coil, preserving the overall Q-factor and effectively eliminating mode ambiguity. Consequently, the proposed topology achieves dual-mode, series-resonance-assisted inverse-class-D operation without expanding beyond the footprint of a standard single inductor. Measurement results demonstrate an FOM of 192.4 dB at a 10 MHz offset, maintaining stable performance with only 2.8 dB FOM variation across a 32.7% tuning range. Consuming <1.25 mW, the proposed oscillator also exhibits high immunity to supply-induced spurs and achieves a low flicker phase-noise corner of 100–350 kHz.**

***Index Terms*—Ultra-low power, oscillator, class-D^{-1}, single footprint, dual-mode, tuning range, supply pushing.**

I. Introduction

Wide-tuning-range (WTR) oscillators operating at very low power are essential for emerging multi-standard communication and high-precision ultra-wideband (UWB) sensing. However, simultaneously achieving WTR, low power, and low phase noise (PN) above 10 GHz in CMOS remains challenging, since highly efficient oscillators typically rely on large inductors whose peak quality (Q) factor occurs at lower frequencies.

To improve power efficiency, [1] proposed the inverse-class-D oscillator, which achieves ultra-low power consumption. However, it suffers from inferior PN, limited tuning range, elevated flicker noise, and strong supply sensitivity (see Fig. 1(a)), making it unsuitable for modern WTR systems. Extending it to a dual-core architecture improves PN, but at the cost of significant area overhead. To mitigate the flicker PN and supply sensitivity issues of class-D^{-1} oscillators, [2] introduced a series-resonance-assisted class-D^{-1} topology that improves the effective tank Q-factor while shielding the resonator from supply variations (see Fig. 1(b)). Nevertheless, its achievable TR remains severely limited, constraining its applicability in wideband and multi-standard systems.

Conversely, several WTR oscillators have been reported [3]–[6], most of which rely on multi-mode and/or multi-core architectures. Although effective at extending the TR, these approaches incur substantial area and power overhead. Furthermore, conventional multi-mode oscillators typically operate in class-B, leading to reduced current efficiency and increased sensitivity to supply noise. Moreover, they often require complex harmonic-tuning networks to suppress flicker-noise upconversion, further increasing silicon area. As a result, such architectures are ill-suited for low-power area-constrained wideband applications.

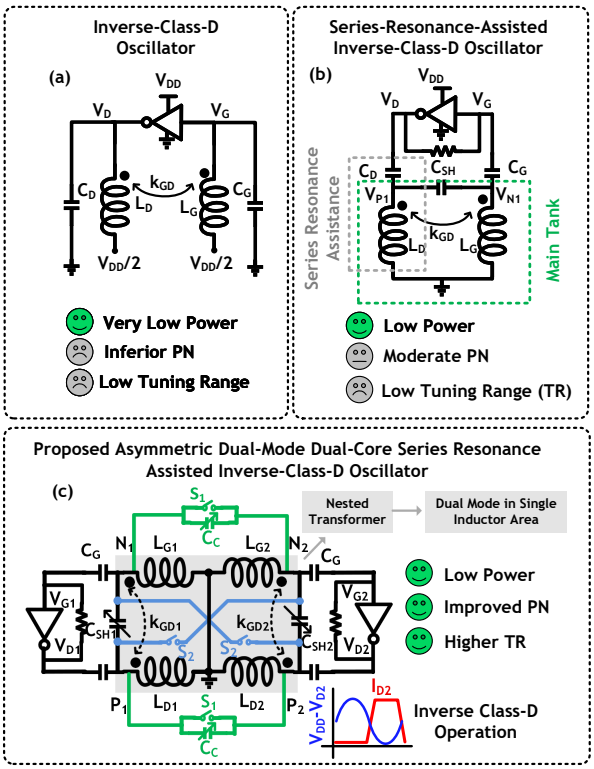

Fig. 1. Conceptual diagrams of (a) class-D^{-1} [1], (b) series-resonance-assisted class-D^{-1} [2], and (c) the proposed compact dual-mode class-D^{-1} oscillator employing asymmetric nested transformers.

To address these challenges, we propose in Fig. 1(c) a highly energy/area-efficient oscillator with an extended TR based on an *asymmetric* dual-core, series-resonance-assisted class-D^{-1} architecture. By implicitly nesting an 8-shaped transformer within a primary outer transformer, and linking the two cores via a passive capacitive coupling network, the design avoids the severe area penalties of traditional dual-core systems.

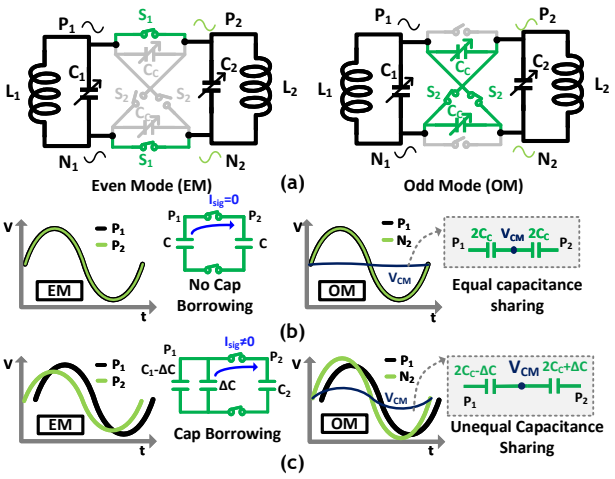

Fig. 2. (a) Equivalent circuits of a generic dual-core oscillator in odd/even modes, corresponding waveforms and equivalent tank capacitance of (b) symmetric ($L_1 = L_2$ and $C_1 = C_2$), and (c) asymmetric oscillator cores.

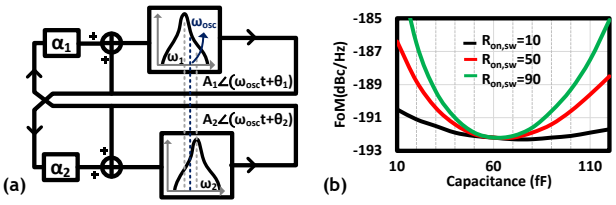

Fig. 3. (a) Simplified diagram of the proposed asymmetric dual-core oscillator, and (b) simulated FOM of the proposed oscillator ($L_1 = L_2 = 800$ pH) across different C_1 (with C_2=60 fF) for various switch on-resistances.

II. Proposed Oscillator Design

A. Operating Principle

Fig. 2(a) shows a generic capacitively coupled dual-core oscillator in its equivalent even/odd-mode circuit representations. In the even mode, switch S_1 is enabled, locking the two cores to the common oscillation frequency, while the coupling capacitor C_C is bypassed. Conversely, in the odd mode, S_1 is off while S_2 is on, so C_C becomes part of the resonant network and lowers the oscillation frequency. As shown in Fig. 2(b), the transient waveforms remain phase-aligned in such *symmetrical* dual-core, dual-mode oscillators. However, duplicating two well-matched resonant tanks incurs a substantial area penalty.

Using *nested* inductors mitigates this area penalty, but introduces an inherent *asymmetry* between the two core frequencies. Although such a mismatch has been analyzed in injection-locked oscillators [7], its extension to dual-mode operation has received limited attention. As illustrated in Fig. 2(c), in the even-mode, this asymmetry introduces an inter-core phase difference, causing signal current to flow through the coupling switch. Consequently, the higher frequency core "borrows" capacitance from the lower-frequency core. In the odd mode, the same phase difference disrupts the virtual ground at the midpoint of C_C, resulting in unequal capacitance sharing. Through this dynamic capacitance redistribution, the two core frequencies are nearly equalized and get injection locked thereafter. From the equivalent model in Fig. 3(a), the resulting phase difference ($\theta_1 - \theta_2$), and synchronized oscillation frequency $\omega_{\rm osc}$ for two cores with quality factors $Q_{1,2}$, nearly equal natural frequencies $\omega_{1,2}$, injected-voltage feedback factors $\alpha_{1/2}$ ($\approx$ 1 here), and oscillation amplitudes $A_{1/2}$ ($\approx V_{\rm DD}$), can be expressed as:

$$\theta_2 - \theta_1 = \sin^{-1}\left(\frac{\omega_2 - \omega_1}{\frac{\omega_1\alpha_1 A_2}{2Q_1A_1} + \frac{\omega_2\alpha_2 A_1}{2Q_2A_2}}\right) \quad (1)$$

$$\omega_{\rm osc} = \omega_1 + \frac{\omega_1\alpha_1 A_2}{2Q_1A_1}\sin(\theta_2 - \theta_1) \quad (2)$$

where, the natural frequencies are defined as $\omega_{1|\rm even} = 1/\sqrt{L_1(C_1 - \Delta C)}$, $\omega_{2|\rm even} = 1/\sqrt{L_2(C_2 + \Delta C)}$ for the even mode, and $\omega_{1|\rm odd} = 1/\sqrt{L_{1,2}(C_1 + 2C_C - \Delta C)}$, $\omega_{2|\rm odd} = 1/\sqrt{L_2(C_2 + 2C_C + \Delta C)}$ for the odd mode.

Despite the inherent frequency mismatch, the proposed oscillator still achieves a ~3 dB PN improvement, comparable to a symmetrical dual-core design. This is because capacitance borrowing in even mode and unequal sharing in odd mode only marginally alter the overall tank Q-factors at the newly established synchronized frequency ω_{osc}. Consequently, the equivalent tank impedance in both modes can be approximated as $R_1||R_2 \approx \min(R_1, R_2)/2 + \Delta R/4$, where R_1 and R_2 are the effective impedance of the individual tanks at ω_1 and ω_2, and $\Delta R = |R_1 - R_2|$. When ΔR is sufficiently small, the overall effective impedance approaches $R/2$, mirroring the symmetrical case. Importantly, the coupling on-resistance ($R_{\rm on,sw}$) is also critical. As shown in Fig. 3(b), a lower $R_{\rm on,sw}$ is preferred, as it ensures a minimal phase shift between the cores (e.g., <10° for $R_{\rm on,sw}$=10 Ω), leading to negligible performance degradation even with significant capacitance mismatch.

The dual-core oscillator is realized using an 8-shaped coil nested inside a 2-turn outer coil. This specific geometry deliberately minimizes the electromagnetic coupling between the inner and outer coils, effectively eliminating mode ambiguity while enabling full inductor area sharing. As a result, the proposed oscillator maintains low PN despite the intentional geometric and inductive asymmetry.

B. Implementation Details

The proposed dual-mode class-D^{-1} operation requires two transformers, which are implemented using a nested structure of a two-turn outer inductor and a two-turn 8-shaped, center-tapped inner inductor. As illustrated in Fig. 4, this arrangement also forms an auto-transformer, which enhances the Q-factor of both coils. Because of the physical asymmetry between the coils, the ideal resonance condition ($L_2/L_1 \neq C_1/C_2$) does not apply. Instead, the optimal inductance/capacitance ratio is dependent on the individual tank Q-factors and their peak frequencies. Post-layout simulations therefore indicate that for $L_1/L_2 \approx 1.16$, the optimum performance is achieved with $C_{\rm SH2}/C_{\rm SH1} \approx 1.5$. To suppress 2$^{\rm nd}$-harmonic current at the differential nodes, ground-isolating resistors are inserted

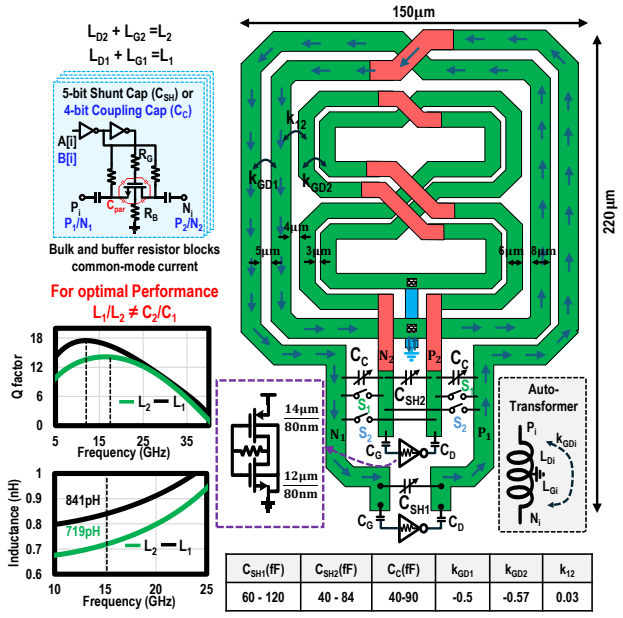

Fig. 4. Implementation of the proposed oscillator using asymmetric nested transformers, including simulated inductance and Q factors of each coil.

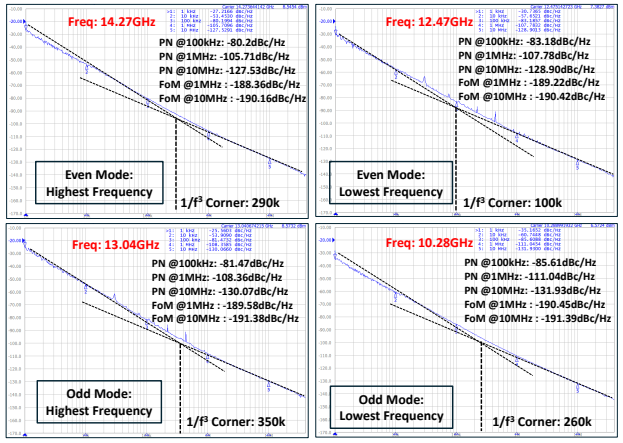

Fig. 5. Measured PN characteristics at the highest and lowest oscillation frequencies in the even (top) and odd (bottom) modes.

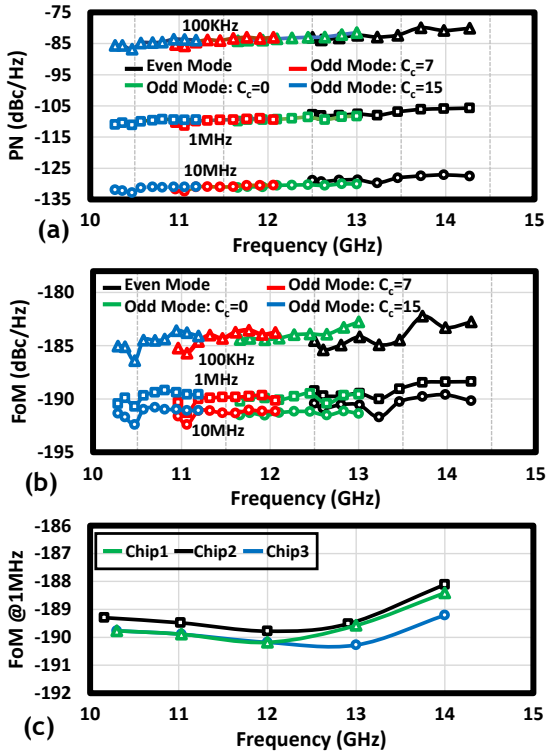

Fig. 6. Summary of measured (a) PN, and (b) FOM, along with (c) FOM measured across three different chips over the TR.

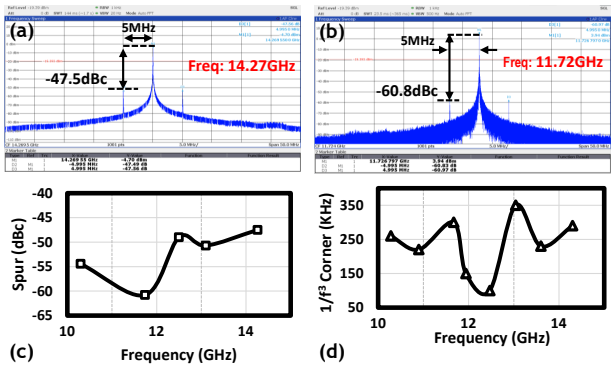

Fig. 7. Measured supply-induced spurs due to a 100-mV_{pp} 5-MHz sinusoidal perturbation at the (a) highest, and (b) lowest oscillation frequency, (c) spur across TR, and (d) measured flicker-noise corner across TR.

at both the local bulk of the capacitor switches (R_B) and the inverter outputs (R_G) (see Fig. 4(top-left). Combined with the use of longer-channel devices, this technique mitigates the flicker PN upconversion without additional harmonic-tuning networks. Furthermore, as illustrated in Fig. 1, supply-dependent capacitances (e.g., C_{gs}) primarily modulate higher-order poles rather than the fundamental pole [2]. This significantly reduces supply sensitivity, which is an important attribute for practical multi-core oscillators.

III. Experimental Results

The proposed imbalanced dual-core, dual-mode oscillator was fabricated in GlobalFoundries 22 nm FDSOI CMOS. As shown in the chip micrograph in Fig. 8, the nested two-transformer layout enables a highly compact core area of only 0.033 mm^2. Fig. 5 presents the measured PN at the lowest and highest oscillation frequencies in both even and odd modes. Power consumption remains consistent across

TABLE I
COMPARISON TABLE OF THE STATE-OF-THE-ART LOW-POWER AND MULTI-MODE OSCILLATORS.

	H. Guo ISSCC' 19	M. Fang RFIC' 22	K. Xu VLSI' 23	S. Kumar RFIC'25	H. Guo ISSCC'25	Y. Li RFIC'25	H. Ge ISSCC' 24	Q. Wu JSCC' 24	This Work
Technology	65nm CMOS	40nm CMOS SOI	28nm CMOS	28nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS	**22nm FDSOI**
Architecture	Low-Power Parallel Resonance				Multi-Mode Parallel Resonance				**Dual-Mode Inverse-class D**
Supply (V)	0.48	0.3	0.58	0.6	0.6	0.3/0.4	0.4 to 0.55	0.8	**0.9**
Power (mW)	3.8 to 4	1.4 to 1.6	0.64 to 0.67	0.58	9.6 to 24.9	4.5 to 13	2 to 8.8	5.6 to 14.8	**1.1 to 1.26**
Area (mm^2)	0.08	0.153	0.043	0.026	0.14	0.13	0.14	0.1	**0.033**
No. of Modes	1	1	1	1	2	2	4	2	**2**
Freq (GHz)	25.48 – 29.92 (16%)	12.1 – 14.94 (21%)	7.82 – 9.38 (18.1%)	13.8 – 16.2 (16%)	9.05 – 18.5 (68.6%)	4.54 – 8.7 (62.8%)	13.7 – 41.5 (101%)	8.9 – 21.9 (84.4%)	**10.3 – 14.3 (32.7%)**
PN @100KHz (dBc/Hz)	-87 to -90.5	N/A	-68.4 to -75.1*	-71.7 to -74.3*	-100 to -90*	-103.2 to -95.1	-86.2 to -69.4*	-93 to -85.9*	**-86.8 to -80.8**
PN @1MHz (dBc/Hz)	-112.3 to -115.3	-88 to -105.6*	-98.6 to -103.5	-98 to -99.7	-126 to -118.6	-125.9 to -120.1*	-112 to -98	-118 to -115	**-111.3 to -105.7**
PN @10MHz (dBc/Hz)	-130.8 to -134	-108 to -131.8	-112.7 to -127.1	-118 to -121	-147 to -139.6	-146.9 to -141.3	-133.2 to -124.4	-138.6 to -131.1	**-132.8 to -127.1**
FoM @100KHz (dBc/Hz)	-184.5 to -186.8	N/A	-171.4 to -175.2	-177.4 to 182.2	-187.4 to -182.7	-188.3 to -184	-187 to -169.4	-185 to -169.6	**-186.4 to -182.2**
FoM @1MHz (dBc/Hz)	-189.8 to -191.6	-168* to -187.6	-179.8 to -183.6	-183.7 to -185.6	-193.4 to -191.3	-190.5 to -187*	-193 to -178	-190 to -178.7	**-191.3 to -188.4**
FoM @10MHz (dBc/Hz)	-188.2 to -190.3	-168* to -193.8	-184 to -187	-185.1 to -188.4	-194.4 to -192.3	-191.5 to -188.2	-194 to -184.4	-190.5 to -184.8	**-192.4 to -189.6**
FoM_T @1MHz (dBc/Hz)	-193.9 to 195.7	-174.4 to-194	-184.9 to – 188.7	-187.7 to -189.7	-210.2 to -208.1	-206.6 to -202.9	-213 to -198	-208.5 to -197.2	**-201.6 to -198.7**
FoM_A @1MHz (dBc/Hz)	-200.8 to -202.6	-159.8 to -179.4	-193.5 to -197.3	-199.5 to -201.4	-202.9 to -200.8	-200.4 to -197.1	-201.5 to -186.5	-200 to -188.7	**-206.1 to -203.2**
FoM_{TA} @100KHz (dBc/Hz)	-199.5 to -201.8	N/A	-186 to -194	-197.3 to 202.13	-213.6 to -208.9	-212.1 to -207.7	-215.7 to -197.9	-213.5 to -198.1	**-211.5 to -207.3**
FoM_{TA} @1MHz (dBc/Hz)$	-204.8 to -206.6	-182.6 to -202.2	-198.6 to -202.4	-203.6 to -205.5	-219.6 to -217.5	216.5 to 213	-221.t to -207.2	-218.5 to -207.2	**-216.4 to -213.6**
$1/f^3$ Corner (KHz)	130 to 230	>1000	600	200 to 400	170 to 700	70 to 250	>1000	>1000	**100 - 350**
Supply Induced Spur**	N/A	N/A	N/A	N/A$	N/A	N/A	N/A	N/A	**-60 to -47**

$FoM = PN + 20\log\left(\frac{\Delta f}{f_{osc}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right)$ $FoM_T = FoM - 20\log\left(\frac{TR}{10}\right)$ $FoM_A = |FoM| - 10\log\left(\frac{Area}{1\,mm^2}\right)$ *Taken from graphs **100mV peak – to – peak supply disturbance $$K_{vdd}$ is 50MHz/V. Spur measurement not shown.

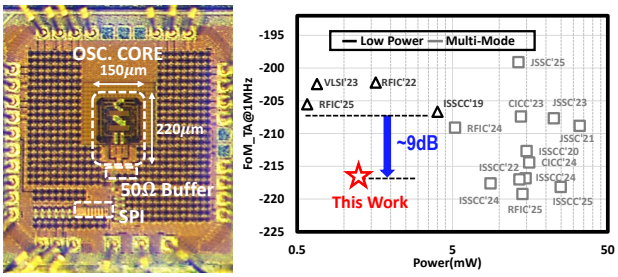

Fig. 8. Chip micrograph and benchmarking of the proposed oscillator against the state-of-the-art low-power and multi-mode oscillators.

operating modes, measuring 1.10–1.12 mW in the even mode and 1.20–1.25 mW in the odd mode. This minimal mode dependence contrasts sharply with conventional multi-mode oscillators, which typically exhibit pronounced power variation across modes [3]–[5].

Fig. 6 summarizes the oscillator's performance across the entire TR. The peak figure-of-merit (FOM) reaches –186.4, –191.3, and –192.4 dB at 100-kHz, 1 MHz, and 10 MHz offsets, respectively, while the worst-case values are –182.2, –188.4, and –189.6 dB. This indicates a tightly bound FOM variation of ∼3 dB at both 1 MHz and 10 MHz offsets. Fig. 6(c) further confirms consistent performance across three fabricated chips. To assess supply pushing, an exaggerated 100-mV_{pp} sinusoidal disturbance was applied to the supply. From Fig. 7, spur levels of –47 dBc and -60 dBc were measured with 5 MHz offset at the highest and lowest oscillation frequencies, respectively. Across the TR, the flicker-noise corner varies from 100 kHz to 350 kHz, demonstrating competitive performance with state-of-the-art low-flicker oscillators employing harmonic-tuning techniques [8].

Table I compares the proposed oscillator against state-of-the-art low-power and multi-mode designs. Owing to its compact nested-transformer architecture, the proposed design achieves a minimal core area of 0.033 mm^2, <1.25 mW power, low flicker PN, a stable FOM across operating modes, and the widest TR among low-power oscillators. Additionally, it achieves the highest FOM_{TA} within its category while remaining highly competitive with multi-mode designs, as highlighted in Fig. 8 (right).

IV. CONCLUSION

This paper introduces a low-power, capacitively coupled dual-core inverse-class-D oscillator employing an asymmetric nested transformer, thereby enabling dual-mode operation within a single-inductor footprint. Operating from 10.3–14.3 GHz, it consumes 1.25 mW and achieves the highest reported FOM_{TA} among low-power >10 GHz oscillators. With a 100 kHz flicker-noise corner and low supply-induced spurs, it is well suited for wideband multi-standard applications.

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