A 113.7dB-DR BW/Power Scalable Sensor Readout IC with a 1600× Scaling Range and a Dynamic-Filtering Bootstrapped Switch

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***Abstract*—This paper presents the first reported bandwidth (BW)/power scalable sensor readout IC (ROIC), which consists of a programmable gain amplifier (PGA), a discrete-time (DT) ΔΣ modulator (ΔΣM), and a dynamic bandgap reference (BGR), achieving a 1600× scaling range. To mitigate noise folding due to sampling, a bootstrapped switch with an embedded anti-aliasing filter is proposed, yielding up to 37% noise power suppression across the entire scaling range. Fabricated in a 180-nm CMOS process, the proposed fully scalable ROIC achieves a dynamic range of 113.7 dB, a minimum input-referred noise of 1.4 μVrms, and a gain error of ±0.27% from -40°C to 125°C.**

***Keywords*—bandwidth/power scalable, readout IC, anti-aliasing filter, bootstrapped switch, frequency-controlled current source.**

I. Introduction

The evolving IoT and wearable device markets require versatile sensor interfaces to handle diverse sensor signals with widely varying BWs (sub-10 Hz to kHz) and amplitudes (μV to V). To maintain high energy efficiency across such disparate scenarios, BW/power scalable [1], [2] sensor ROICs are desired. This allows IP reuse across different products, resulting in more agile design.

To adapt to different input amplitudes, a sensor ROIC usually consists of a PGA, an ADC, and a BGR (Fig. 1(a)). Although BW/power scalable DT ADCs have been reported [2], [3], conventional PGAs and BGRs typically consume constant static power, limiting the overall system scalability [4], [5]. Moreover, to drive the DT ADC, the BW of the PGA should be much larger than the ADC's sampling frequency (f_S), resulting in significant noise folding (Fig. 1(b)). Inserting a dynamic RC filter can alleviate this issue [6], but the fixed cutoff frequency (f_{CUT}) is incompatible with the scalable f_S. Although the floating-inverter amplifier (FIA) leverages its intrinsic dynamic BW to suppress noise folding [7], it suffers from limited PVT robustness.

To address these challenges, this work proposes a sensor ROIC employing a cascoded frequency-controlled current source (FCCS) and a dynamic-filtering bootstrapped (BST) switch. This architecture not only enables global BW/power scalability but also ensures stable anti-aliasing and settling performance, achieving a 1600× scaling range.

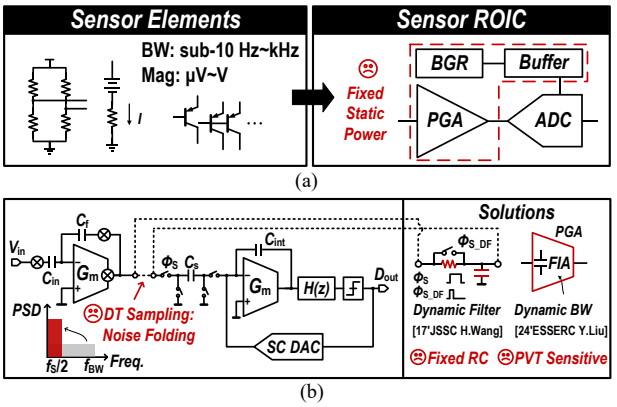

Fig. 1. (a) Typical ROIC architecture. (b) Prior art of ROICs with anti-aliasing techniques.

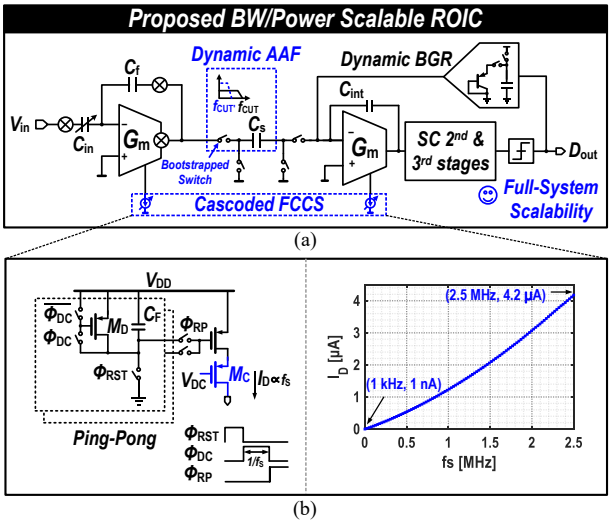

Fig. 2. (a) Proposed BW/power scalable ROIC. (b) Topology and simulation results of the cascoded FCCS.

II. Proposed BW/Power Scalable ROIC

A. Proposed ROIC Enabled by a Cascoded FCCS

Fig. 2(a) shows the block diagram of this work, comprising a PGA, a DT ΔΣM, and a dynamic BGR. Instead of using FIAs [7], [8], more stable statically biased amplifiers are adopted in the PGA and DT ΔΣM. To achieve BW/power scalability, a capacitively biased diode (CBD)-based FCCS is employed to provide the global bias current [9]. As shown in Fig. 2(b), the pre-charged capacitor C_F is discharged through the diode-connected MOSFET M_D. By setting the discharge duration to $1/f_S$, a bias current I_D proportional to f_S is obtained, which is then mirrored to other blocks. Compared to [9], a cascode MOSFET M_C is added to boost the output impedance, reducing the supply sensitivity. The ping-pong operation is retained from [9] to ensure continuous bias generation. Thanks to the cascoded FCCS, the global bias current scales linearly with f_S, achieving a >2000× scaling range in simulation.

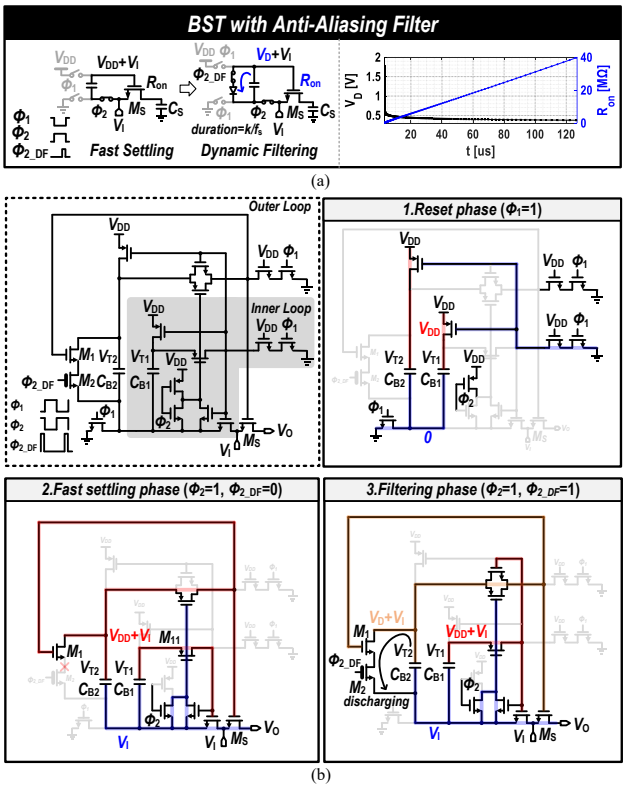

Fig. 3. (a) Principle and (b) circuit implementation of the proposed BST with AAF.

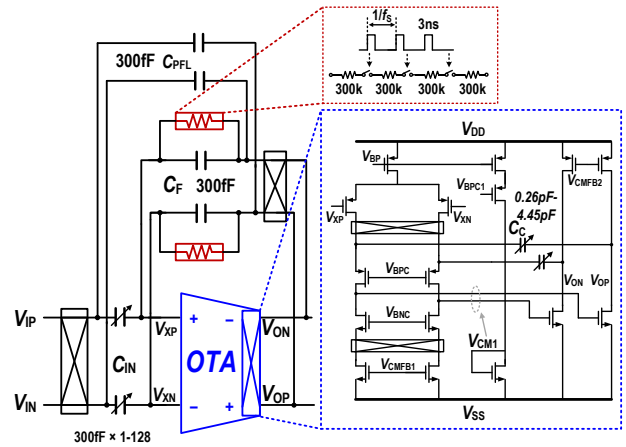

Fig. 4. Circuit implementation of the PGA.

B. Bootstrapped Switch with Embedded AAF

To mitigate the noise folding between the PGA and DT ΔΣM, a BST switch with an embedded dynamic anti-aliasing filter (AAF) is proposed (Fig. 3(a)). At the beginning of the sampling phase (Φ_2=1), the sampling switch M_S is configured as the conventional BST switch, with its gate voltage boosted to $V_{DD}+V_I$ to achieve a signal-independent R_{ON}. This ensures fast settling with low distortion. After settling, the switch M_S is driven by a dynamic gate voltage (V_D+V_I), where V_D is generated by the CBD circuit and is proportional to ln(1/t) (t is the discharge duration) [10]. As V_D decays, M_S enters the sub-threshold region rapidly, where its R_{ON} increases approximately linearly with t (Fig. 3(a)). By defining the discharge duration $t=k/f_S$, the resulting R_{ON} of M_S scales with $1/f_S$. Together with the subsequent sampling

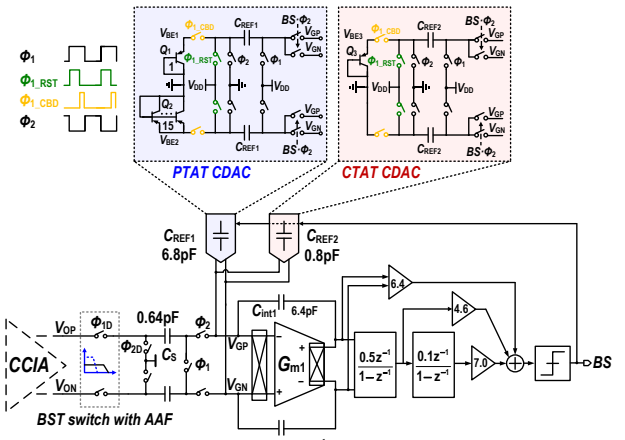

Fig. 5. Circuit implementation of the 3rd-order 1-bit DT ΔΣM and embedded dynamic BGR.

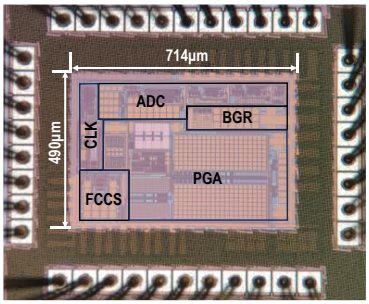

Fig. 6. Die micrograph.

capacitor C_S (0.64 pF), an AAF with a scalable f_{CUT} is realized. To balance linearity and noise suppression, k is set to ~0.125. As illustrated in Fig. 3(b), the proposed BST switch employs a dual-loop architecture. The inner loop provides the basic timing signals and PMOS biasing as the conventional BST switch [11], while the outer loop generates the frequency-controlled V_D for M_S. It has three operation phases: Reset (Φ_1=1): $C_{B1/2}$ are pre-charged while M_S is held off. Fast-Settling (Φ_2=1, Φ_{2_DF}=0): The top-plate voltages $V_{T1,2}$ of $C_{B1,2}$ are boosted to $V_{DD}+V_I$. Filtering (Φ_2=1, Φ_{2_DF}=1): After settling, the thick-oxide device M_2 is activated by a boosted clock Φ_{2_DF} to discharge C_{B2} through the diode-connected M_1, generating the frequency-controlled V_D (=$V_{GS,M1}$) for the sampling switch M_S.

C. CCIA-Based Programmable Gain Amplifier

The PGA is implemented as a capacitively-coupled chopper instrumentation amplifier (CCIA) (Fig. 4). To extend the DR, its gain is 3-bit programmable (C_{IN} =1–128×C_F, C_F=300fF). To suppress flicker noise and offset, nested chopping (at f_S/4 and f_S/128) is employed [12]. The OTA is implemented as a two-stage amplifier with a telescopic-cascode 1st stage and a common-source 2nd stage to provide a >100dB open-loop gain. As in [13], an area-efficient duty-cycled resistor (R=4×300kΩ, on-time≈3ns) is placed across the input and output of the OTA to define the input DC bias and reduce the chopping ripple. To ensure loop stability over the wide f_S scaling range, Ahuja compensation [14] is adopted instead of conventional Miller compensation, as the latter requires a nulling resistor that cannot scale with f_S. Moreover, the compensation capacitor C_C (0.26pF to 4.45pF) scales inversely with C_{IN}, stabilizing the closed-loop BW across different gains while maintaining loop stability. To boost the input impedance, a positive feedback loop (C_{PFL}=C_F) is adopted [15].

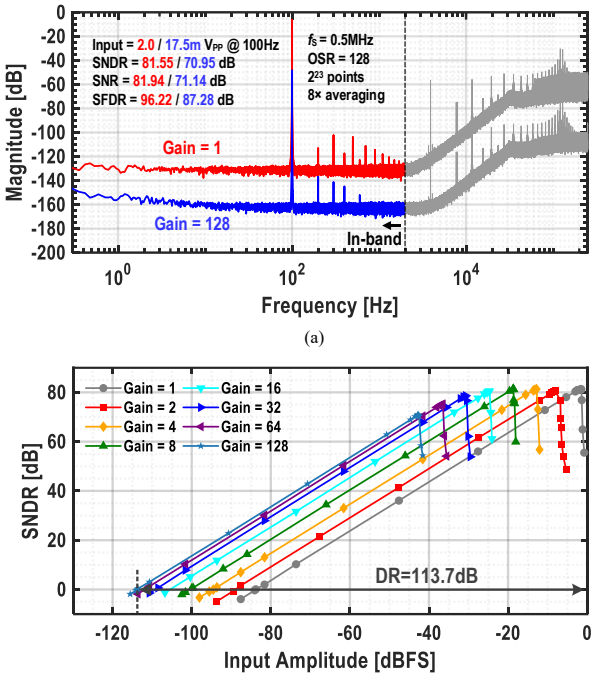

Fig. 7. (a) Measured spectra at gain=1/128 and (b) DRs across PGA gains (1–128) at f_S =0.5MHz.

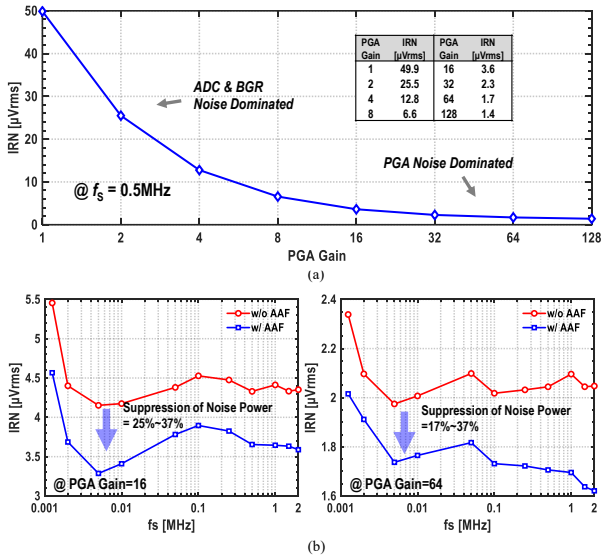

Fig. 8. Measured IRN vs. (a) PGA gain; (b) f_S with and without AAF at gain=16/64.

D. DT ΔΣM and Embedded Dynamic BGR

The PGA output is digitized by a 3rd-order 1-bit CIFF DT ΔΣM (Fig. 5). To achieve BW/power scalability, a CBD-based dynamic BGR is embedded within the ΔΣM [1]. It consists of a PTAT and a CTAT DAC, where C_{REF1} (6.8 pF) and C_{REF2} (0.8 pF) discharge through diode-connected PNPs $Q_{1,2}$ (1:15) and Q_3 to produce ΔV_{BE} and V_{BE}, respectively. As in [1], the discharge duration is controlled by an on-chip RC delay circuit, effectively decoupling these reference voltages from the scalable f_S. They are then directly summed within the first integrator of the ΔΣM. Thanks to the preceding PGA gain, the kT/C noise contributed by both the ΔΣM and the BGR can be effectively suppressed.

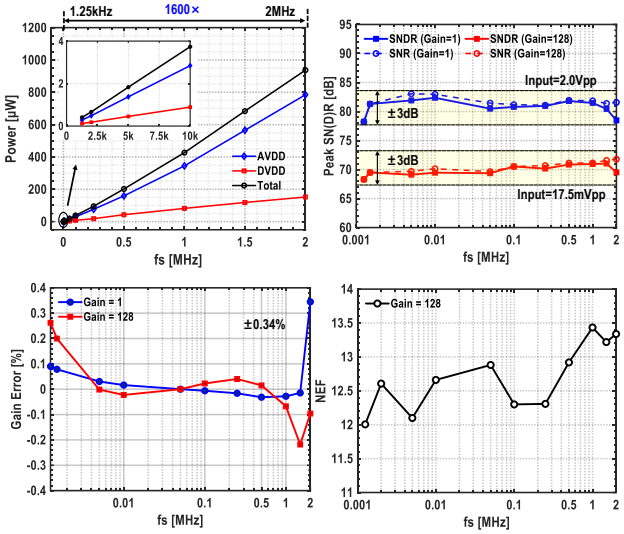

Fig. 9. Measured power consumption, peak SNDR, gain error, and NEF vs. f_S.

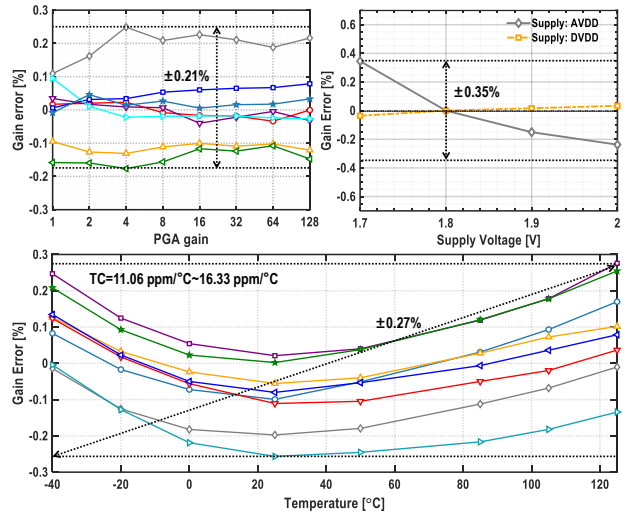

Fig. 10. Measured gain errors of eight samples across PGA gains and temperatures, and gain variation across supply voltages.

III. Measurement Results

The prototype is fabricated in a 180-nm CMOS process with an active area of 0.35mm^2 (Fig. 6). Operating at a typical f_S of 0.5MHz, the ROIC achieves an SNDR of 81.55dB (2V$_{PP}$ input, gain=1) and 70.95dB (17.5mV$_{PP}$ input, gain=128), respectively (Fig. 7(a)). Measured across different PGA gains (1–128), it achieves a DR of 113.7 dB (Fig. 7(b)).

At low gains, the input-referred noise (IRN) is dominated by the ΔΣM and the BGR, while their IRN contribution is effectively suppressed at high gains, achieving a minimum IRN of 1.4μVrms (Gain=128) (Fig. 8(a)). With the proposed dynamic AAF, the noise power can be suppressed by 17% to 37% across a 1600× f_S scaling range (Fig. 8(b)).

As shown in Fig. 9, within this scaling range, the ROIC maintains a stable SNDR (Δ<±3dB) and a gain variation <±0.34%, while exhibiting linear scaling in power consumption. This leads to a stable NEF of ~12.7 across the entire frequency range.

To verify the robustness, eight samples were evaluated across different gains (1–128) and temperatures (-40°C to

125°C), as shown in Fig. 10. After a simple batch-calibration, they demonstrate gain errors of <±0.21% at room temperature and <±0.27% over temperatures. The measured temperature coefficients (TCs) range from 11.06 to 16.33 ppm/°C. Under supply variations (1.7V–2.0V), the measured gain variation is less than ±0.35%.

Table I summarizes the performance of this work and compares it with the state-of-the-art designs. To the best of the authors' knowledge, this is the first reported fully scalable ROIC integrating PGA, ADC, and BGR. It shows stable performance over a 1600× scaling range and achieves a 113.7-dB DR.

TABLE I. COMPARISON WITH THE STATE OF THE ART

	This work	**ISSCC'24 [1]**	**ESSERC'24 [7]**	**JSSC'22 [4]**
Architecture	**CCIA+ DTΔΣM + VREF**	DTΔΣM + VREF	CC(FIA)-DTΔΣM	PGA+ CTΔΣM
Tech. [nm]	**180**	130	22	180
Supply [V]	**1.8**	1.2	1.8/0.9	1.2/0.8
Area [mm²]	**0.35**	0.20	0.038	0.72
BW/Power Scalable	**Yes**	Yes	Yes	No
Include Reference	**Yes**	Yes	No	No
Gain Range	**1-128 (8 steps)**	N.A.	20	1, 8-256 (7 steps)
Input Range	**17.5mV$_{PP}$ (G*=128) / 2.0V$_{PP}$ (G=1)**	2.4V$_{PP}$	128mV$_{PP}$	8mV$_{PP}$ (G=256) / 1.6V$_{PP}$ (G=1)
f_S[Hz]	**1.25k-2M (1600×)**	25k-1.5M (60×)	1M-5M (5×)	1.92M
BW [Hz]	**4.9-7.8k**	98-5.9k	3.9k-19.5k	5k
Power [μW]	**0.4-937**	1.7-50.8	64-265	13.6
IRN [μVrms]	**1.4 (G=128)/ 49.9 (G=1)[a]**	46.8	2.6	6.1 (G=256)
NEF	**12 (f_S=1.25k)/ 12.9 (f_S=50k)/ 13.3 (f_S=2M)[b]**	157.7	9.3[c]	9.5 (G=256)[c]
DR [dB]	**113.7**	87.1	84.9	99.5
TC [ppm/°C] (-40°C-125°C)	**11-16 (0-pt)**	16-29 (0-pt)	N.A.	N.A.
Inaccuracy (-40°C-125°C)	**±0.27% (0-pt)**	±0.26% (0-pt)	N.A.	N.A.

* G denotes the PGA gain; [a] measured at f_S=0.5MHz, OSR=128; [b] measured at G=128; [c] Not include VREF generator.

CONCLUSION

Targeting sensor signals with variable bandwidths and amplitudes, this paper presents a fully bandwidth/power scalable ROIC with a high dynamic range. The proposed ROIC comprises a PGA, a DT ΔΣM, and a dynamic BGR. To enable global power scalability, a cascoded frequency-controlled current source is employed to provide static bias currents that scale linearly with the sampling frequency f_S. Furthermore, a bootstrapped switch with an embedded dynamic anti-aliasing filter is proposed. Its cutoff frequency tracks f_S linearly, ensuring stable anti-aliasing and settling performance across the entire scaling range. Fabricated in a 180-nm CMOS process, the proposed ROIC demonstrates robust operation over a 1600× scaling range and achieves a 113.7-dB DR, making it suitable for diverse sensing applications.

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