Bias and Temperature Behavior of 1/f Noise and RTN in MOSFETs with Edge Conduction Effects

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***Abstract*—This work focuses on the study of edge conduction effects on low-frequency noise (LFN) in MOSFETs, through the analysis of 1/f noise and random telegraph noise (RTN). The role of the edge transistor on the degradation of LFN in the subthreshold region and at lower temperatures is made evident using bias and temperature measurements on different layouts. The resulting noise is shown to still be predicted in the context of the carrier number fluctuations model, provided that a parasitic edge transistor is included. The results highlight the need for realistic modeling of 1/f noise and RTN at different bias and temperature conditions, and they show the enhancement in terms of noise level enabled by an optimized, hump-free layout. These findings provide practical guidelines for both compact modeling and low-noise layout design in CMOS analog technologies.**

***Index Terms*—1/f noise, RTN, Temperature, Edge conduction**

I. Introduction

In low-noise applications such as high-precision sensors and MEMS, low-frequency noise (LFN) is a major concern in MOSFETs used in analog circuits. Particular attention is given to the level and variability of $1/f$ noise, as well as to the presence of random telegraph noise (RTN), since both severely affect the performance of the circuit. On top of the quality of the silicon/oxide interface, it has been previously shown that the layout design of the device plays a significant role in the noise [1], [2]. The latter can notably be paired with the presence of parasitic conduction at the edges of the transistor, along the shallow trench isolation (STI). This leads to the appearance of a 'hump' in the I_d-V_g characteristic of the transistor due to the creation of two additional transistors in parallel with the intrinsic one, of smaller width and lower threshold voltage (V_t), degrading its mismatch performance [3]. Transistors suffering from edge conduction also show more prominent hump effect in low temperature condition, due to a weaker effect of temperature on its V_t and subthreshold slope. Yet, there is limited evidence on how edge conduction influences LFN, especially with temperature. Hence, realistic modeling is needed to correctly assess the behavior of LFN and RTN impacted or not by edge conduction effects, including the influence of geometry, bias, and temperature.

To investigate both the layout and modeling aspects, statistical analyses of $1/f$ noise and RTN have been carried out on NMOS transistors of two different layouts. First, the impact of the parasitic edge transistor on $1/f$ noise is investigated, followed by a statistical study at different temperatures. Then, the effects of edge conduction mechanisms on the level of RTN are probed and modeled.

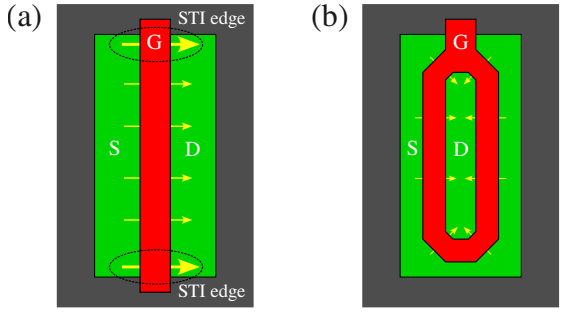

Fig. 1. Top-view layout schematic of (a) the standard layout transistor, and (b) the octagonal layout transistor (not put to scale). The standard layout suffers from parasitic STI edge conduction.

II. Experimental Details

The study focuses on thick oxide NMOS transistors issued from a 90 nm CMOS analog technology, of width W = 10 µm and length L = 0.5 µm. Two different transistor layouts were considered, illustrated in Fig. 1: a standard monofinger layout and an 'octagonal' transistor, as described in [4]. The latter was initially designed to improve mismatch performance due to being immune to the hump effect, thanks to the channel not having any edges shared with the STI.

Frequency and time domain drain current noise measurements were performed using the NOISYS equipment [5], with the transistors biased in linear regime (V_d = 0.1 V). Statistical samples between 50 and 200 transistors were measured depending on the conditions. The following analyses were undertaken for different fixed drain current values (varying V_g), and three temperatures: -40°C, 25°C and 125°C.

III. Results and Discussion

A. 1/f noise and STI edge conduction

First observations can be made on the DC characteristics of the devices at 25°C, where Fig. 2a and 2c show the I_d-V_g curves of 50 transistors for the standard layout and the octagonal layout respectively. The first shows some increased dispersion in the subthreshold region, yet more meaningful results are observed on the g_m/I_d curves in Fig. 2b and 2d. Clear evidence of the hump effect can be seen on the standard

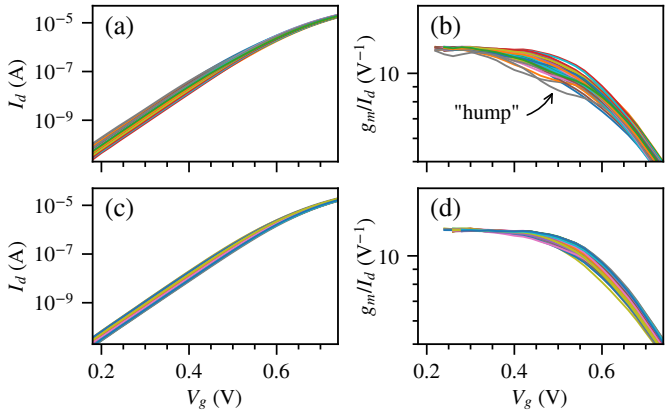

Fig. 2. Electrical characteristics in terms of I_d versus V_g and g_m/I_d versus V_g respectively, for (a) and (b): the standard layout NMOS transistors, and (c) and (d): the octagonal layout NMOS transistors, at T = 25°C.

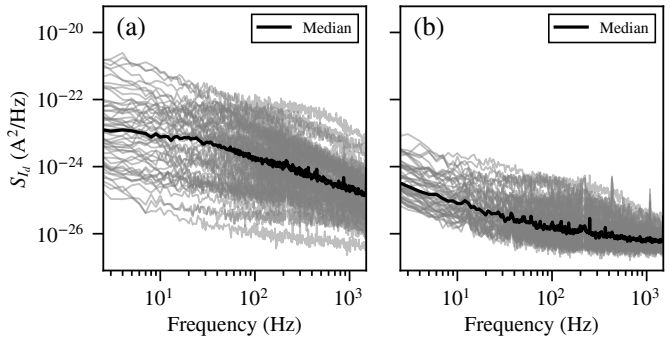

Fig. 3. Drain current noise (S_{I_d}), as a function of frequency for 50 transistors from (a) the standard layout, and (b) the octagonal layout, for I_d = 30 nA and T = 25°C. The black curve represents the median S_{I_d} value.

layout characteristics, while typical variability is visible on the octagonal layout. Additionally, the presence of hump is not systematic, which results from the variability of the edge transistors' V_t.

Edge conduction along the STI is an issue for DC and mismatch performance, but can also degrade the level of LFN. Fig. 3a and 3b show the drain current noise (S_{I_d}) measured on 50 transistors of the standard and octagonal layouts respectively, for a constant drain current I_d = 30 nA at 25°C, where the impact of the edge transistor can be probed. For equivalent biasing conditions, the standard layout's median noise is almost two decades higher than the octagonal one, and its variability is much higher. This observation gives a first insight on the impact the edge MOS can have due to its smaller size, since LFN scales inversely with the area when it comes to its average level and variability [6].

Deeper analysis on the edge transistor influence can be made by measuring the median input-referred gate voltage noise ($S_{V_g} = S_{I_d}/g_m^2$) extracted at 10 Hz as a function of I_d, as presented in Fig. 4. The standard layout's noise is confirmed to be much higher than the octagonal one in the subthreshold region, but the gap between the two tends to decrease for currents above 1 µA. The $1/f$ noise behavior of a MOS transistor can be described by the carrier number fluctuations (CNF) with correlated mobility fluctuations (CMF) model,

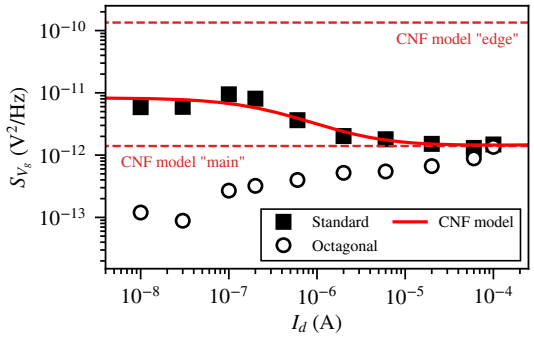

Fig. 4. Median S_{V_g} extracted at 10 Hz, as a function of the drain current for both studied layouts, at T = 25°C. The dashed curves are the CNF models for the main and edge MOS of the standard layout transistor, and the red curve is the CNF model on the sum of both contributions.

defined as [7]:

$$S_{V_g} = S_{V_{fb}} \left(1 + \Omega \frac{I_d}{g_m}\right)^2, \tag{1}$$

$$S_{V_{fb}} = \frac{q^2 \lambda k_B T N_t}{f W L C_{ox}^2}, \tag{2}$$

where Ω is the CMF factor linked to the remote Coulomb scattering effect on the mobility, and $S_{V_{fb}}$ is the input-referred flatband voltage noise, where λ is the tunneling attenuation length, and N_t is the density of oxide traps in volume and energy responsible for LFN. For the octagonal MOS, S_{V_g} increases with the current, which is described by the CNF/CMF model with $\Omega > 0$. A purely CNF-like behavior with Ω = 0 should show a constant S_{V_g}. However, the standard layout MOS shows a decreasing S_{V_g}, especially between 100 nA and 50 µA. This behavior corresponds to the impact of the edge transistor, which has a smaller surface and a possibly higher N_t, leading to a higher $S_{V_{fb}}$, and thus a higher S_{V_g} in regimes where its contribution is non-negligible, that is in the subthreshold region.

The latter can be properly modeled knowing the DC characteristics of each contribution on the total current. Since drain current noise sources add up for transistors put in parallel, the total S_{V_g} can be expressed through the contribution of the main and edge transistors in the context of the CNF model:

$$S_{V_g} = \frac{S_{I_d}}{g_m^2} = \frac{S_{V_{fb},\text{main}}\, g_{m,\text{main}}^2 + S_{V_{fb},\text{edge}}\, g_{m,\text{edge}}^2}{\left(g_{m,\text{main}} + g_{m,\text{edge}}\right)^2}. \tag{3}$$

The acquisition of each independent contribution is made possible thanks to Monte-Carlo SPICE simulations, where a width of 0.4 µm for the edge transistor, with the centering and V_t mismatch predicted by the given model, seems to qualitatively reproduce the observations at DC-level, as shown by Fig. 5. Using (3) and the simulations, the noise behavior of the standard layout transistor can be properly modeled as demonstrated by Fig. 4. However, the smaller width of the edge transistor is not sufficient to account for the increase of S_{V_g} in lower currents, and an N_t four times greater than the one found for the main transistor was taken. This could result from the differences in the silicon/oxide interface quality near

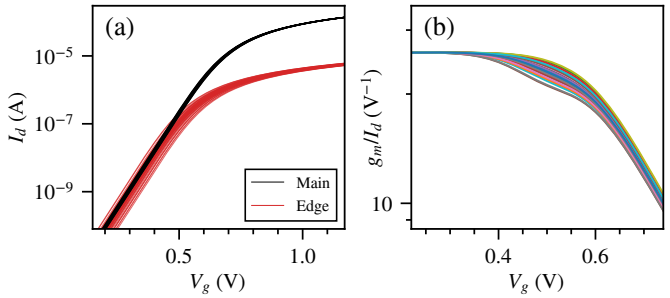

Fig. 5. (a) I_d-V_g Monte-Carlo SPICE simulations for 50 samples of the main transistor of width 9.6 µm (black curves), and of the edge transistor of width 0.4 µm (red curves). (b) g_m/I_d curves of the sum of both contributions, qualitatively reproducing the behavior observed on the standard layout MOS.

the edges of the transistor, as well as from the contribution of additional traps close to the STI interface. In the end, this type of behavior is managed in the PSP [8] and BSIM-BULK [9] compact models, but experimental evidence is scarce in the literature. The use of transistors suffering from edge conduction should thus be made with particular attention, since their LFN performance can be heavily degraded.

B. 1/f noise versus temperature

The second study focuses on the relationship between $1/f$ noise and temperature, with the role of STI edge conduction. Fig. 6a and 6b show the median S_{V_g} extracted at 10 Hz as a function of I_d for the standard and octagonal layouts respectively, at three different temperatures. First, temperature has minimal impact on the octagonal layout's median S_{V_g}. The CNF model of (1) and (2) predicts the noise to be proportional to k_BT, but either a slightly decreasing or slightly increasing S_{V_g} are observed depending on the current regime. The temperature effect can be considered weak (less than a factor 2 of difference between -40°C and 125°C), and the device-to-device variability or the measurement uncertainties could influence the measured median noise. On the other hand, strong variation of S_{V_g} as a function of temperature is found for the standard layout MOS in Fig. 6a, far from the theoretical dependency of (2). At -40°C, the noise is degraded and increases by almost a decade in low currents regime, but its level heavily decreases at 125°C and is identical to the octagonal layout's noise. For stronger drain currents above 10 µA, whatever the temperature, S_{V_g} falls back to similar values as observed for the octagonal layout.

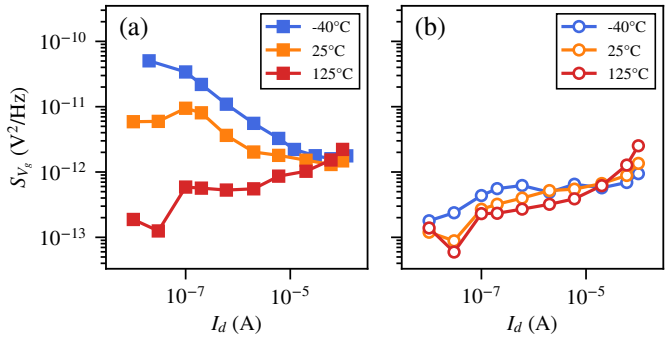

Fig. 6. Median S_{V_g} as a function of I_d measured at -40°C, 25°C, and 125°C, for (a) the standard layout, and (b) the octagonal layout transistors.

Again, these results are consistent with the influence of the edge transistor. Indeed, the latter is more visible at lower temperatures due to its weaker V_t and subthreshold slope temperature dependence. On the other hand, the octagonal MOS is immune to the hump effect, and does not show any strong noise degradation for lower temperatures. Hence, there is a direct link between the presence of a parasitic edge transistor and the temperature behavior of $1/f$ noise. Modeling this phenomenon thus requires a fine understanding of the edge transistor at multiple temperatures, including its mismatch.

C. Influence of STI edge conduction on RTN

The last study proposes evidence of the impact of the edge transistor on the measured RTN at statistical level. Here, RTN is characterized on 100 to 200 samples thanks to an automatic histogram-based procedure. Its evaluation focuses on the number of RTN-inducing traps following a Poisson distribution, and their associated amplitudes showing a lognormal distribution. The average RTN parameters are extracted on both studied layouts, for different drain currents and temperatures, and are presented in Fig. 7. Similarly to the observations made on $1/f$ noise, the RTN parameters are degraded for the standard layout: at 25°C, it shows a higher number of RTN traps (Fig. 7a) than its octagonal counterpart (Fig. 7b). This increase is consistent with the impact of the smaller edge transistor, since the presence of RTN will increase when the device's surface decreases [10]. Then, decreasing the temperature amplifies this phenomenon, while increasing it hides it and shows levels akin to the octagonal MOS. The average RTN amplitudes ($\Delta V_g = \Delta I_d/g_m$) are also degraded in lower current regimes for the standard MOS (Fig. 7c), compared to the octagonal one (Fig. 7d), this time whatever the temperature. In the same manner as $1/f$ noise, the octagonal layout shows a roughly increasing average ΔV_g with I_d, that does not seem to be impacted by temperature,

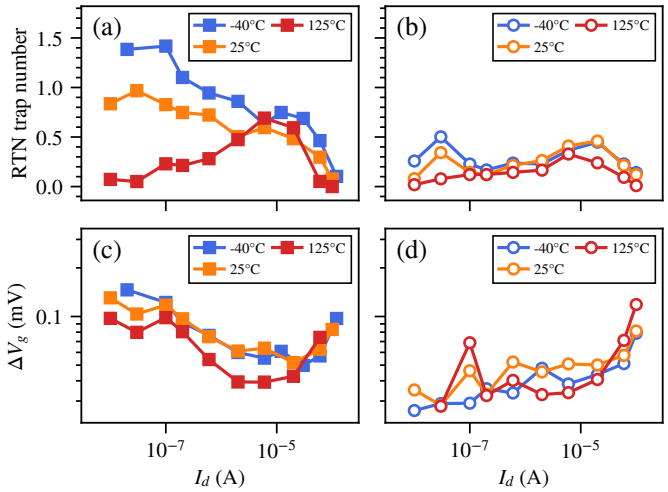

Fig. 7. Average number of RTN-inducing traps and average ΔV_g as a function of I_d for (a) and (c): the standard MOS, and (b) and (d): the octagonal MOS.

which a CNF/CMF model can properly describe [11]. Again, the standard layout MOS shows a decreasing amplitude with the drain current due to the higher edge transistor's average ΔV_g, then falls back to levels aligned with the octagonal MOS.

The edge transistor's influence on the average RTN amplitude can be directly probed on the distributions of ΔI_d, illustrated in Fig. 8. The amplitudes are well described by lognormal distributions, but the ones measured at I_d = 600 nA show some bimodal behavior. At this intermediate current, the main and edge MOS have similar contributions on the total current, and the same goes for their contributions on the total noise. The bimodal distribution can thus be explained by the simultaneous draw of RTN-inducing traps from the main MOS, with a relatively big surface and small RTN amplitudes, and from the edge MOS, with a small surface and thus showing bigger amplitudes. This is modeled considering the mixture of two lognormal distributions of equal weights, with a CDF described by the following equations:

$$F(\Delta I_d) = \frac{1}{2}F_{\text{main}}(\Delta I_d) + \frac{1}{2}F_{\text{edge}}(\Delta I_d), \tag{4}$$

$$F_i(\Delta I_d) = \Phi\left[\frac{\log(\Delta I_d/w_i) - \mu_i}{\sigma_i}\right], \tag{5}$$

where Φ is the normal distribution CDF, and w_i is the contribution of i on the total current. The extraction at I_d = 600 nA on the SPICE simulation from Fig. 5a gives $w_{\text{main}} \approx 2/3$ and $w_{\text{edge}} \approx 1/3$, with a roughly Gaussian spread due to the edge transistor's V_t mismatch, but not considered in (5) as a first approximation. The model of (4) is then fitted on the bimodal distribution in Fig. 8, and gives the average ΔI_d values for the main and edge transistors to be 1.3 nA and 4.3 nA, and the spreads σ_{main} = 0.1 and σ_{edge} = 0.4 decade respectively. The larger values of the average ΔI_d and standard deviation for the edge MOS are consistent with the RTN behavior for smaller devices. Note that the edge transistor's contribution is also visible when looking at the distribution for I_d = 30 nA, where the spread of ΔI_d is close to the one extracted from the edge part of the previous distribution. For a stronger current I_d = 20 µA, the edge transistor becomes negligible in the total current, and its impact is no longer visible in the distribution, where its spread is closer to the one extracted for the main part of the bimodal distribution. Hence, RTN requires proper modeling that takes into consideration edge conduction effects.

IV. Conclusion

The impact of STI edge conduction effects on $1/f$ noise and RTN in MOSFETs, with focus on the influence of bias and temperature, has been examined. Firstly, the CNF model allows the prediction of the increase of noise in the subthreshold region, where the fit can be fine-tuned thanks to DC analysis of the hump effect and SPICE simulations. Secondly, lowering the temperature degrades even more the $1/f$ noise in the subthreshold region when the transistor suffers from edge conduction effects, while increasing it hides the effect. An optimized hump-free layout allows the complete removal of these specific bias and temperature behaviors. Finally, the edge conduction mechanism can be probed on the distribution of RTN amplitudes, where a mixture model between the main and edge transistors can describe the statistical RTN behavior. The results highlight the need for realistic modeling of $1/f$ noise and RTN, and demonstrate the superiority of optimized layouts when it comes to low-noise applications.

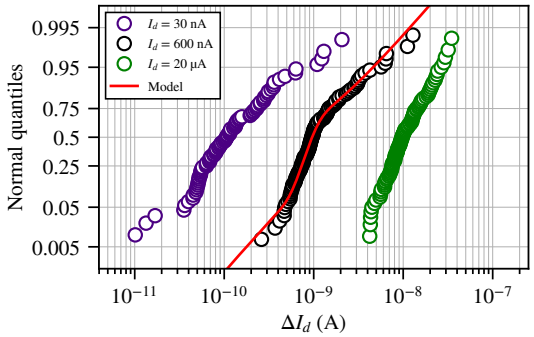

Fig. 8. Distributions of ΔI_d measured on 200 standard layout transistors, for three different drain current levels: 30 nA, 600 nA, and 20 µA, and T = 25°C. The red curve is the model using (4).

References

[1] F. Simioni, L. Labate, D. Savio, M. Brizzi, F. Ottogalli, R. Marchetti, S. Brazzelli, and M. Rossetti, "Impact of layout and channel processing on CMOS low frequency noise variability," in *ESSDERC 2023 - IEEE 53rd European Solid-State Device Research Conference (ESSDERC)*, Sep. 2023, pp. 17–20.

[2] M. Gouveia da Cunha, S. Place, O. Gauthier, N. Virollet, M. Vignetti, P. Martin-Gonthier, P. Magnan, and V. Goiffon, "Design Techniques Evaluation to Mitigate RTS Noise Effect in Column ADC of 3D Stacked Image Sensors," in *2024 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2024, pp. P67.TX–1–P67.TX–6.

[3] Y. Joly, L. Lopez, J.-M. Portal, H. Aziza, Y. Bert, F. Julien, and P. Fornara, "Impact of hump effect on MOSFET mismatch in the sub-threshold area for low power analog applications," in *2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology*, Nov. 2010, pp. 1817–1819.

[4] Y. Joly, L. Lopez, J.-M. Portal, H. Aziza, P. Masson, J.-L. Ogier, Y. Bert, F. Julien, and P. Fornara, "Octagonal MOSFET: Reliable device for low power analog applications," in *2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, Sep. 2011, pp. 295–298.

[5] https://www.synergie-concept.fr/noise.php.

[6] E. G. Ioannidis, S. Haendler, C. G. Theodorou, S. Lasserre, C. A. Dimitriadis, and G. Ghibaudo, "Evolution of low frequency noise and noise variability through CMOS bulk technology nodes from 0.5μm down to 20nm," *Solid-State Electronics*, vol. 95, pp. 28–31, May 2014.

[7] E. G. Ioannidis, C. A. Dimitriadis, S. Haendler, R. A. Bianchi, J. Jomaah, and G. Ghibaudo, "Improved analysis and modeling of low-frequency noise in nanoscale MOSFETs," *Solid-State Electronics*, vol. 76, pp. 54–59, Oct. 2012.

[8] S. Martinie, O. Rozeau, T. Poiroux, J.-C. Barbé, F. Gilibert, X. Montagner, S. E. Ghouli, A. Juge, D. J. Geert Smit, and A. J. Scholten, "New physical insight for analog application in PSP bulk compact model," in *2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2018, pp. 356–359.

[9] A. Sharma, Y. H. Zarkob, R. Goel, C. K. Dabhi, G. Pahwa, C. Hu, and Y. S. Chauhan, "Recent Enhancements in the Standard BSIM-BULK MOSFET Model," in *2022 IEEE International Conference on Emerging Electronics (ICEE)*, Dec. 2022, pp. 1–6.

[10] A. Ghetti, C. Monzio Compagnoni, A. S. Spinelli, and A. Visconti, "Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Deca–Nanometer Flash Memories," *IEEE Transactions on Electron Devices*, vol. 56, no. 8, pp. 1746–1752, Aug. 2009.

[11] O. Gauthier, S. Haendler, Q. Rafhay, and C. Theodorou, "Variability of Trap-induced Mobility Fluctuations in Nanoscale Bulk and FD-SOI MOSFETs," in *2023 International Electron Devices Meeting (IEDM)*, Dec. 2023, pp. 1–4.