A 12-Gb/s Broadcast Video Retimer Equalizing 53+dB Coax at a BER $<$ 1e–12 Without FEC

Abishek Manian[1], Yongseon Koh[1], Robin Gupta[1], Amit Rane[1], Ashkan Roshan Zamir[1], Mike Vrazel[2], Chris Yim[3], Pakyiu Leung[1], Steven Wong[1], Doug Wente[3], Jim Skidmore[3], Nithin Poduval[1], Jameson Zhang[1], Yonghui Tang[3], Shita Guo[3], Eric Chen[1], Mehmet Sahin[1], Nasser Mohammadi[1], Michael Lu[1]
Texas Instruments: [1]Santa Clara, CA 95054, USA; [2]Duluth, GA 30096, USA; [3]Dallas, TX 75243, USA

***Abstract*—This paper describes a serial digital interface retimer supporting up to 12-Gb/s 4K ultra-high-definition (UHD) video. Through architecture and circuit techniques including a time-domain pre-cursor intersymbol interference mitigation, a dual-feedback loop baseline-wander correction, and least mean squares equalizer adaptation and amplitude estimation, the proposed retimer equalizes single-ended coax up to 53-dB and 58-dB insertion losses for pathological and color bar patterns, respectively, achieving a bit error rate $< 10^{-12}$ in the absence of forward error correction.**

***Keywords*—broadcast video, SDI, pathological, retimer, receiver, pre-cursor ISI, baseline-wander correction, single-ended, coax.**

I. Introduction

From global sporting events like the World Cup and the Olympics to everyday news and live concert streams, broadcast video continues to play a central role in enriching the lives of billions, arguably more so in today's age of artificial intelligence. Serial digital interface (SDI) retimers, also known as reclockers, are used in broadcast video applications to receive video data from a camera through a long single-ended 75-Ω coaxial cable, equalize it and send a clean version of the data to a field-programmable gate array (FPGA) for video processing and overlay, as depicted in Fig. 1.

These systems encounter two major issues. Firstly, these retimers need to support a wide range of cable lengths with losses exceeding 40 dB at 12 Gb/s for 4K ultra-high-definition (UHD) video. Even though the data rates are lower than most of the wireline research areas today, ultra-high channel losses combined with single-ended signaling pose significant challenges in terms of equalization and clock recovery requiring innovative breakthroughs, especially due to the absence of forward error correction (FEC) in the SDI standard defined by the society of motion pictures and television engineers (SMPTE). Secondly, the problem is compounded by the fact that the scrambler used to encode the data, as defined by SMPTE, has an inherent flaw [1]. When a particular video pattern (magenta + gray/green static image) is applied, the scrambler produces a dc imbalanced pattern with 1 ONE and 19 ZEROs repeatedly for several microseconds at a time, interspersed between occurrences of random data. A complementary repetitive pattern with 1 ZERO and 19 ONEs is equally likely to occur. These low transition-density "pathological" patterns pose a major bottleneck in these ac-coupled systems, depicted in Fig. 2. The low-frequency content of these pathological patterns is blocked by the off-chip ac-coupling capacitor, resulting in baseline

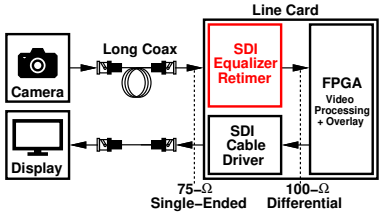


Fig. 1. Broadcast video production application.

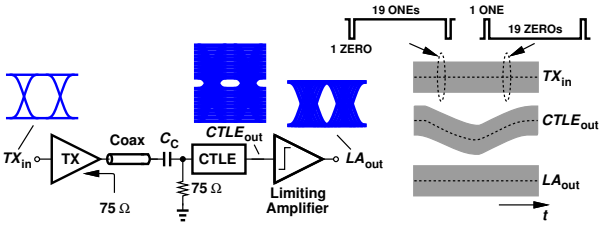


Fig. 2. Issue of baseline wander due to pathological pattern.

wander. Consequently, the received waveform has increased jitter and reduced eye-opening affecting signal integrity if left uncorrected. Additionally, the lack of "randomness" in the pathological sequence may lead to mal-adaptation of equalizer coefficients. This work addresses these issues.

II. Proposed Architecture

Figure 3(a) shows the proposed overall retimer datapath architecture. The front-end matching network, shown in Fig. 3(c), consists of a common-mode regulator with the P-side connected to the single-ended coax and the N-side terminated with 75-Ω on the board. T-coils are utilized to meet SMPTE return loss specifications [2], [3].

A. Equalization Strategy

In order to tackle the first problem of ultra-high channel losses, this work incorporates a 4-stage continuous-time linear equalizer (CTLE) with programmable capacitive degeneration and noise filtering using programmable capacitors at the output. As this work targets channel loss $>$ 50 dB at 12 Gb/s, the CTLE's frequency response is designed to match the inverse of the channel response only at low-to-mid frequencies to cancel long-tail post-cursor intersymbol interference (ISI) while filtering out high-frequency noise. Each CTLE stage and the boost distribution across stages are tuned to achieve optimal noise performance. At 58-dB coax loss, the CTLE adapts to a setting with 36-dB peaking. To equalize the

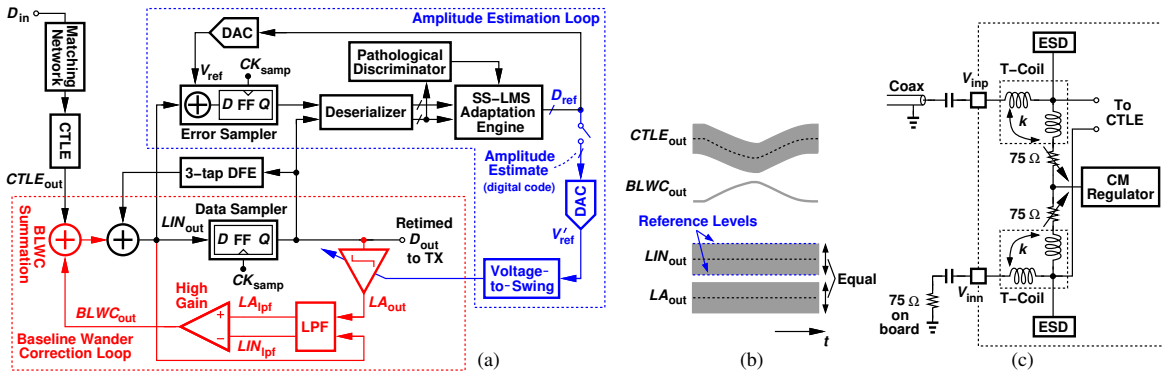


Fig. 3. (a) Overall retimer datapath architecture, (b) baseline-wander correction operation, and (c) front-end matching network.

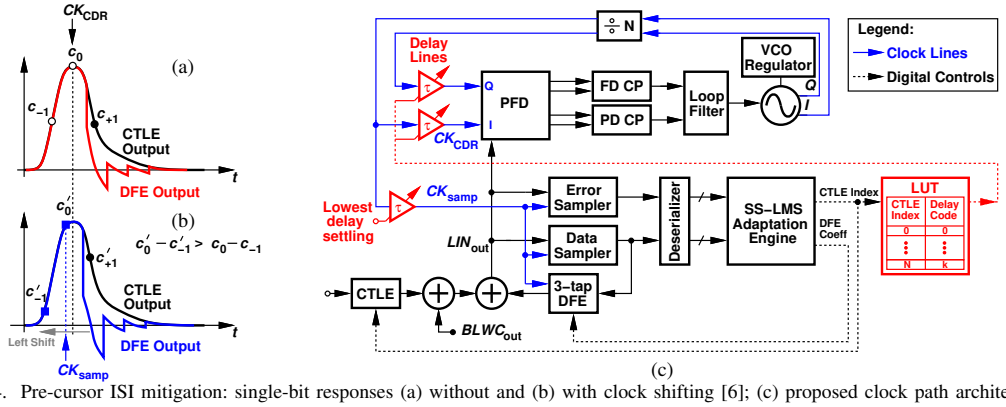


Fig. 4. Pre-cursor ISI mitigation: single-bit responses (a) without and (b) with clock shifting [6]; (c) proposed clock path architecture.

remaining high-frequency loss near Nyquist, a 3-tap decision-feedback equalizer (DFE) is employed. The CTLE and DFE coefficients are adapted using sign-sign least mean squares (SS-LMS) algorithm. The CTLE adapts once after detecting the presence of an input signal whereas the DFE continuously adapts to track temperature and voltage variations.

Such a high insertion loss also causes significant pre-cursor ISI which is not compensated effectively by CTLE and DFE. The SDI standard does not allow a TX feedforward equalizer (FFE) like in [4], whereas an RX FFE like in [5] has noise amplification issues. To ease the tradeoff between pre-cursor ISI and noise, a time-domain clock phase adjustment technique was proposed in [6]. Leveraging the bell shape of the single-bit response in Fig. 4(a), shifting the sampling clock phase to the left significantly reduces the pre-cursor ISI with little impact on the main cursor as shown in Fig. 4(b). However, the data filtering used in [6] reduces the clock-data recovery's (CDR) phase detector gain, is incompatible with SDI pathological patterns, and when combined with the edge-sampler voltage threshold adjustment of [6] may cause inability for the CDR to lock in the presence of highly lossy channels and baseline wander. Thus, we propose a pre-cursor ISI mitigation circuit, shown in Fig. 4(c), in which programmable CML delay lines are used to delay the full-rate CDR clock with respect to the sampler clock, effectively shifting the latter to the left. The consequent increase in post-cursor ISI terms is compensated by the adaptive 3-tap DFE discussed above. However, large phase shifts in the sampler clock can result in large DFE tap weights leading to potential burst-error concerns. To alleviate this issue, the phase shift is limited to < 0.07 UI in this work. Adjusting only the sampler clock phase yields no noise amplification unlike RX FFEs. The delay lines are adaptively controlled through the aforementioned SS-LMS algorithm as follows. The channel loss and consequently the single-bit response is estimated based on the adapted CTLE index which is fed into a look-up table (LUT) to determine the delay settings. The LUT is constructed by sweeping Belden 1694A coax length in 5-m increments in simulations and mapping optimal delays to the adapted CTLE indices. Figures 5(a) and (b) show a comparison of simulated eye diagrams at 12 Gb/s for a 60-dB lossy channel at the DFE summation node marked "linear output" or LIN_{out}, without and with a 5-ps sampler clock adjustment, respectively. A 67% increase in the vertical eye opening (VEO) is observed with the latter.

B. Handling Pathological Patterns

Arriving at the second problem of pathological patterns, prior techniques such as [7] use a combination of input high-pass filter with quantized/sampled positive feedback to address baseline wander. However, the positive feedback can rail out in the presence of clock-like patterns due to low swings or closed eyes in the chain. Furthermore, the parasitics of the on-chip ac coupling capacitor of the high-pass filter degrade datapath bandwidth and/or swings. Overcoming these limitations, an alternative baseline-wander correction (BLWC) scheme is proposed, highlighted in red in Fig. 3(a). Using

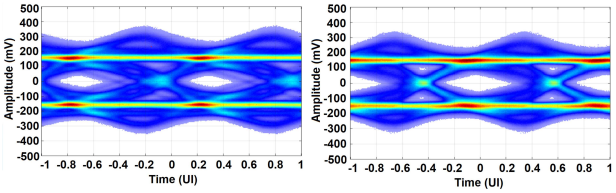


Fig. 5. Simulated 12-Gb/s eyes at LIN_{out} for 60-dB loss with pathological pattern: (a) no clock adjustment and (b) with 5-ps clock adjustment.

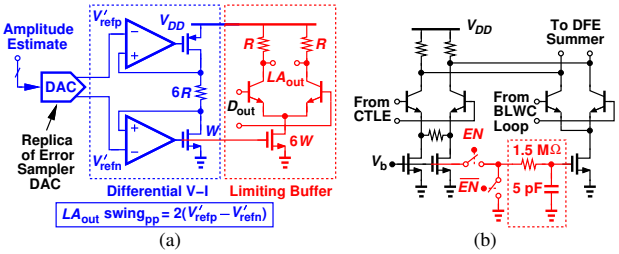


Fig. 6. (a) Converting amplitude estimate to swing. (b) BLWC summation.

the retimed output as an accurate replica of the far-end transmitter's (TX) waveform, we sense the low-frequency content of the limiting amplifier output, LA_{out}, using a low-pass filter (LPF), and force it to equal that of LIN_{out} through a high-gain feedback loop, effectively correcting baseline wander. Unlike prior techniques, the proposed dual-feedback loop allows us to connect the feedback, $BLWC_{out}$, at any point in the datapath prior to the sampler, thus offering an additional degree of freedom in optimizing correction range and loop gain along with other high-speed datapath parameters like linearity, bandwidth and noise. In this work, the datapath linearity is not limited by the CTLE and the CTLE's linear range accommodates the maximum input wander of 50 mV as per the SMPTE specification [2]. Thus, the BLWC feedback is connected after the CTLE to maximize its correction range and loop gain while minimally impacting CTLE's performance.

Due to the high loop gain of the BLWC loop, nominally 40 dB, the feedback summation can be made nonlinear. The LPFs in feedback are designed such that the closed-loop unity-gain bandwidth (1.5 MHz) is more than two orders of magnitude higher than the external ac coupling capacitor's cutoff frequency (typically $<$ 6 kHz) by design. This fact combined with the self-referenced nature of this architecture desensitizes it to the external ac coupling capacitance.

Since we equalize the low-frequency content of LIN_{out} and LA_{out}, their amplitudes must be equal to prevent under/over-correction of baseline wander, as indicated by the waveforms in Fig. 3(b). The amplitude at LIN_{out} varies with process, voltage and temperature (PVT), and equalizer settings. In order to adaptively set the correct amplitude at LA_{out}, we leverage the on-chip SS-LMS engine as shown in blue in Fig. 3(a). The SS-LMS engine uses the error sampler to estimate mean of the positive and negative data levels (reference levels) at LIN_{out}, as shown in Fig. 3(b). The absolute value of these two reference levels are averaged to eliminate offset and serve as the amplitude estimate. As the LMS engine continuously runs in the background, the amplitude estimates get updated

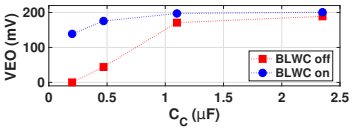


Fig. 7. Simulated VEO at LIN_{out} for a 12-Gb/s pathological pattern (assuming 30-μs run length) with a 90-m (53-dB) coax.

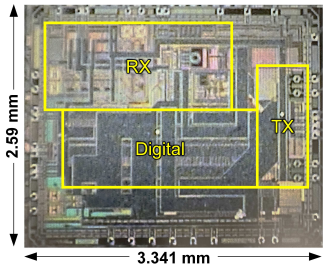


Fig. 8. Die photograph.

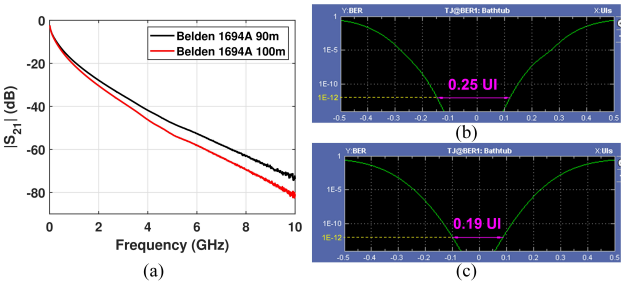


Fig. 9. (a) Measured insertion loss of Belden 1694A cables. Measured 12-Gb/s bathtub curves at LIN_{out} for (b) 90-m (53-dB) coax with pathological pattern, and (c) 100-m (58-dB) coax with color bar pattern.

periodically through a programmable timer to track voltage, temperature, and TX swing variations.

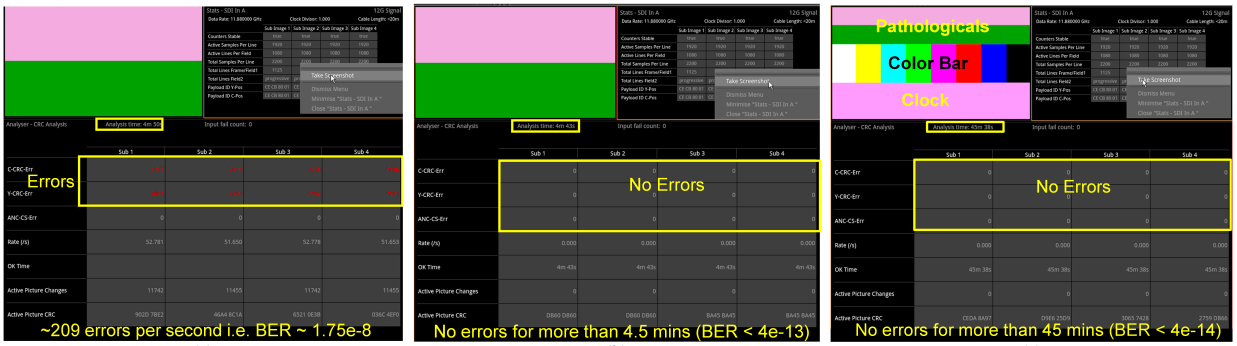
The digital amplitude estimate is converted to swing using a DAC and a voltage-to-swing converter, shown in Fig. 6(a). The DAC, which is a replica of that in the error sampler path [Fig. 3(a)], converts the digital amplitude estimate into an analog differential voltage, $V'_{refp} - V'_{refn}$, which is then converted into a proportional current using a dual op amp loop. This current is scaled appropriately to set the swing of the limiting buffer. The replica DAC ensures PVT tracking of the swing at LA_{out} compared to that sensed at LIN_{out} by the error sampler.

The pathological discriminator in Fig. 3(a) detects pathological sequences and ensures only the random non-pathological portion of the received data is used to estimate amplitudes and equalizer coefficients, making them immune to the periodic nature of pathological patterns and incoming baseline wander.

Figure 7 depicts the VEO improvement at LIN_{out} for various external ac coupling capacitor values when BLWC is turned on for a 90-m coax for a 12-Gb/s pathological pattern.

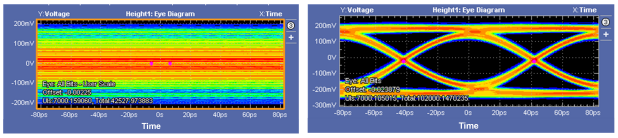
C. Other Considerations

The BLWC loop is enabled only after the CDR locks and initial equalizer adaptation is completed to ensure that 1) the data sampler makes a majority of correct decisions and is a reasonable replica of the far-end TX, and 2) the amplitude estimate has been established before the loop is set running. Since the BLWC is a high-gain analog loop, the



(a) (b) (c)

Fig. 10. Measured 12-Gb/s results on Phabrix Qx video analyzer using 90-m (53-dB) coax for: (a) pathological pattern with BLWC off, (b) pathological pattern with BLWC on, and (c) composite pattern with BLWC on.



(a) (b)

Fig. 11. Measured 12-Gb/s eyes at retimer's (a) input and (b) output, for a 90-m coax for composite pattern with BLWC on (horizontal: 20 ps/div, vertical: 100 mV/div).

initial conditions are indeterminate and the CDR may lose lock if the loop is enabled abruptly. To resolve this issue, an RC filter is inserted at the bias of feedback circuit to enable the loop gracefully as shown in Fig. 6(b).

The retimed data output in Fig. 3 is buffered and driven out using a 100-Ω differential hybrid voltage-mode driver [8].

III. Experimental Results

The proposed retimer is fabricated in TI's 130-nm BiCMOS process and integrated in a wire-bond QFN package. Figure 8 shows the die photograph. To measure the retimer performance, we use a Phabrix Qx video generator whose output is connected to a Belden 1694A cable and subsequently ac-coupled using a 4.7-µF capacitor to the device under test (DUT). The video generator output is also internally ac coupled (capacitance unknown). Shown in Fig. 9(a) is the measured insertion loss of Belden 1694A cables, indicating 53-dB loss at 6 GHz for 90 m and 58 dB for 100 m, not including the loss of connectors, board traces and package which amount to an additional 1.7 dB at 6 GHz. The output of the DUT is looped back to the Phabrix Qx video analyzer through an off-chip 100-Ω to 75-Ω limiting buffer for error analysis. Shown in Fig. 9(b) and (c) are the bathtub curves at LIN_{out}, after passing through on-chip limiting buffers for an 800-mV_{pp} 12-Gb/s pathological pattern (72-mV measured wander at DUT input, exceeding the 50-mV SMPTE specification) with a 90-m coax and color bar pattern with a 100-m coax, indicating horizontal eye openings of 0.25 UI and 0.19 UI, respectively, at a bit error rate (BER) $< 10^{-12}$ without FEC. Figures 10(a) and (b) show the video analyzer's received pathological pattern with BLWC turned off and on, respectively, indicating an improvement in BER from $\sim 10^{-8}$ to $< 10^{-12}$, when a 90-m coax is attached before the DUT. Shown in Fig. 10(c) is the video analyzer result with a composite pattern: magenta + green pathological pattern, color bar and clock in pink, with a 90-m coax. We observe zero errors for more than 45 minutes indicating a BER $< 10^{-13}$. Figures 11(a) and (b) show the retimer input and output eyes for this case, respectively.

TABLE I
Comparison to Recent SDI Retimers

Metrics	[9]	[10]	This Work
Pathological Cable Reach[a] at 12 Gb/s	Not reported	Not reported	**90 m [b] (53 dB)**
Color Bar Cable Reach[a] at 12 Gb/s	80 m (46 dB)	75 m (44 dB)	**100 m [b] (58 dB)**
Pathological Cable Reach[a] at 3 Gb/s	Not reported	Not reported	**220 m (56 dB)**
Color Bar Cable Reach[a] at 3 Gb/s	190 m (49 dB)	200 m (51 dB)	**230 m (59 dB)**
Supply Voltage (V)	1.8, 1.2	2.5	**2.5**
Bit Error Rate	Not reported	$< 10^{-12}$	**$< 10^{-12}$**
Die Area (mm^2)	Not reported	Not reported	**8.65**
Power (mW)	405	275	**350**
Technology	Not reported	Not reported	**130-nm BiCMOS**
Package (QFN)	40-pin	32-pin	**32-pin**
Package Form (mm^2)	6 × 4	5 × 5	**5 × 5**

[a] Only Belden 1694A coax loss; not including PCB, connector, and package losses.
[b] Measured over multiple wafer lots, –40 to 85°C ambient, 800-mV_{pp} ± 10% TX swing.

Table I compares the proposed retimer against recent commercial 12-Gb/s SDI retimers, indicating significant improvement in cable reach across patterns and data rates.

References

[1] D. Brown and J. Hudson, "Pathological check codes and the SMPTE scrambler in the HD Age," *SMPTE Motion Imaging Journal*, Oct. 2011.

[2] *12Gb/s Signal/Data Serial Interface – Electrical*, SMPTE Standard ST 2082-1:2023, Nov. 2015.

[3] S. Galal and B. Razavi, "Broadband ESD protection circuits in CMOS technology," *IEEE JSSC*, vol. 38, pp. 2334-2340, Dec. 2003.

[4] A. Mostafa *et al.*, "A 2.2pJ/b 212.5Gb/s PAM-4 transceiver with > 46dB reach in 5nm FinFET," *ISSCC*, pp. 138-139, 2025.

[5] Y.-P. Lin *et al.*, "A 2.06pJ/b 106.25Gb/s PAM-4 receiver with 3-tap FFE and 1-tap speculative DFE in 28nm CMOS," *ISSCC*, pp. 146-147, 2025.

[6] J. Ren *et al.*, "Precursor ISI Reduction in High-Speed I/O," *VLSI Symp.*, pp. 134-135, 2007.

[7] E. Fang *et al.*, "A 5.2Gbps hypertransport™ integrated AC coupled receiver with DFR DC restore," *VLSI Symp.*, pp. 34-35, 2007.

[8] K. Abugharbieh *et al.*, "A 33 mW 12.5 Gbps BiCMOS transmitter for high speed backplane applications," *Microelectronics Journal*, Jan. 2014.

[9] *12G UHD-SDI Reclocking Adaptive Cable Equalizer GS12341 Datasheet*, Semtech, Aug. 2019.

[10] *12G UHD-SDI Bidirectional I/O With Integrated Reclocker LMH1297 Datasheet*, Texas Instruments, July 2022.