A 0.77mK-Resolution 78fJ·K^2-FoM Resistor-Based Temperature Sensor Utilizing a Multi-Phase Slope-Boost Frequency-Locked Loop

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***Abstract*—This work reconfigures a multi-phase slope-boost (MP-SB) waveform and extends its application throughout a frequency-locked-loop (FLL)-based temperature sensor, enabling simultaneous energy–noise optimization. As a result, the proposed sensor achieves a state-of-the-art FoM of 78 fJ·K² and the best-reported resolution of 0.77 mK among time-domain designs, broadening its applicability to sub-mK temperature-compensated systems. Fabricated in a 180-nm CMOS process, the proposed sensor is the smallest (0.06 mm²) among sub-mK-resolution sensors and is process-scalable, making it suitable for precise local temperature sensing.**

***Index Terms*—temperature sensor, frequency-locked loop (FLL), multi-phase slope-boost (MP-SB) technique**

I. Introduction

Recently, resistor-based temperature sensors [1]–[11] have achieved high energy efficiency, small silicon footprint, and process scalability, making them suitable for on-chip thermal-monitoring applications including DRAMs and microprocessors [1], [2]. In addition, some of them also provide sub-mK resolution, which is critical for temperature compensation in high-performance frequency references [9], [10]. Achieving both area efficiency and high resolution enables precise local temperature sensing and extends applicability to performance-critical systems.

However, such performance metrics have remained difficult to attain simultaneously in prior sensors, which are classified into successive-approximation-register (SAR), delta-sigma-modulation (DSM), and time-domain designs. SAR-based works [8] exhibit excellent area efficiency, but are application-limited due to their poor resolution of >10 mK. Although DSM-based works [9]–[11] feature sub-mK resolution through noise-shaping behavior, they are area-inefficient and less scalable due to their large integration capacitors of >40 pF in total. Time-domain sensors based on frequency-locked loops (FLLs) [1]–[5] are promising candidates for both high resolution and area efficiency. However, even the state-of-the-art works exhibit limited resolution of >1 mK.

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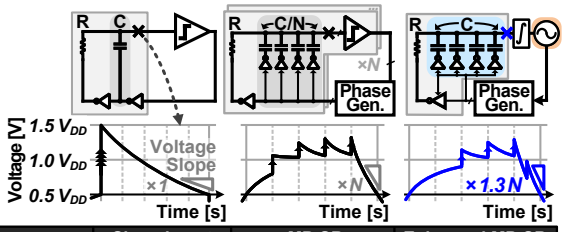

	Slope-boost	MP-SB	Enhanced MP-SB
Application	FVC[2], Relax. Osc.[12]	Relax. Osc.[13]	MP-SB FVC, MP-SB Ring VCO
Reduce jitter?	Yes (thermal and 1/f noise)		
Volt. slope	☹	😐	☺
Gate stress	☹	☺	☺
Power / area overhead	–	☹ (*N* comp. required)	☺ (No added comp.)

Fig. 1: Characteristics of slope-boost (left), MP-SB (middle), and the proposed slope-enhanced MP-SB (right) techniques.

Thereby, we present an area-efficient FLL-based temperature sensor structure, reconfiguring multi-phase slope-boost (MP-SB) technique to optimize conversion energy and noise performance. As a result, this paper proposes the first time-domain resistor-based sensor achieving sub-mK resolution (0.77 mK), which is also the smallest (0.06 mm²) among sub-mK-resolution sensors with a process-scalable structure. The remainder of the paper is organized as follows. Section II explains the FLL optimization strategy. Section III describes the circuit implementation and detailed circuit operation. Finally, Section IV discusses the measurement results, and Section V concludes this paper.

II. Design Strategy for FLL Optimization

A. Slope-Enhanced MP-SB with Extension Across FLL

The proposed FLL-based temperature sensor enhances prior slope-boost techniques, as shown in Fig. 1. The basic slope-boost technique [2], [12] reduces timing jitter due to large voltage slope, but it boosts target voltage to more than 1.5·V_{DD} at once, suffering from a transistor gate stress. A conventional MP-SB technique partially boosts the voltage across N phases for both less gate stress and an N-times larger voltage slope. However, it may consume more power and area overhead due to additional comparators [13].

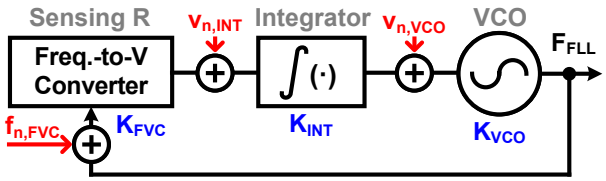

Fig. 2: FLL circuit blocks and their gain and noise models.

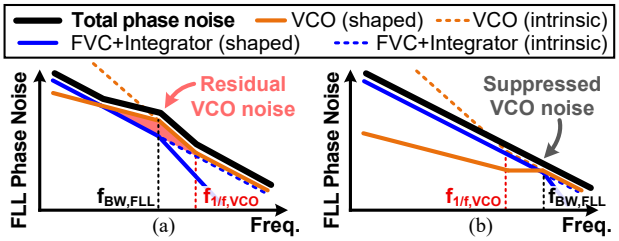

Fig. 3: FLL loop bandwidth selection based on phase noise characteristics when (a) $f_{BW,FLL} < f_{1/f,VCO}$ and (b) $f_{BW,FLL} > f_{1/f,VCO}$

Here, we further enhance the MP-SB voltage slope by 1.3× compared to [13] by re-timing the boost phases. The design overhead is also negligible, since the proposed slope-enhanced MP-SB technique only requires a few more inverters to drive the split capacitors compared to [12]. Moreover, this work extends MP-SB application throughout FLL circuit blocks for the following advantages: 1) An MP-SB FVC is presented for a large gain to optimize FLL noise; 2) A proposed MP-SB ring VCO with suppressed 1/f noise relieves FLL loop bandwidth constraints for better energy efficiency.

B. FLL Noise and Energy Optimization

Fig. 2 illustrates an FLL structure, where K_{FVC}, K_{INT}, and K_{VCO} denote the gain of a frequency-to-voltage converter (FVC), an integrator, and a voltage-controlled oscillator (VCO), respectively, and $f_{n,FVC}$, $v_{n,INT}$, and $v_{n,VCO}$ represent the input-referred noise of each block. Assuming a sufficiently high loop gain, F_n can be simplified as follows:

$$F_n \approx \sqrt{f_{n,FVC}^2 + (\frac{v_{n,INT}}{K_{FVC}})^2 + (\frac{v_{n,VCO}}{K_{FVC} \cdot K_{INT}})^2}. \quad (1)$$

To minimize F_n, K_{FVC} should be implemented as large as possible to suppress $v_{n,INT}$ and $v_{n,VCO}$ simultaneously, so that the inevitable noise component $f_{n,FVC}$ from the sensing resistors at the FVC becomes dominant during conversion. Here, K_{FVC} is expressed as follows:

$$K_{FVC} = \frac{dV_{FVC}}{dF_{FLL}} = \frac{dV_{FVC}}{dt} \cdot (F_{FLL})^{-2}, \quad (2)$$

where V_{FVC} and F_{FLL} denote FVC output voltage and FLL output frequency, respectively. Therefore, as discussed in Section III, the MP-SB FVC is implemented for large K_{FVC} with an effectively large voltage slope. In addition, a 2-stage integrator follows the FVC with a large K_{INT} to further suppress $v_{n,VCO}$ for FLL noise optimization.

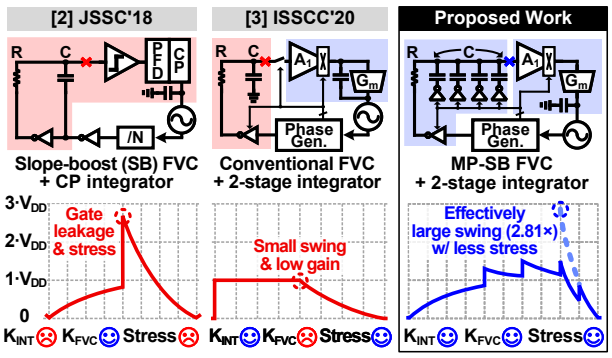

Fig. 4: Simplified block diagrams of the prior and proposed temperature sensors and characteristics of their FVC outputs.

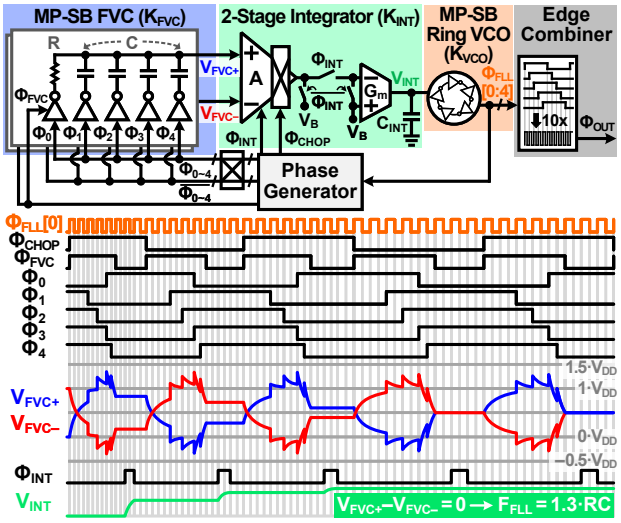

Fig. 5: Detailed architecture of the proposed MP-SB FLL-based temperature sensor and the corresponding timing diagram.

Meanwhile, Fig. 3 illustrates energy optimization strategy from FLL loop bandwidth ($f_{BW,FLL}$) constraint. When $f_{BW,FLL}$ is set below the VCO's 1/f corner ($f_{1/f,VCO}$) as depicted in Fig. 3(a), the VCO's 1/f noise is insufficiently suppressed, leaving residual noise that degrades phase noise and resolution. Therefore, as represented in Fig. 3(b), $f_{BW,FLL}$ should be chosen higher than $f_{1/f,VCO}$ to effectively suppress the VCO's 1/f noise. Fig. 3(b) further implies that a lower $f_{1/f,VCO}$ allows the FLL to achieve the same noise performance with a narrower loop bandwidth $f_{BW,FLL}$, directly reducing the FLL energy. Hence, the MP-SB ring VCO is designed to exhibit inherently low 1/f noise as described in Section III.

III. Circuit Implementation and Operation

Fig. 4 illustrates how the proposed MP-SB FLL optimizes its noise compared to prior structures [2], [3]. A prior design [2] exhibits a large K_{FVC} by a voltage swing boosted up to $2.73 \cdot V_{DD}$, inducing gate stress. Moreover, it exhibits a small K_{INT} since it has no amplification stage after the FVC block. Although another design [3] achieves a large K_{INT} using a 2-stage integrator, it shows a small K_{FVC} because it cannot utilize slope-boost FVC due to switch leakage at the integrator input.

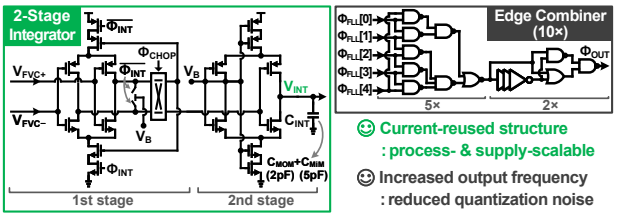

Fig. 6: Implementation of the 2-stage integrator and EC and their advantages.

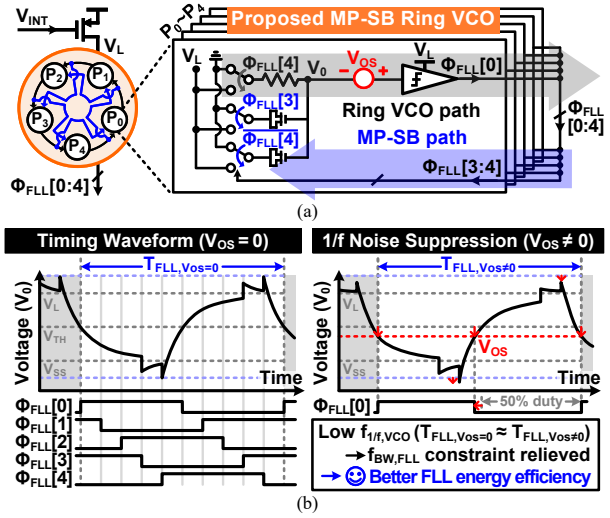

Fig. 7: (a) Implementation of the proposed MP-SB ring VCO and (b) its timing waveforms demonstrating its contribution to FLL power optimization.

To solve the prior issues, the enhanced MP-SB technique is applied to FVC to achieve both less gate stress and an effectively large swing compared to [2]. In addition, the proposed MP-SB FVC is followed by a 2-stage integrator unlike [3], since it inherently samples the voltage without the integrator input switch. Thus, the MP-SB FVC simultaneously allows 1) a large K_{INT} and 2) a large K_{FVC} with an effectively large swing ($2.81 \cdot V_{DD}$) and low stress.

Fig. 5 illustrates the architecture and timing diagram of the proposed sensor, which consists of a differential MP-SB FVC, a 2-stage integrator, an MP-SB ring VCO, a phase generator (PG), and an edge combiner (EC). From the VCO output Φ_{FLL}, the PG creates divided clocks (Φ_{FVC}, $\Phi_{0\text{-}4}$, Φ_{INT}, and Φ_{CHOP}). Φ_{FVC} determines whether the FVC is in a boost or a hold state. During the boost state, Φ_{FVC} is turned high to activate tri-state inverters in the FVC, and $\Phi_{0\text{-}4}$ sequentially boost FVC output voltages, V_{FVC+} and V_{FVC-}. When Φ_{FVC} becomes low, FVC capacitors hold the voltages at the FVC output. The voltage difference, V_{FVC+}–V_{FVC-}, is then accumulated to V_{INT} by the 2-stage integrator, which is duty-cycled by Φ_{INT}.

As depicted in Fig. 6, the integrator consists of an amplifier and a G_m-C stage with a current-reused topology to achieve high K_{INT} and scalability. Φ_{CHOP} enables chopping at the amplifier output, as V_{FVC+} and V_{FVC-} are inherently chopped by $\Phi_{0\text{-}4}$. The integration capacitor C_{INT} is implemented to be smaller (7pF) compared to DSM-based designs [9]–[11], thereby being more area-efficient and feasible for further process scaling. Since the VCO is implemented with 5 phases,

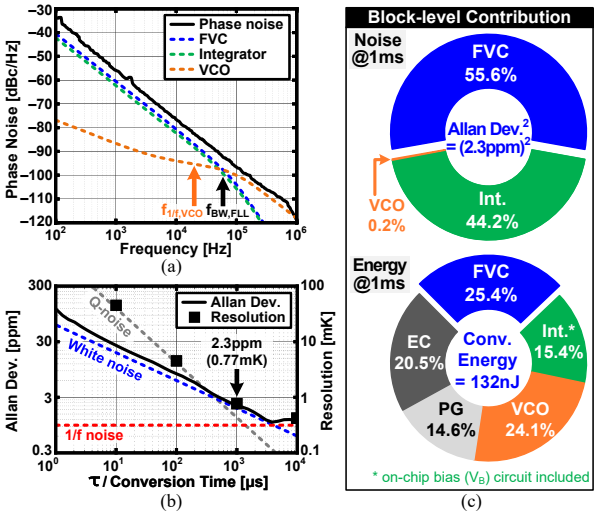

Fig. 8: (a) Measured and simulated phase noise of FLL, (b) measured Allan deviation and resolution, and (c) noise and energy breakdown.

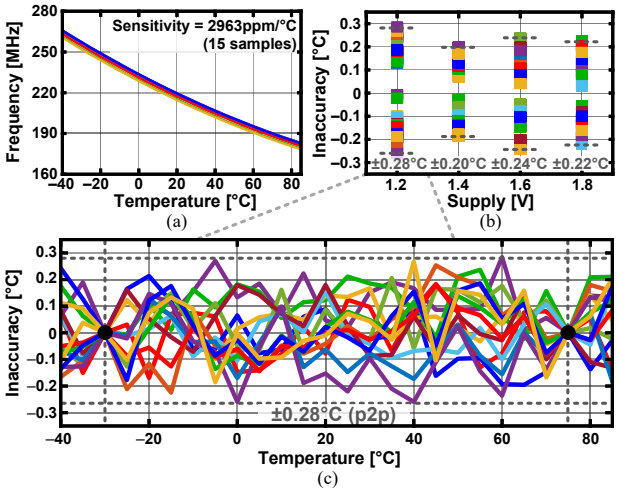

Fig. 9: (a) Measured frequency and sensitivity over temperature; 2pt-trimmed inaccuracy of 15 chips (b) across 1.2-1.8-V supply and (c) at 1.2-V supply.

the EC generates 10 times the VCO frequency to reduce quantization noise by combining transition edges of Φ_{FLL}.

Fig. 7(a) shows the proposed MP-SB ring VCO to optimize FLL energy. The proposed VCO exhibits low $f_{1/f,VCO}$ of a few tens of kHz, as high and low durations of Φ_{FLL} cancel each other thanks to its slope-boost nature [12], [13], as depicted in Fig. 7(b). Therefore, the MP-SB ring VCO inherently allows lower $f_{BW,FLL}$ as discussed in Section II-B, reducing the FLL energy consumption.

IV. Measurement Results

The proposed temperature sensor is fabricated in a 180-nm CMOS process as shown in Fig. 10(a). Fig. 8(a) shows the measured phase noise of Φ_{FLL}, indicating that the inevitable noise from sensing resistors in the FVC remains dominant (Fig. 8(c)). The noise from the other blocks is well-optimized thanks to the large K_{FVC} and K_{INT}. Meanwhile, since the proposed MP-SB ring VCO exhibits $f_{1/f,VCO}$ of 20kHz, $f_{BW,FLL}$

TABLE I: Performance summary and comparison with state-of-the-art designs.

		This Work	ISSCC'20 [3]	TCAS-II'23 [4]	ISSCC'25 [5]	ISSCC'24 [6]	ISSCC'26 [7]	ISSCC'23 [8]	JSSC'21 [10]
Method		FLL (Time)	FLL (Time)	FLL (Time)	FLL (Time)	RC Osc. (Time)	RC (Time)	SAR (Voltage)	ΔΣM (Voltage)
Process [nm]		180	65	65	28	3	2	65	180
Area [mm²] (Area Efficiency*)		0.0602 (1.85)	0.0088 (2.08)	0.0064 (1.51)	0.0041 (5.23)	0.0009 (100)	0.0006 (156)	0.0023 (0.54)	0.11 (3.40)
Supply [V]		1.2~1.8	0.95~1.2	0.85~1.25	0.7~0.9	0.65~0.85	0.6~0.77	0.6/1.0	1.4~2.0
Conv. Energy [nJ]		132	45	100	31.5	20	0.18	0.003	440
Conv. Time [ms]		1	1	2.5	3	1	0.012	0.02	8
Resolution [mK]		0.77	1.43	1.05	1.2	22.1	61	470	0.15
FoM** [fJ·K²]		78	92	110	45	9768	669	660	10
Temperature Range [°C]		–40~85	–30~90	–50~125	–40~125	–25~125	–40~125	–20~120	–55~125
Inaccuracy [°C]	1-pt Trim.	±0.50 (p2p)	±0.72 (p2p)	±0.64 (3σ)	±1.5 (3σ)	±1.0 (p2p)	±3.9 (3σ)	-	±0.4 (3σ)
	2-pt Trim.	±0.28 (p2p)	±0.32 (p2p)	±0.12 (3σ)	±0.2 (3σ)	±0.7 (p2p)	±0.5 (3σ)	–0.6/+0.7 (p2p)	±0.1 (3σ)
Samples		15	10	16	30	52	20	15	40

* Area Efficiency = Area [mm²] × (Process [μm])²

** Resolution FoM [J·K²] = Conv. Energy [J] × (Resolution [K])²

can be optimized as low as a few tens of kHz. Despite loop bandwidth optimization, the VCO, EC, and PG suffer from significant power and delay due to parasitic components in the 180nm process. Here, process scaling highly reduces the excessive power and delay, improving FLL energy efficiency and supply sensitivity.

Fig. 8(b) shows the measured Allan deviation and resolution. Since the EC effectively reduces quantization noise, a sub-mK resolution is achieved at 1-ms conversion time. Fig. 9(a) presents the measured FLL frequency ranging from 264MHz to 181MHz over –40 to 85 °C. Across a supply range from 1.2 to 1.8 V, the peak-to-peak (p2p) inaccuracy is ±0.28 °C after 2-point trimming at –30 °C and 75 °C as shown in Fig. 9(b)-(c) and the supply sensitivity is 6.1 °C/V.

Table I presents a performance comparison between this work and prior resistor-based temperature sensors [14]. The proposed MP-SB FLL structure inherently optimizes its performance, achieving both a superior FoM of 78 fJ·K² and the best-reported resolution of 0.77 mK among time-domain temperature sensors [1]–[7]. This work is also the smallest among sub-mK-resolution sensors and is process-scalable. When scaled from 180 nm to 28 nm, the estimated energy/area consumption from EC, PG, and VCO is highly reduced by 7×/55× under the same operating conditions as depicted in Fig. 10(c)-(d), reducing total energy/area by 2×/30×. As such, the reported energy and area of our design can be even further optimized, benefiting from its process-scalable structure.

V. Conclusion

This work presents a resistor-based temperature sensor employing a slope-enhanced MP-SB technique throughout the FLL blocks for noise and energy optimization. The proposed MP-SB FLL architecture ensures that only the inevitable noise and energy components from the sensing resistors remain dominant, achieving a state-of-the-art FoM of 78 fJ·K² and the best-reported resolution of 0.77 mK among time-domain sensors, broadening its applicability even to sub-mK temperature-compensated systems. Moreover, the proposed sensor is the smallest among sub-mK-resolution designs and exhibits strong scalability to advanced technology nodes, highlighting its suitability for on-chip local temperature sensing.

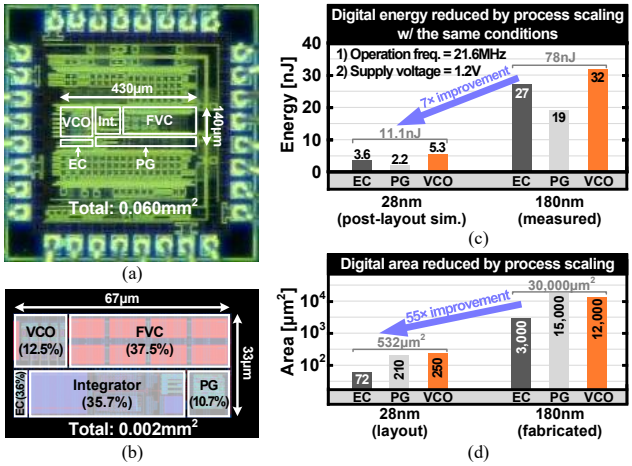

Fig. 10: (a) Die photo, (b) layout view scaled to 28-nm process, and projected reduction of (c) energy and (d) area by process scaling.

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