An 8GS/s 8b Time-Interleaved SAR ADC with Ping-pong Voltage/Time Domain Comparators and Metastability Correction

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***Abstract*—An 8 GS/s 8-bit time-interleaved SAR ADC with ping-pong voltage/time-domain comparators and metastability correction is presented. The mutually exclusive metastability behaviors in the voltage and time domains are exploited to correct both voltage- and time-domain metastability errors. In addition, ping-pong voltage/time-domain comparators with background calibration are employed to further enhance the conversion speed. The ADC achieves 42.7-dB SNDR and 56.3-dB SFDR at 8 GS/s at Nyquist, leading to 24.7 fJ/conv.-step Walden FoM and a metastability error rate below 10^{-10}.**

***Keywords*—Time interleaved ADC, SAR, time domain, metastability correction, background calibration**

I. Introduction

The SAR ADC is an energy-efficient architecture whose speed has been significantly increased through technology scaling and circuit innovations [1-7]. However, as the speed increases, the available comparison time is reduced, making the conversion more susceptible to metastability. As a result, the conversion may not complete correctly, leading to errors, as illustrated in Fig. 1(a).

To address metastability, the mutually exclusive metastability correction scheme has been proposed [8-9] as shown in Fig. 1(b), in which offset is injected into two channels to prevent simultaneous metastability, allowing a reliable decision to be selected from these two mutually exclusive paths. However, this approach doubles the hardware overhead and requires complex selection logic. Another solution is to employ a time-domain comparator to detect metastability by comparing the comparator's valid signal with a delayed comparator clock [1-2]. This allows the metastable SAR cycle to be identified and the SAR conversion to be terminated early. However, the time-domain comparator itself may also enter a metastable state. As shown in Fig. 1 (c), when the valid signal is close to the delayed comparator's clock, the metastability signal may be generated after the SAR has advanced to the next cycle, causing the indication to be misaligned and resulting in large conversion errors.

To overcome these issues, this work proposes a low-overhead algorithm that corrects both voltage- and time-domain metastability. Furthermore, ping-pong voltage/time-domain comparators with background calibration are employed to speed up the conversion. The ADC achieves 42.7-dB SNDR at 8 GS/s at Nyquist while consuming 22mW. With the proposed metastability correction, the metastability error rate is reduced to below 10^{-10}.

II. Proposed Metastability Correction

The proposed metastability correction algorithm is based on a key observation: voltage- and time-domain metastability

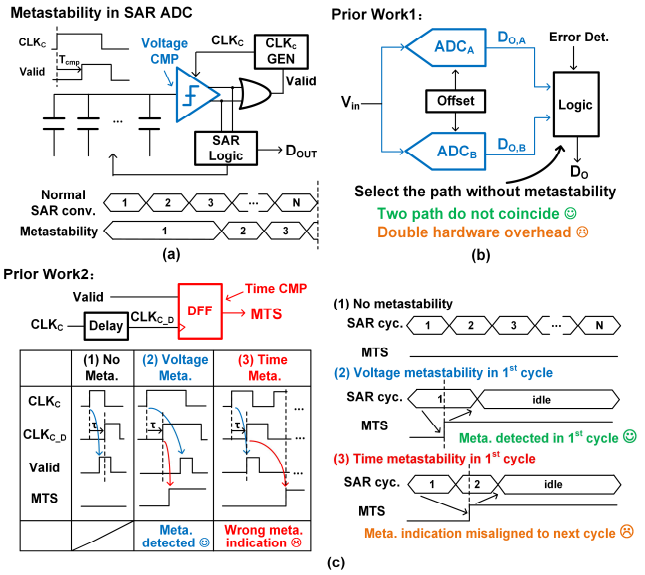

Fig.1. (a) metastability in SAR ADC (b) mutually exclusive metastability correction (c) metastability detector and its limitation

events are inherently mutually exclusive. As shown in Fig. 2, when the input signal is small, the voltage-domain comparator requires a long resolving time, while the time-domain comparator can rapidly make the correct decision, and vice versa. Exploiting this complementary behavior, the proposed algorithm is able to correct both voltage- and time-domain metastability with low hardware overhead, as illustrated in Fig. 3.

The metastability correction algorithm operates as follows: First, based on the SAR and metastability detector's outputs, both the voltage-domain output and the time-domain-assisted output can be reconstructed. When metastability is detected at the i-th SAR cycle, the time-domain reconstruction forces D_i to 0 and sets all lower bits to 1. Additionally, 1-bit resolution enhancement is achieved by setting the time-domain threshold to 1/2 LSB.

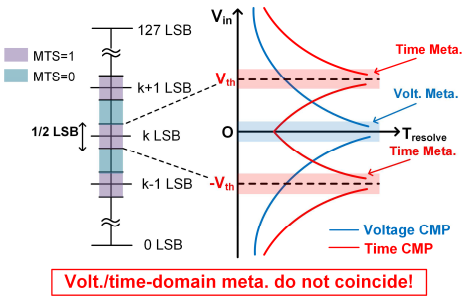

Fig.2. mutually exclusive metastability behaviors in voltage/time domains

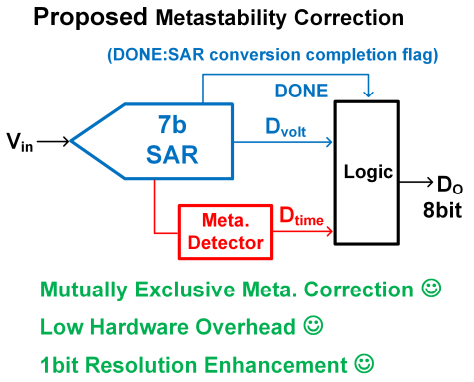

Fig.3. Proposed metastability correction

The reliable result is then selected as illustrated in Fig.4: when the ADC DONE signal (SAR conversion completion flag) is 0, indicating an incomplete SAR conversion, the time-domain output is used; when DONE is 1, the two reconstructed outputs are compared. If their difference exceeds a predefined threshold (8 LSB in this work, chosen considering the trade-off between metastability and noise), the voltage-domain output is chosen, indicating time-domain metastability; otherwise, the time-domain output is selected to achieve the resolution enhancement. In this way, large metastability errors from voltage and time domain can be corrected.

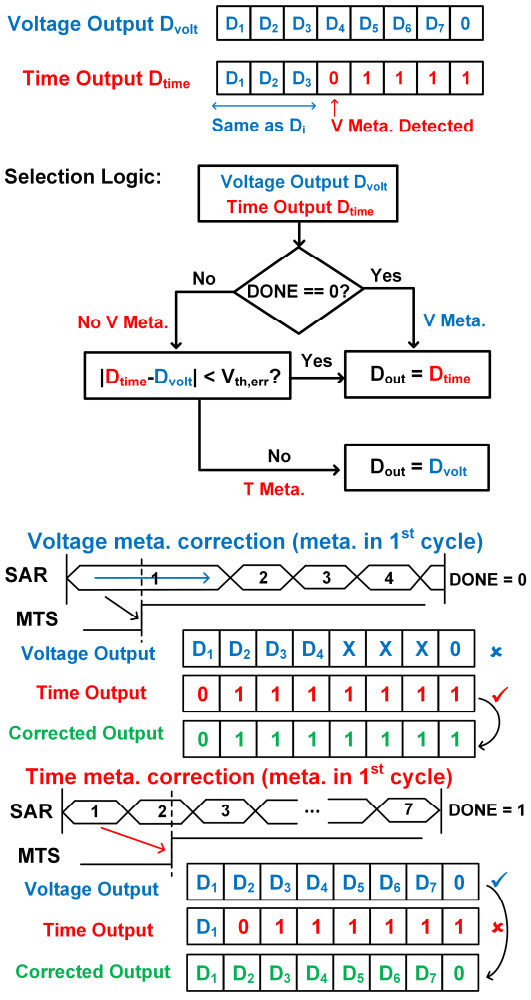

Fig.4. Reconstruction and selection logic

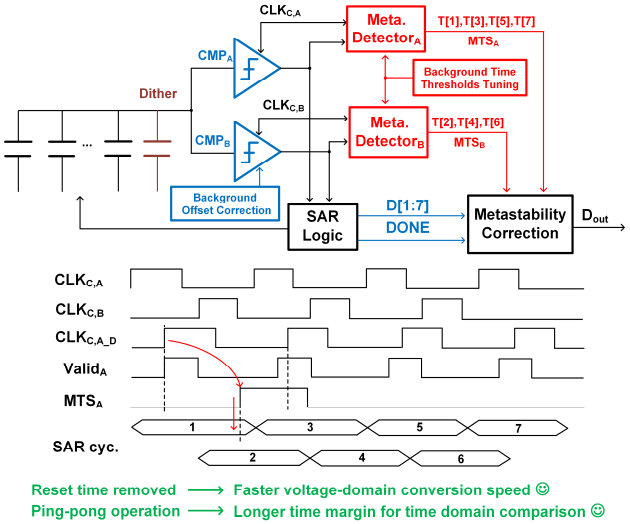

Fig.5. Proposed asynchronous SAR ADC with ping-pong voltage/time-domain comparators

III. Proposed SAR ADC

To further enhance the SAR conversion speed and extend the resolving time for metastability detection, an asynchronous SAR ADC with ping-pong voltage/time-domain comparators is proposed, as shown in Fig. 5. Two voltage-domain comparators operate alternately, removing reset time, accelerating SAR conversion [4-5]. In addition, since each metastability detector only monitors its corresponding comparator, the time-domain comparison is given one additional SAR cycle to fully resolve, reducing the time-domain metastability.

Fig. 6 shows the circuit implementation. The valid signal is generated by a balanced OR gate to ensure input symmetry, and the time-domain comparator is implemented using a DFF. The state machine is updated on each rising edge of CLK_C. When metastability occurs, the MTS signal rises, and the current state is sampled to identify the metastable SAR cycle.

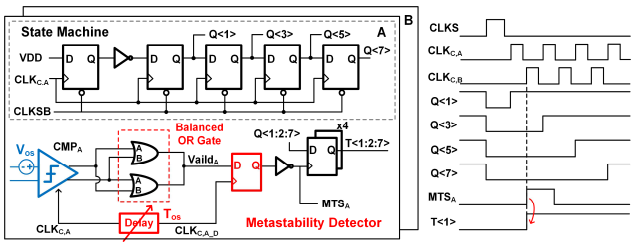

Fig.6. Circuit implementation

The offsets between ping-pong comparators degrade quantization performance, necessitating calibration. While voltage-domain offset is corrected in the background [5] by equalizing the last two voltage bits' probabilities via a charge pump, as shown in Fig.7, the time-domain offset exhibits greater PVT sensitivity. A statistical background calibration method is employed: the last two LSB bits' ideal metastability probability is theoretically known (e.g., 1/4 for the LSB and 1/8 for the second LSB, as shown in Fig. 8). A charge pump dynamically adjusts the delay cell to align measured probabilities with theoretical targets, ensuring PVT robustness. One-bit dither injection guarantees stable convergence across diverse input conditions.

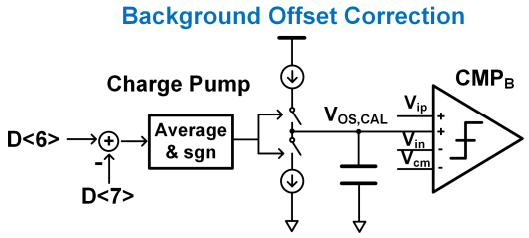

Fig.7. Background offset calibration

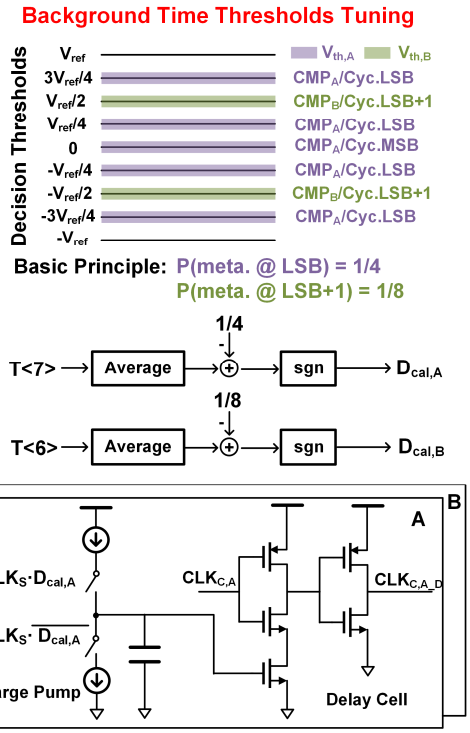

Fig.8. Background time thresholds tuning

IV. TI ADC Architecture

The 8x time-interleaved ADC architecture is shown in Fig. 9. An AC-coupled push-pull source follower input buffer drives 2 track-and-buffer stages, which feed buffered samples to 4 sub-ADCs. The track-and-buffer stage also uses a push-pull source follower for high energy efficiency and fast settling speed. Bottom-plate sampling with split capacitors is adopted: during sampling, the top plate is connected to the bias voltages $V_{BN,BUF}$ and $V_{BP,BUF}$, while the buffer's output is reset to V_{CM}, preventing channel crosstalk; after sampling, the bottom plate is connected to V_{CM}, and the signal is buffered to the ADCs. The clock generator receives an 8GHz external clock and generates CLK_S and CLK_{ADC} using divided clocks, as illustrated in Fig. 10. Clock skew is foreground calibrated by a 9-bit digitally controlled delay line (DCDL).

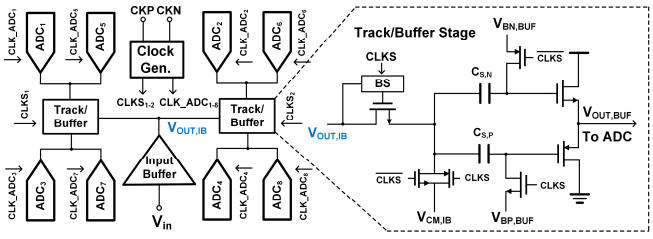

Fig.9. Time-interleaved SAR ADC architecture

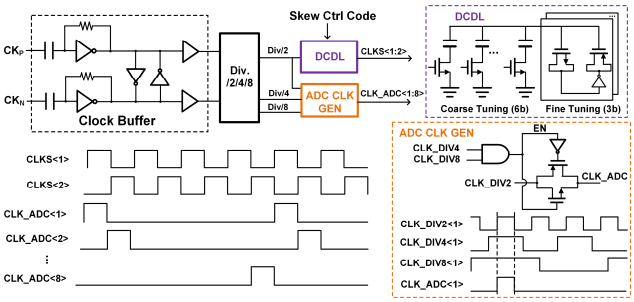

Fig.10. clock generation circuit

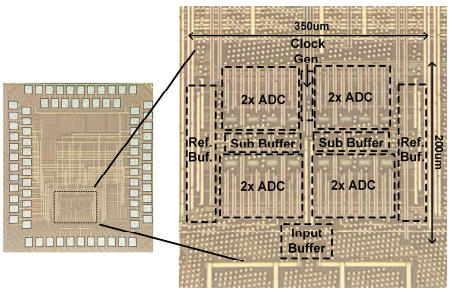

Fig.11. Chip micrograph of the proposed time-interleaved SAR ADC

V. Measurement Results

Shown in Fig. 11, the prototype time-interleaved SAR ADC is fabricated in a 28 nm CMOS process with an active area of 0.05 mm². Interleaved offset, gain, and time-skew mismatches are calibrated in the foreground, while the comparator offsets in voltage/time domains are calibrated in the background. Fig. 12 shows the measured output spectrum at a sampling frequency of 8 GS/s, decimated by 425. The ADC achieves 43.5/57.4 dB SNDR/SFDR at low input frequency and 42.7/56.3 dB SNDR/SFDR at Nyquist input, respectively. The measured dynamic range is 44 dB. SNDR variation remains within 1 dB across temperatures from −40 °C to 80 °C, ±5% supply-voltage variation, and five different chips, as shown in Fig. 13, demonstrating the effectiveness of the PVT-robust background calibration loop. The measured DNL and INL are −0.63/+0.67 LSB and −0.72/+0.68 LSB, respectively. Fig. 14 also shows the power breakdown, SNDR/SFDR versus input frequency, and the error probability for voltage-domain, time-domain, and metastability-corrected outputs, confirming that large time-domain errors are effectively mitigated.

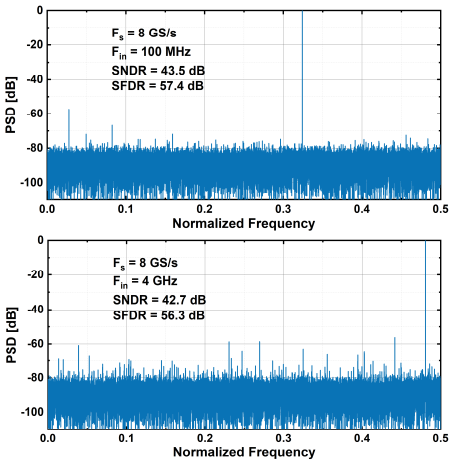

Fig.12. Measured ADC output spectrum at Fs=8GS/s with input frequency of 100MHz and 4GHz (decimated by 425)

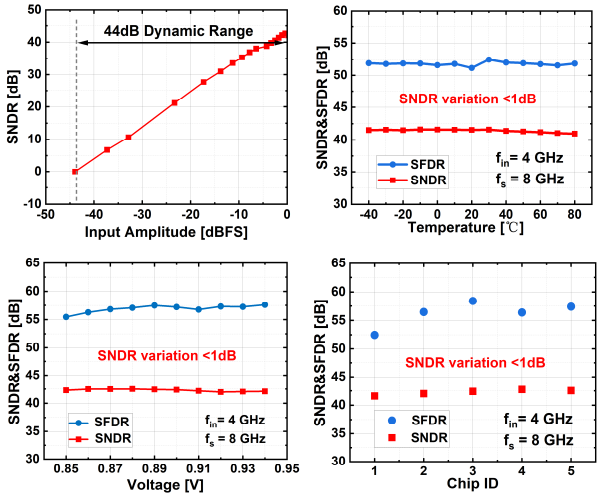

Fig. 13. Measured dynamic range, SNDR/SFDR variation among five chips, temperatures and power supply variations.

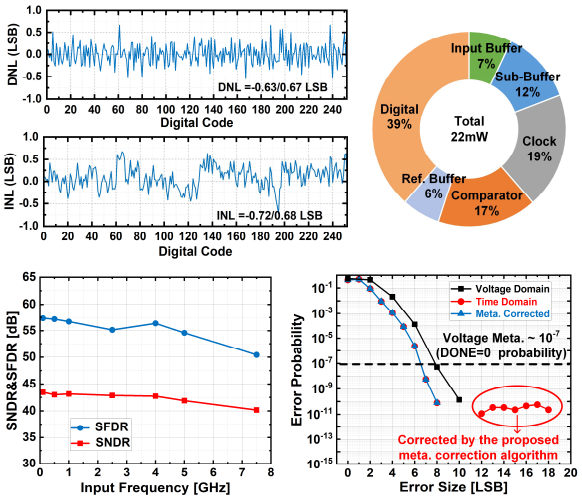

Fig. 14. Measured DNL/INL, power breakdown, SNDR/SFDR versus input frequency and error probability

VI. Conclusion

This paper presents an 8 GS/s 8-bit time-interleaved SAR ADC with ping-pong voltage/time-domain comparators and metastability correction. By exploiting the mutually exclusive metastability behaviors in the voltage and time domains, the proposed method effectively corrects both voltage- and time-domain metastability errors. Furthermore, ping-pong voltage/time-domain comparators with background calibration are employed to further enhance the conversion speed. Benefiting from these techniques, the proposed TI SAR ADC achieves 42.7-dB SNDR and 56.3-dB SFDR at Nyquist input with a metastability error rate below 10^{-10}, while consuming 22mW, including input buffers and reference buffers. This corresponds to 24.7 fJ/conv.-step Walden FoM. Table I and Fig. 15 summarize the comparison with state-of-the-art, highlighting the energy efficiency and effectiveness of the proposed metastability correction.

Acknowledgement

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TABLE I. Performance Summary and Comparison Table

	This Work	J. P. Keane ISSCC'17	C. -H. Chan ISSCC'15	Z. Liu ISSCC'25	M. Zhang ISSCC'20	E. Martens VLSI'21	Y. Tao ISSCC'25
Process	**28nm**	28nm	65nm	28nm	65nm	16nm	28nm
Architecture	**TI-SAR**	TI-SAR	TI-SAR	TDC	TI-TDC	TI-SAR	TI-Pipeline
Supply [V]	**0.9/1.1**	0.9/1.1/1.9	1.2	0.9	1	0.85	1
Sampling Rate [GS/s]	**8**	8	6	3	10	8	10
channel	**8**	16	4	1	4	8	2
Resolution [bit]	**8**	11	6	10	8	8	8
SNDR [dB]	**42.7**	49	30.13	47.2	40.1	42.7	41.7
SFDR [dB]	**56.3**	60.3	43.12	66.4	52.8	46	55.3
Area [mm^2]	**0.05**	0.184	0.09	0.032	0.095	0.023	0.009
Power [mW]	**22**	300	10.6	22.9	50.8	26	21.9
FoMs [dB]	**155.3**	150.2	144.6	155.4	150.0	154.6	155.3
FoMw [fJ/conv-step]	**24.7**	162.9	67.4	40.8	61.5	29.2	22.0
Metastability Reduction?	√	√	√	√	√	×	×
P_{Meta}	**<10^{-10}** *	<10^{-15}	<10^{-6}	<10^{-10}	~10^{-8}	-	-

*limited by finite measurement time (2 weeks) and slow data rate due to decimation

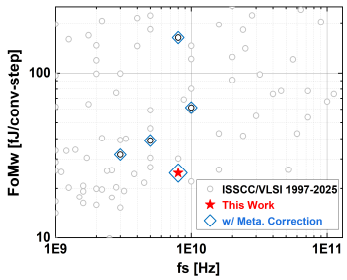

Fig. 15. Walden FoM comparisons with ISSCC/VLSI 1997-2025.

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