An FR2 Configurable Dual-stream Asymmetric 64-Element Phased Array Receiver

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***Abstract*—This paper presents a highly reconfigurable phased array receiver IC, which was used to implement a 64 dual-polarized antenna element array using 16 ICs with 45-nm CMOS PDSOI and 192 mW power dissipation per element. Each IC includes four RF beamforming front-ends per polarization, chip-to-chip bus interfaces and sliding-IF mixing stages. High reconfigurability via chip-to-chip interfaces allows for flexible forming of subarrays and easy scaling to larger arrays. Effect of array scaling is demonstrated showing the impact on EVM using 100 MHz 5G NR OFDM signal at 26.5 GHz reaching down to 5.0% EVM over a one meter over-the-air link. Receiver antenna pattern was also proven to work up to $\pm 45^\circ$ azimuth scanning range.**

***Index Terms*—Asymmetrical routing, chip-on-board, irregular antenna array, mmW interconnect, phase shifters, low noise amplifiers, receiver, phased array, RFIC.**

I. Introduction

Asymmetric or irregular phased arrays and their elements have been proposed and analyzed from various perspectives with respect to their scan and bandwidth properties [1], [2]. Thinned arrays have been shown to both steer the beams and perform spatial zeroing without additional phase control of individual elements even in relatively small array sizes [3]. However, most phased array transceivers are designed to support conventional phased array architectures with corporate i.e. symmetrical feeding networks with typical element distance of half the wavelength [4], [5]. The arrangement of antennas and integrated circuits depends on the carrier frequency and packaging choices, among other tradeoffs in implementation [6]. To combine the capabilities of phased arrays and MIMO communications, hybrid beamforming has been proposed. For a limited number of antennas, those can be implemented using a single chip solution as in [7], [8], but routing signals over multiple chips for complex, irregular structures is difficult.

To avoid issues related to large off-chip feeding networks in terms of losses and area needed in dense 2D panels or to avoid 3D packaging, an IC architecture supporting chip-to-chip (C2C) interconnects at carrier or other frequencies for scalable phased arrays has been proposed in [9]. This paper describes a new version of the transceiver (TRX) chip that is integrated for the first time into a mmW antenna array using chip-on-board (COB) assembly on a Panasonic's Megtron 7 substrate with 64 dual-polarized patch antennas [10]. The main focus in the paper is on the system level performance of the asymmetrically routed phased array receiver (RX) demonstrating only a small loss in performance due to beam squint even in large steering angles. A companion paper on the implementation of transmit (TX) array [11] with the same platform indicates similar observations with different feeding network examples with decent output power in over-the-air (OTA) experiments.

This paper is organized as follows: Section II describes the transceiver architecture, and Section III gives details on the new receiver circuits, specifically the low noise amplifier (LNA), compared with the earlier publication. The experimental results are given in Section IV before the conclusions.

II. Transceiver Architecture

The system platform is shown in Fig. 1. Transceiver IC is shown in Fig. 1(a). The IC contains eight RF-front-ends, two mixing stages (sliding IF), inputs and outputs for mmWave, IF, BB and LO buses, which together with PCB routing result in asymmetrical electrical lengths to the antenna elements.

The RF front-ends are designed to support two independent streams connected to vertical (V) and horizontal (H) polarized antennas. The front-ends also include cross connections and combiners/splitters to support hybrid beamforming i.e. forming beams in two directions from same antenna elements. Signals to/from the front-ends are distributed/combined with an active splitter/combiner network. The mmWave routing matrix at the center of the chip routes and switches signal paths to mmWave bus blocks and mmWave/IF mixers. Respectively, the IF routing matrix routes and switches signal paths to the IF and BB circuits. The IC is shown in Fig. 1(b). The IC is implemented on 45-nm CMOS partially depleted silicon-on-insulator technology from GlobalFoundries and the total chip area is 35.2 mm^2.

8×8 antenna array architecture implemented on 16-layer PCB is show in Fig. 1(c) and the PCB photograph on (d), respectively. 16 flip-chip packaged ICs are connected with differential buses operating at multiple frequency domains: horizontal connections are made with mmWave buses and vertical connection with IF buses. The mmWave bus consists of two bidirectional buses whereas the IF buses are routed unidirectionally on PCB. The first two columns are routed "down" and the latter two columns "up".

Local oscillator (LO) signals are daisy chained vertically from one chip to the next for each column in the array. The LO

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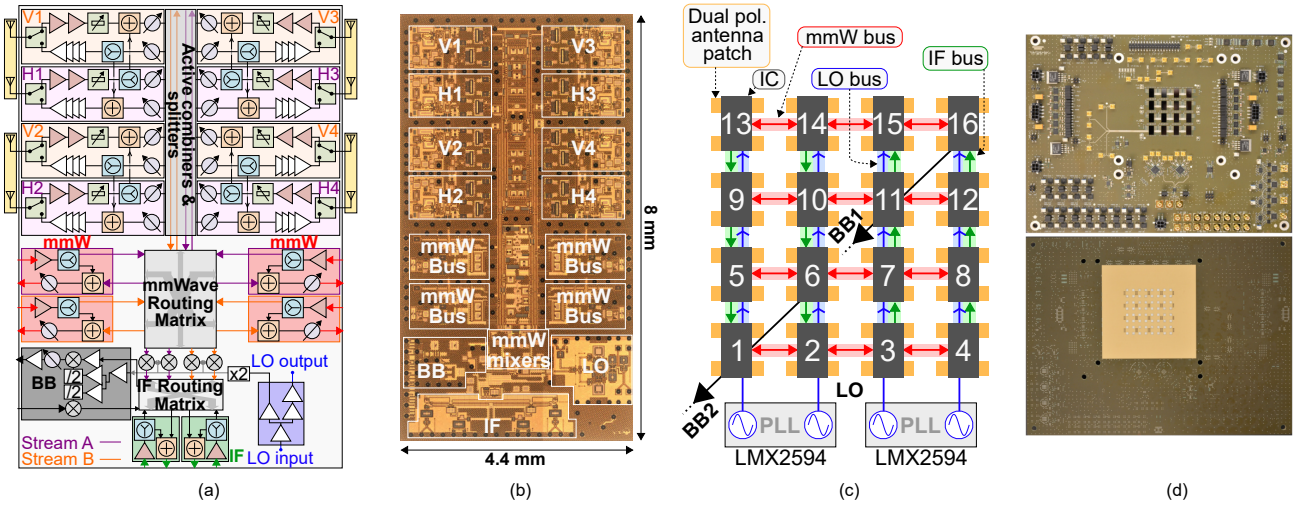


Fig. 1. (a) Block diagram and (b) micrograph of transceiver chip with 2×4 transmit/receive TDD front-ends, active splitting/combining network, mmWave, IF, BB and LO bus interfaces, mixers and routing/switching matrices. Assembled 8×8 element panel on Panasonic Megtron 7 with (c) block diagram illustrating the routed buses and (d) photographs of the PCB front and backside.

is generated with LMX2594 frequency synthesizer ICs which provide two differential outputs per unit. Differential IQ baseband signals are connected diagonally and converted to single-ended signals on the PCB using four dual-channel LTC6419 amplifiers. After that, they are combined via eight ADG901 switches and four resistive EP2RKU+ power combiners: ICs 1 and 6 to BB2, and ICs 11 and 16 to BB1, enabling both combined or individual BB measurement.

Example routing configurations used in this paper are shown in Fig. 2 for one antenna element (N=1), one antenna row (N=8), four antenna rows (N=32) and for the full 64-element array (N=64). The output in receive mode is measured from IC1. LO is active only for the first column of ICs (1, 5, 9 and 13) where frequency conversion is needed to mix the mmWave signals to the vertically routed IF bus and at IC 1 to the BB.

III. Low Noise Amplifier

In the previous iteration of the transceiver, the low-noise amplifier (LNA) chain inside the RF front-end consisted of three gain stages providing over 40 dB gain [9]. This resulted in limited linearity. In the current version of the transceiver chip, the third stage of the LNA has been replaced with an attenuator shown in Fig. 3. The first two stages are single-ended input cascodes and the output load transformer X1 converts the single-ended signal to differential. The attenuator was implemented with a two-bit variable capacitor bank which tunes the front-end gain by approximately 9 dB with a small impact on the frequency response shape. From the antenna port to the output of the phase shifter, the simulated noise figure of the RF front-end is 5.1 dB and peak gain 31.5 dB, input preferred compression point of -32.3 dBm and 4.2 GHz bandwidth (15.8% relative).

IV. Measurements

The RX measurements were done inside an anechoic chamber with an OTA setup illustrated in Fig. 4. The setup includes

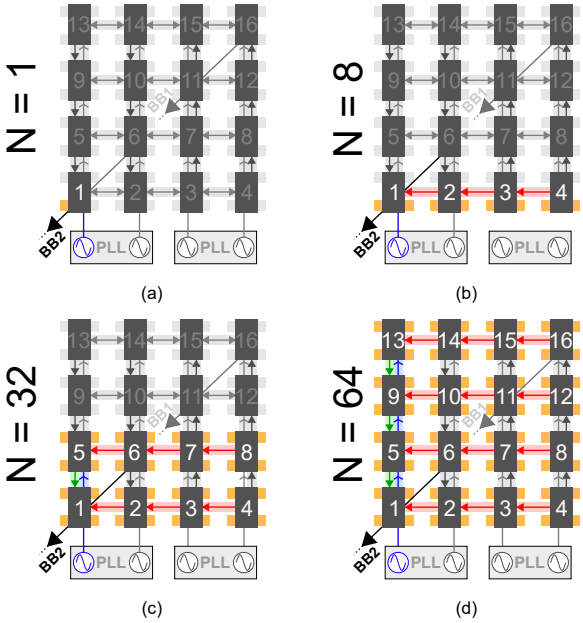


Fig. 2. Signal routing configurations for (a) one, (b) eight, (c) 32 and (d) 64 antenna elements showing the use of LO (blue), mmWave (red), IF (green) and baseband (black) buses.

a fixed orientation dual-polarized antenna (LB-SJ-50500) and the phased array platform on a rotating table which is used to measure beam patterns. In this paper, only vertically polarized signals paths were measured. Test signals are generated in an arbitrary waveform generator (ARB) (Keysight M8190A) and upconverted to RF frequencies with a signal generator (Keysight E8267D) and transmitted to the air with the antenna. Baseband I/Q outputs of the phased array are measured with a 16 GSa/s oscilloscope (Keysight MXR058A).

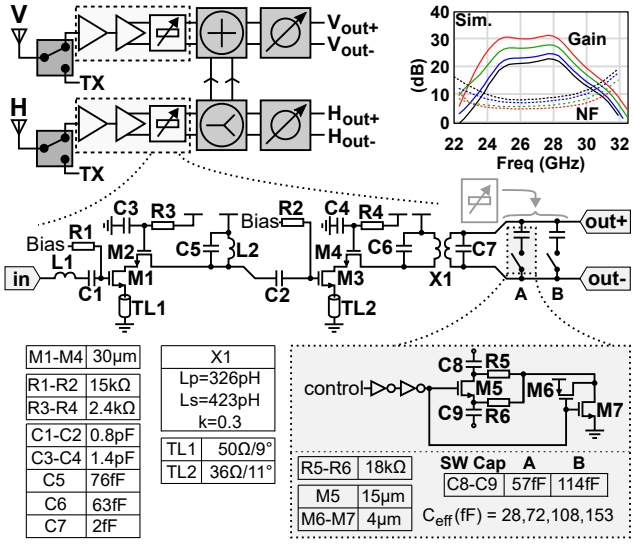


Fig. 3. LNA schematic and simulation of attenuator stage sweep.

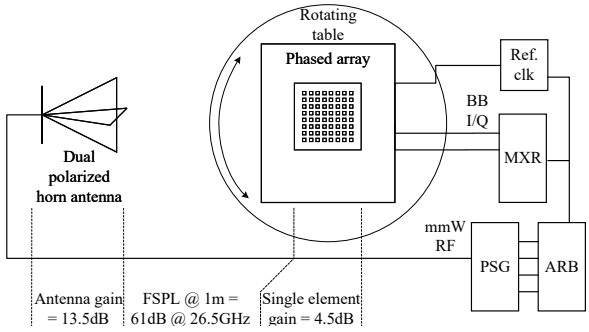


Fig. 4. OTA measurement setup.

A. Array Calibration

Large antenna arrays require careful phase and amplitude control for individual RF paths to antenna for precise beamforming. To achieve this, the array is calibrated in three stages. In the first stage, the I/Q constellations of vector modulator based phase shifters in RF front-ends are characterized one-by-one [12]. In the second stage, the gains from antennas to the baseband output are characterized with maximum gain and minimum noise biases and then adjusted to a common gain level with the RF front-end with bias and attenuator controls. This second stage is illustrated in Fig. 5(a) showing maximum gain one-tone power sweeps at 26.5 GHz and equalized gain configurations in Fig. 5(b). In the third stage, phase differences between antenna paths are calibrated. First, each 8 element antenna rows are calibrated with the search based phase calibration method [13]. Then, the phases between rows are calibrated by enabling rows one-by-one and rotating the phases of all antenna elements in the row compared with already activated rows and selecting the phase that maximizes the receiver gain. Measured RF frequency responses of one chip for four receiver paths with maximum gain biases (V1-V4) are shown in Fig. 5(c). The 3 dB bandwidth is approximately 25.2–26.9 GHz. The reported gain includes the path from the IC RF input to the IC BB output.

TABLE I
COMPARISON OF RECENT MMWAVE PHASED ARRAY RECEIVERS.

	This work	TMTT'26 [14]	TMTT'24 [15]	TMTT'23 [4]
Technology	**45nm CMOS SOI**	90nm SiGe	22nm CMOS SOI	180nm SiGe
Freq (GHz)	**25.2-26.9**	3-28	23-30, 36-40	15-57
Feed-architecture	**Irregular**	Corporate	Corporate	Corporate
Pdiss per path (mW)	**192**	150	55	200
# of antennas per pol.	**64**	16	4	64
Polarization	**dual-pol. linear**	dual-pol. linear	single, linear	single
Beam steering (°)	**±45**	±55	±40	±60
Gain (dB)	**37**	20...30	20.5	22
NF (min./typ.) (dB)	**3.8/8.4**	3.7/-	6/-	4.7/-
ICP,elem (dBm)	**-45**	-32...-24	-25	-28
Modulation	**OFDM 64QAM 100Mbaud**	SC 64QAM 400Mbaud	SC 64QAM 500Mbaud	OFDM 256QAM 400Mbaud
OTA EVM (%)	**5.0**	0.9-1.8	8.3	2.0

B. EVM and Beam Pattern Measurements

The beam patterns were tested by sweeping the steering azimuth angle from -45 to +45 degrees. Normalized gain curves at 26.5 GHz with 64-elements are shown in Fig. 6(a). Maximum sidelobe gain levels are below -10 dB for all steering angles. Wide radiation pattern of an antenna element is expected to support even wider beamsteering ranges.

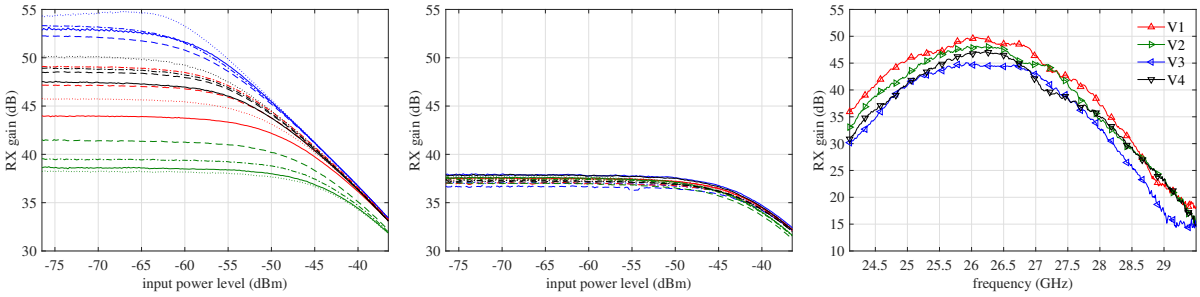
EVM measurements were performed with 5G new radio (NR) orthogonal frequency division multiplexing (OFDM) 64-QAM signals with 100 MHz bandwidth. EVM curves for multiple antenna array configurations with boresight and +45° steering angle are shown in Fig. 6(b). As the number of antenna elements is increased, the gain of the array increases as expected from coherent combining, which enables longer link ranges. The minimum EVM itself does not improve, however. Constellation of the lowest achieved EVM of 4.96% with 64 elements active is also shown in Fig. 6(c).

This receiver array is compared to other recent phased array receivers at FR2 frequencies in Table I. Power dissipation and noise figures are comparable to other works, especially when considering that the chips include also interface buses and mixers. Future work includes testing with wider beam scanning angles and with broader modulation bandwidths.

V. CONCLUSION

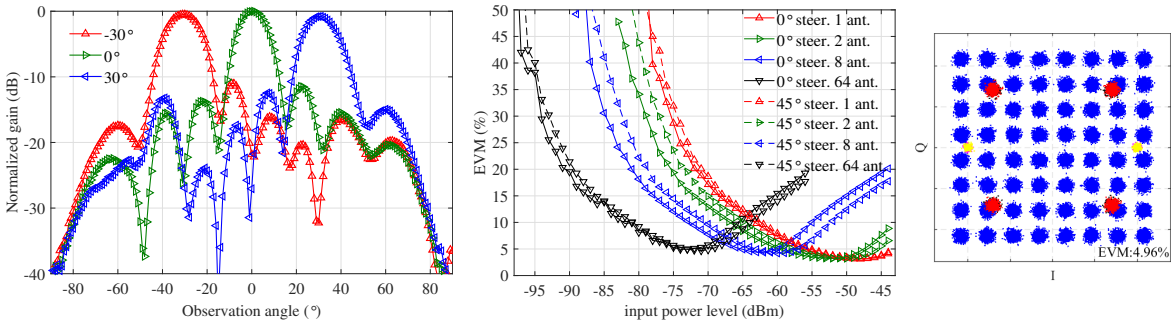
Irregular arrays provide a highly flexible alternative for constructing phased arrays. This work demonstrates the performance of a complete platform with 16 mmW IC's that provide C2C interconnects for configuring an antenna array panel. The receiver routes mmW or IF signals over several IC's with capability to sum the signal using any of the antenna elements. It is possible, but not demonstrated here, to form several data streams using a flexible selection of antenna elements using two independent mmW C2C interconnects.

The array is tested using all 64 antenna elements with corner chip feeding representing the worst case scenario for the beam



(a) (b) (c)

Fig. 5. Power sweeps of 16 receiver paths before (a) and after (b) amplitude calibration. (c) Frequency responses for four paths of one IC.



(a) (b) (c)

Fig. 6. (a) Radiation patterns with 64 antenna elements array scaling, (b) EVM and (c) constellation of the best EVM achieved with 64 elements.

squint. Despite moderate noise figure and linearity, when all chips are normalized to equal gain in the panel, a good EVM performance was achieved and the dynamic range can be scaled based on the number of active antenna front ends in the platform. A large steering angle only slightly degrades the EVM, giving solid proof of the beam steering capability in a highly irregular feeding network.

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