A 2.8-NEF 130-mV/140-V DM/CM Artifact-Tolerant Biopotential Amplifier for Two-Electrode Recording System Using Signal Folding

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***Abstract*— This paper presents a motion-artifact-tolerant analog front-end (AFE) for two-electrode biopotential recording to improve dynamic range (DR) in the low-frequency region where motion artifacts dominate. The proposed AFE employs a dual-slope artifact-tracking (DSAT) loop based on signal folding to confine large-amplitude low-frequency inputs within the linear operating range, enabling fast settling without requiring excessive bandwidth or comparator speed. To enhance robustness against common-mode interference (CMI), a common-mode-stabilized dual-bias (CMSD) OTA is introduced to regulate bias currents and extend the input common-mode range (ICMR). Fabricated in a 110-nm CMOS process, the prototype achieves a low-frequency DR of 130 mV$_{PP}$, a CMI tolerance of up to 140 V$_{PP}$, and a total CMRR of 101 dB while consuming 4.71 µW with an NEF of 2.8.**

***Keywords*—Analog front-end (AFE), biopotential amplifier, common-mode interference (CMI), wearable biomedical sensor, motion-induced artifacts, motion artifacts (MA).**

I. Introduction

While wearable two-electrode ExG systems offer superior user comfort, they are highly vulnerable to both differential-mode (DM) and common-mode (CM) artifacts. As illustrated in Fig. 1, motion-induced artifacts, stemming from electrode mismatch and variations in electrode–tissue impedance, appear as large low-frequency DM components. Simultaneously, power-line coupling introduces substantial CM interference. Crucially, these artifacts overlap with the ExG signal bandwidth, rendering conventional filtering ineffective for suppression.

In particular, MAs are concentrated in the low-frequency band and can easily exceed the DR of the analog front-end (AFE), leading to output saturation. This indicates that the performance bottleneck of the AFE is not dictated by the overall signal bandwidth, but rather by its tolerance to large-amplitude low-frequency interference. In addition, under extreme CMI conditions exceeding 100 V$_{PP}$ [1], even state-of-the-art T-CMRR may allow CM-to-DM conversion to generate residual artifacts on the order of several millivolts, further disturbing the input and exacerbating AFE saturation.

To suppress significant DM interference caused by motion and Z_{ETI} mismatch, prior works employed precise input charge subtraction or digital-assisted loop (DAL) [2]–[4]. However, the subtraction schemes in [2] and [3] increase system complexity or power consumption, as they necessitate real-time artifact estimation and high-speed transient tracking. While the DC-feedback-based approach in [4] prevents saturation by applying negative feedback to the input, it requires frequent, high-resolution comparisons to settle large DC artifacts, leading to slow settling and increased power consumption. Furthermore, these approaches do not account for the spectral concentration of MAs in the low-frequency region, resulting in inefficient DR utilization.

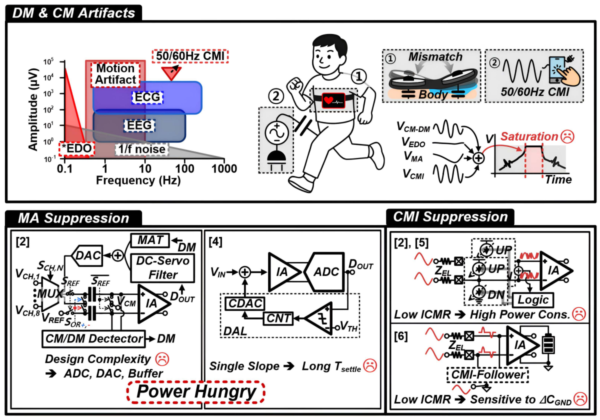

Fig. 1. Design challenges of wearable devices and prior art for motion artifact (MA) and common-mode interference (CMI) suppression.

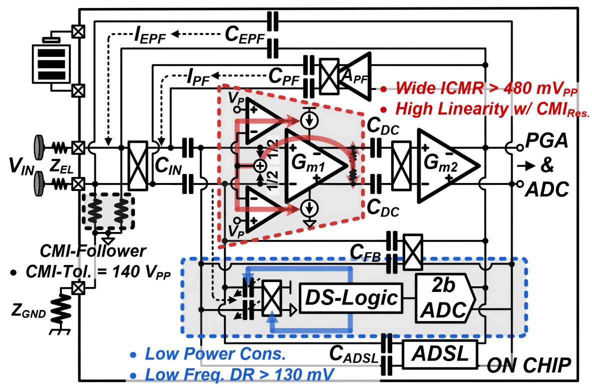

Fig. 2. Proposed artifact-tolerant AFE architecture.

To enhance CMI tolerance, the CMI canceling (CMIC) [2], pseudo RLD [3], CM suppression loop (CMSL) [5], and CMI-Follower [6] have been introduced. While CMIC, CMSL and pseudo RLD can improve tolerance by maintaining the input CM within the allowable voltage swing of the instrumentation amplifier (IA), they incur a power penalty proportional to the interference level. Although the CMI-Follower mitigates this power overhead, it remains sensitive to motion-induced variations in the parasitic capacitance to earth (C_{GND}) [7], causing residual CMI and subsequent CM-to-DM conversion.

To address these challenges, we propose a DSAT loop that confines large-amplitude low-frequency DM artifacts within the linear operating range using a rapid and power-efficient signal-folding scheme. By leveraging the spectral

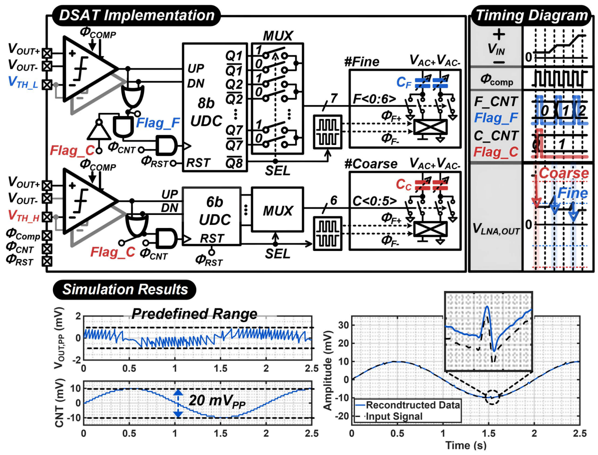

Fig. 3. Proposed DSAT architecture, timing diagram, and simulation results.

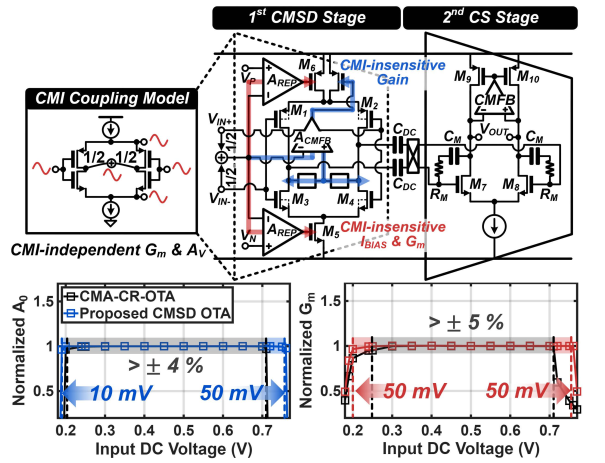

Fig. 5. Proposed CMSD OTA schematic and simulated G_m and A_0 comparison with CMA-CR-OTA [6].

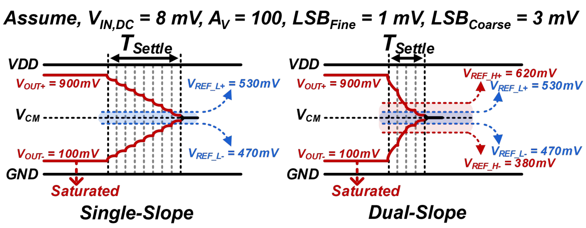

Fig. 4. Output waveform comparison for single- and dual-slope operations.

characteristics of MAs, the proposed approach avoids unnecessary wideband DR extension and improves power efficiency. Furthermore, a CMSD OTA is introduced to maintain stable bias conditions under residual CMI, ensuring robust operation against variations in C_{GND} and achieving superior CMI tolerance compared to conventional AFEs.

II. Proposed Artifact-Tolerant Biopotential AFE

Fig. 2 depicts the proposed AFE with the DSAT loop and CMSD OTA. The DSAT loop monitors the output using a 2b analog-to-digital converter (ADC) and bidirectionally folds the input signal to ensure linear operation within the allowable DR. To achieve high CMI tolerance in two-electrode configurations, the proposed AFE incorporates the CMI-Follower architecture [6] and introduces a CMSD, which suppresses motion-induced residual CMI effects.

A. DSAT Loop

Fig. 3 shows the architecture and simulated waveforms of the proposed DSAT loop. The low-noise amplifier (LNA) output is roughly quantized by comparators with threshold levels V_{TH_L} and V_{TH_H}. When the signal exceeds V_{TH_H}, a 6-bit up/down counter (UDC) is activated to rapidly track large excursions. Conversely, an 8-bit UDC operates when the output remains between V_{TH_L} and V_{TH_H} to ensure precise settling. The MSB indicates the output polarity and controls the chopping clock phase of the capacitor bank, enabling bidirectional signal folding back into the linear range. To minimize dynamic power and capacitor crosstalk, the DSAT loop is disabled, and the bottom plate of the dual-slope capacitive digital-to-analog converter (CDAC) is connected to ground when the LNA output remains within the fine range.

The DM artifact tolerance is determined by the DSAT loop operating speed, governed by the LSB and the clock frequency (Φ_{COMP}) of the dynamic comparator. Since this Φ_{COMP} is fundamentally limited by the LNA bandwidth, the DSAT loop is optimized to achieve a power-efficient design that meets the required DR specifically within the target low-frequency range. This frequency-selective DR extension prevents unnecessary power consumption in high-frequency regions where MAs are negligible. Simulation results in Fig. 3 verify the operation of the proposed DSAT loop under 0.5 Hz, 20 mV_{PP} sinusoidal baseline drift, emulating moderate MA. The reconstructed signal, obtained by combining the analog output and digital count, faithfully restores the input waveform, with a slight offset due to gain mismatch. As shown in Fig. 4, the dual-slope operation provides significantly faster settling for large-scale excursions compared to conventional single-slope architectures. While single-slope tracking either requires excessive bandwidth or suffers from slow recovery, our dual-slope scheme rapidly restores the signal via coarse steps and fine-tunes the residual error, achieving high-speed tracking without requiring high-speed comparators.

B. CMSD OTA

Fig. 5 illustrates the proposed CMSD OTA along with its simulated G_m and A_0 for a performance comparison with the CMA-CR-OTA [6], which utilizes a current-reuse OTA (CR-OTA) [8] for high noise-power efficiency. Despite the advantages of the CMI-Follower, residual CMI can disturb the bias condition, degrading linearity and limiting overall CMI tolerance. To mitigate this, the proposed CMSD OTA incorporates a replica sensing pair that monitors the input CM voltage to indirectly track the V_{DS} of the current sources.

When the headroom of the current sources becomes insufficient due to CM fluctuations, the CMSD mechanism dynamically adjusts the V_{GS} to maintain a constant bias current, thereby compensating for variations in V_{DS}. This effectively increases the output impedance of the current sources, with the enhancement factor proportional to the gain of the auxiliary replica amplifier (A_{REP}) and the intrinsic gain of the input transistors. Moreover, a CM feedback loop senses the output CM level and compares it with the input CM to regulate the CM current, stabilizing the V_{DS} of the input transistors. Consequently, the allowable ICMR is primarily

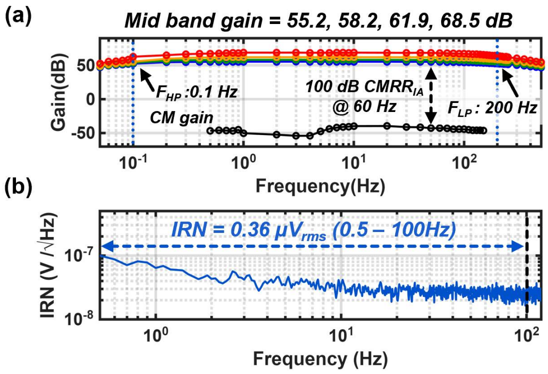

Fig. 6. Measured (a) frequency responses, (b) input-referred noise (IRN).

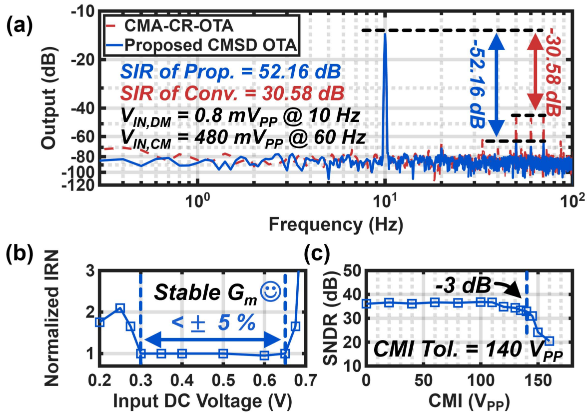

Fig. 7. Measured (a) output spectra: Comparison between the proposed CMSD OTA and CMA-CR-OTA [6], (b) input-referred noise (IRN) versus input DC voltage, and (c) common-mode interference (CMI) tolerance.

governed by the input transistor's V_{GS}, rather than being limited by the headroom of the current source. Simulation results confirm that, with a ±5% variation limit, the linear range of the G_m is extended by approximately 100 mV, while the DC gain range is improved by 60 mV. By stabilizing the PMOS current source and extending the ICMR, the CMSD OTA provides a significant design margin against variations in C_{GND}, ensuring robust performance in non-ideal wearable environments.

III. Measurement Results

The prototype AFE was fabricated in a 110-nm CMOS process. Fig. 6 presents the measured frequency response and input-referred noise (IRN). The mid-band gain is configurable from 55.2 to 68.5 dB, with a high-pass corner frequency of 0.1 Hz determined by the analog DC servo loop. A 100-dB intrinsic CMRR is achieved at 60 Hz with a gain of 55.2 dB, and the integrated IRN from 0.5 to 100 Hz is 0.36 µVrms, yielding a noise efficiency factor (NEF) of 2.8. The IRN was measured with the CDAC in the DSAT loop deactivated and connected to ground.

Fig. 7 evaluates the performance of the proposed CMSD OTA. As shown in Fig. 7(a), under a 480-mV_{PP} CM input and a 0.8-mV_{PP} DM input, the CMSD OTA provides a 22-dB improvement in signal-to-interference ratio (SIR) compared to the CMA-CR-OTA. Fig. 7(b) shows that the IRN remains stable within ±5% over a 350-mV input DC voltage range. Crucially, the CMSD OTA enhances the CMI-Follower's robustness, achieving a measured CMI tolerance of 140 V_{PP}, as depicted in Fig. 7(c). This result aligns with the theoretical expectation that a 100-mV ICMR extension improves CMI tolerance by 10 V_{PP} and 5 V_{PP} for C_{GND} of 1 pF and 2 pF, respectively, significantly outperforming [6].

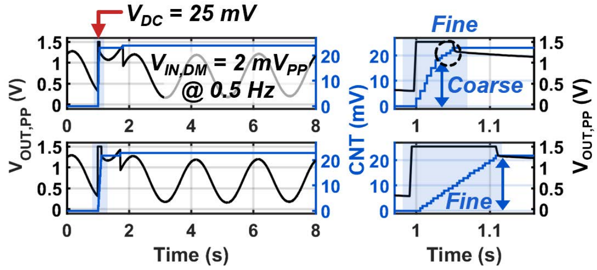

Fig. 8. Measured step responses of the proposed DSAT loop (top) and single-slope (SS) operation (bottom).

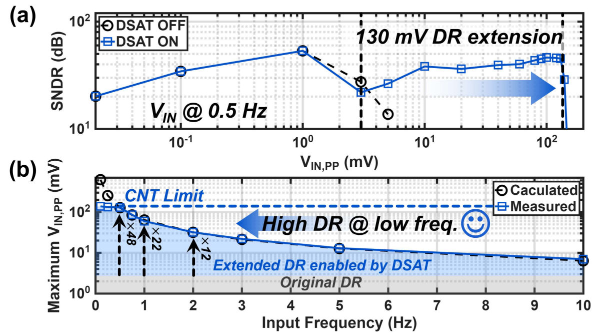

Fig. 9. Measured (a) SNDR versus input amplitude for a 0.5 Hz sinusoidal input and (b) maximum $V_{IN,PP}$ for peak SNDR versus input frequency.

The step-response settling behavior with a 25-mV pulse input in Fig. 8 demonstrates that the proposed DS operation achieves approximately 2× faster settling compared to the SS operation by rapidly restoring the signal via coarse feedback before fine-tuning. Fig. 9 presents the measured DR performance. The proposed AFE maintains an SNDR above 22 dB for a 0.5-Hz sinusoidal input up to 130 mV_{PP}, as plotted in Fig. 9(a). Fig. 9(b) illustrates the maximum allowable $V_{IN,PP}$ for peak SNDR as a function of frequency, along with the calculated $V_{IN,PP}$, demonstrating the frequency-dependent DR extension. The measured results show a good agreement with the calculated values. Even under intensive activities such as jogging and band exercise [3], [9], MAs are predominantly concentrated below 2 Hz. Therefore, prioritizing DR in the low-frequency range is essential for robust operation. The DR improvement at low frequencies is limited by the finite CNT bit, while the achieved DR remains sufficient for practical MA conditions.

To validate practical performance, *in vivo* ECG signals were recorded under harsh conditions, as shown in Fig. 10. Despite intentional MAs from vigorous arm movements and high CMI through body coupling, the DSAT loop effectively confines the output within a predefined linear range while compensating for DM artifacts, enabling stable biopotential acquisition. Fig. 11 shows the chip micrograph, and Table I summarizes the performance comparison with state-of-the-art AFEs. The proposed AFE achieves the highest CMI tolerance up to 140 V_{PP} and robust MA tolerance, while maintaining a T-CMRR of 101 dB under 5% Z_{ETI} mismatch and the lowest NEF of 2.8.

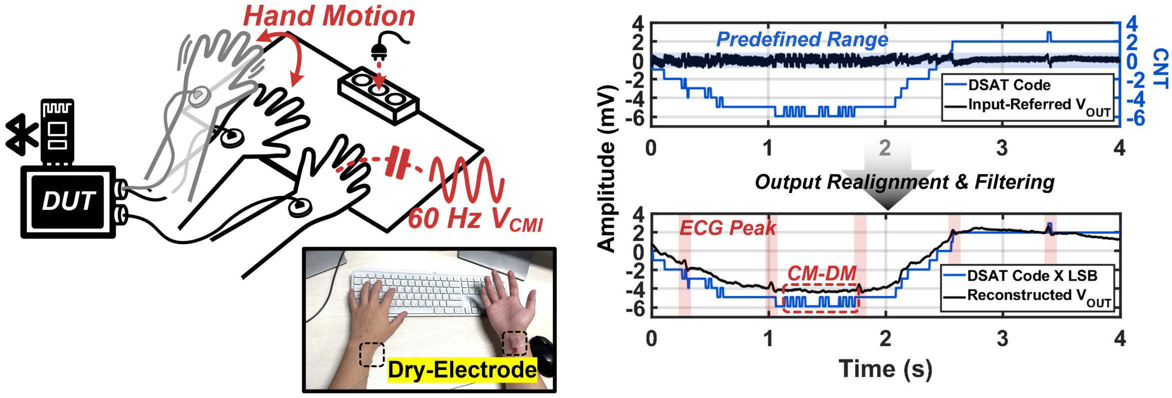

Fig. 10. Measured biopotentials under motion artifacts (MAs) and common-mode interference (CMI).

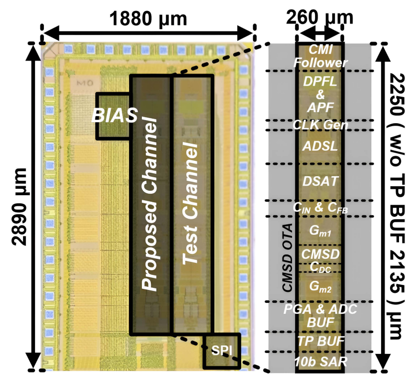

Fig. 11. Chip micrograph.

IV. Conclusion

This paper presents an MA- and CMI-tolerant AFE specifically optimized for two-electrode biopotential recording systems. By employing a DSAT loop based on signal folding, the proposed AFE confines large low-frequency DM artifacts within the linear operating range. This approach enables fast settling without requiring excessive system bandwidth or high-speed comparators. In addition, the CMSD OTA improves robustness against residual CMI by stabilizing internal bias conditions and extending the ICMR.

Fabricated in a 110-nm CMOS process, the prototype AFE consumes 4.71 µW and achieves a CMI tolerance of 140 V_{PP}, a T-CMRR of 101 dB, and a low-frequency dynamic range of 130 mV_{PP}, while maintaining an NEF of 2.8. These results validate that the proposed AFE ensures reliable and high-fidelity biopotential acquisition even under severe motion and interference, making it a highly suitable solution for next-generation wearable healthcare devices.

Acknowledgment

This work was supported in part by Samsung Electronics Co. Ltd (IO260312-15863-01), IITP grant (RS-2025-02217613) funded by the Korea government (MSIT), and the Sogang University Research Grant of 202410029.01.

TABLE I. Comparison with State-of-the-Art AFEs

Parameters	This Work	JSSC 2022 [5]	VLSI 2023 [2]	TBCAS 2025 [3]	JSSC 2025 [6]
Process [nm]	110	180	180	180	110
Area [mm²]	0.556 ^{B}	0.878 ^{B,C}	0.253 ^{B}	6.6 ^{A}	0.468 ^{B}
Supply [V]	1 / 1.5	1.2	1.8	1.2	1 / 1.5
Gain [dB]	55.2 – 68.5	54	25.8	20 – 47	54.5 – 67.9
$CMRR_{IA}$ [dB]	100	N/A	N/A	120	108
Tol. to MA	O	X	O	O	X
Power/Ch [µW]	4.71 ^{D}	43.4	22.19	44	4.6 ^{D}
CMI Tol. [V_{PP}]	140	18	22	40	133
T-CMRR [dB]	101	> 110	110	92	102 / 90.5
ETI Mismatch	5%	30%	73.2 kΩ	29.1 kΩ	5% / 30%
IRN [$µV_{rms}$] (BW) [Hz]	0.36 (0.5-100)	6.47 (0.01-3 k)	2.23 (1-100)	0.62 (1-150)	0.43 (0.5-100)
NEF $^{(E)}$	2.8 ^{D}	27.2	30.26 ^{C}	9.6	3.3 ^{D}
PEF $^{(E)}$	7.9 ^{D}	887.8	1648 ^{C}	110.6	12.54 ^{D}

^{A} Chip area, ^{B} Area from IA to ADC, ^{C} Estimated from reported data, ^{D} Power w/o ADC & biasing ckt., ^{E} Calc. w/ IRN using 1st order LPF

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