Mobius: A 12V-to-1V Charge-Cross-Converging Converter Ring with Monolithic Handshake Driving for Next-Generation AI Server

Xuliang Wang[1], Zhoutong Liu[1], Haoyu Wang[1], Tianxin Min[2], Wing-Hung Ki[2], Yan Wang[1], and Xiaosen Liu[1]
[1]Tsinghua University, BNRist, Beijing, China, [2]The Hong Kong University of Science and Technology, Hong Kong SAR
Email: xwangef@tsinghua.edu.cn, liuxiaosen@tsinghua.edu.cn

***Abstract*—A 12V-to-1V Charge-Cross-Converging Converter Ring, Mobius, is proposed for high-density power delivery in AI computing infrastructure, rendering inherent balancing, inductor current reduction, and Monolithic Handshake Driving. Fabricated in a 130-nm BCD process with flip-chip assembly, it achieves 94.7% peak efficiency, 3% improvement among state-of-the-art (SOTA) designs, and 510-A/cm^3 peak density.**

***Index Terms*—Multi-phase, inherent balancing, cross-phase charge converging, monolithic handshake driving**

I. Introduction

The ever-growing power demands of next-generation AI servers are catalyzing the transition toward 800-V HVDC infrastructures. To mitigate I^2R distribution losses within power racks, a two-stage delivery architecture is typically employed: initially stepping down the 800-V HVDC to a 12-V intermediate bus voltage (IBV), followed by further regulation via point-of-load (PoL) converters (Fig. 1). Among PoL solutions, multi-phase (MP) hybrid Buck converters have gained prominence for their superior current handling and extended voltage conversion ratios (VCRs), facilitated by split inductors and front-capacitive networks [1]–[5]. However, as current density scales up and inductor footprints shrink to meet height-limit constraints, the inductor DCR losses escalate sharply (Fig. 2). Furthermore, the proliferation of passive devices, such as bootstrap capacitors (C_{BST}), increasingly offsets the density advantages offered by low-voltage transistors [6].

This paper introduces a Charge-Cross-Converging (QCC) hybrid Buck converter, Mobius, that simultaneously achieves continuous reduction of inductor current (I_L) and ring-type self-balancing. To eliminate redundant C_{BST} components, a Monolithic Handshake Driving (MHD) technique is proposed. By strategically reusing intrinsic mid-voltage rails, this technique ensures deterministic switching sequences for multi-level power transistors with high efficiency.

II. Charge Cross Converging

Fig. 3 illustrates the operating principle of the proposed Cross-Phase Charge Converging technique. In State I ($S1$), I_L is equally partitioned through C_{F1} and C_{F2}, then steered into the mid-rail DC capacitors (V_{MIDH} and V_{MIDL}). During State II ($S2$), C_{F1} and C_{F2} are charged by V_{IN} and V_{MIDH}, respectively; their charge displacements subsequently converge into C_{F3} along with I_L. Based on the charge balance of the flying capacitors (C_{fly}s), the ratio between I_L and the output current I_{OUT} is derived as $\frac{1}{D+2}$. This represents a substantial reduction in inductor DCR loss compared to conventional output-inductor topologies. The switching-node voltage (V_{SW}) is established at $3V_{OUT} - 0.5V_{IN}$ during the charge-steering state (S_1) and $2V_{OUT}$ during the charge-converging state (S_2). By applying the volt-second balance principle, the voltage conversion gain is determined as $\frac{D}{2(D+2)}$. At a nominal duty cycle of $D = 0.5$, the proposed QCC converter effectively performs a 10:1 step-down from a 12-V V_{IN} to a 1.2-V V_{OUT}. When extending to 4-phase operation, the C_{fly} charge displacement exhibits inter-phase cyclic symmetry (Fig. 4), where the charge steered from phases in S_1 is uniformly transferred to those in S_2. Consequently, inter-phase I_L balancing is intrinsically

This work was supported by BNR2026RC01013, the National Natural Science Foundation of China (NSFC) under Grant 62374100, and the Beijing Municipal Natural Science Foundation under Grant 4244106. *Corresponding Author: Xiaosen Liu.*

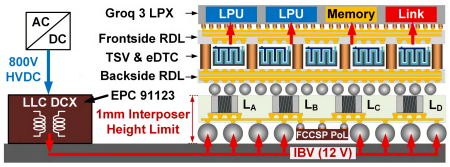

Fig. 1. Power delivery architecture for next-generation AI server.

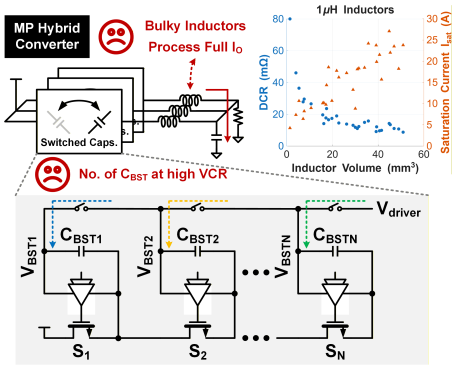

Fig. 2. Limitations of conventional multi-phase (MP) hybrid Buck converters.

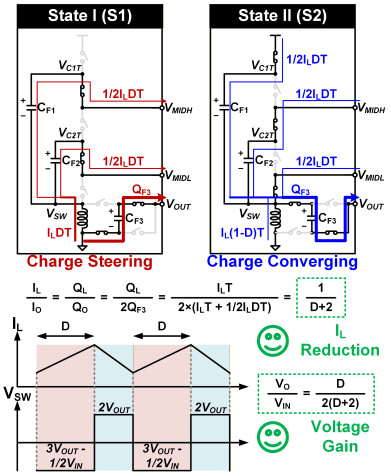

Fig. 3. Switching states, inductor current reduction, and voltage gain extension of the proposed Cross-Phase Charge Converging technique.

maintained by the cross-phase C_{fly} charge equilibrium, necessitating only minimal shared DC capacitance to suppress $V_{MIDH/L}$ ripples. This cyclic symmetry remains robust for general cases regardless of D. For a 3-phase configuration (Fig. 5), the charge balance equations interconnecting the phase currents ($I_{LA,B,C}$) can be elegantly expressed in the following matrix form, whether $D = 1/3$ or not:

$$D \underbrace{\begin{bmatrix} -\frac{1}{2} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{4} & -\frac{1}{2} & \frac{1}{4} \\ \frac{1}{4} & \frac{1}{4} & -\frac{1}{2} \end{bmatrix}}_{\mathbf{M_1}:3\times3} \times \begin{bmatrix} I_{LA} \\ I_{LB} \\ I_{LC} \end{bmatrix} = \mathbf{O_{3,1}} \quad (1)$$

The system matrix $\mathbf{M_1}$, dictated by the QCC mechanism, possesses a zero row-sum property and a rank of 2. Therefore, the all-ones vector $\mathbf{1}$ constitutes the null space of $\mathbf{M_1}$, proving that a uniform current distribution ($I_{LA} = I_{LB} = I_{LC}$) is the unique steady-state solution. As shown in Fig. 6, a parallel derivation for the 4-phase case confirms this inherent balancing even with $D \neq 0.5$.

III. Monolithic Handshake Driving

Fig. 7 (left) illustrates the comprehensive architecture of the proposed 4-phase QCC converter. The high-side switches (S_{H1-6}) are implemented with 5-V CMOS transistors, while the low-side switches (S_{L1-3}) utilize 1.5-V devices. Except for the S_{H1} PMOS, all power switches are NMOS-based. Among the high-side drivers, even-numbered stages are powered by adjacent DC rails, whereas odd-numbered stages are referenced to the terminal voltages of the flying capacitors (C_{fly}). Specially tailored dual-branch gate drivers are employed for $S_{H5,6}$, leveraging the potential differences between V_{C1T}/GND and V_{SW}/fixed-5V. This configuration ensures robust gate overdrive despite significant voltage swings on V_{C1T} and V_{SW} (ranging from $-3V_{OUT} + 0.5V_{IN}$ to $2V_{OUT}$) [7]. To maintain strict non-overlapping operation, the raw

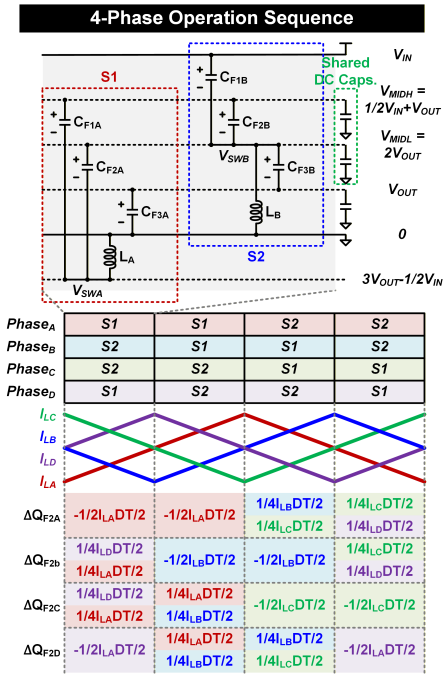

Fig. 4. 4-phase operating sequence and C_{fly} charge displacement of the proposed QCC converter with $D = 0.5$.

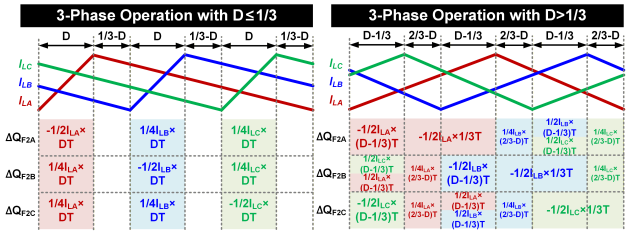

Fig. 5. 3-phase operating sequence and C_{fly} charge displacement of the proposed QCC converter with $D = 1/3$ (left) and $D \neq 1/3$ (right).

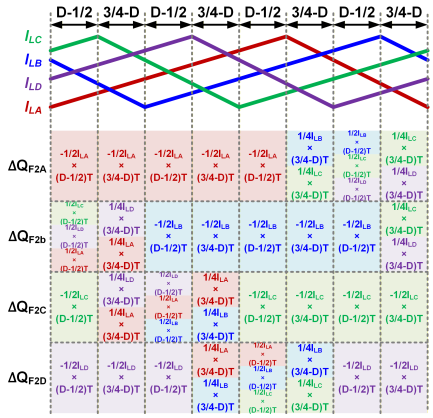

Fig. 6. 4-phase operating sequence and C_{fly} charge displacement of the proposed QCC converter with $D \neq 0.5$.

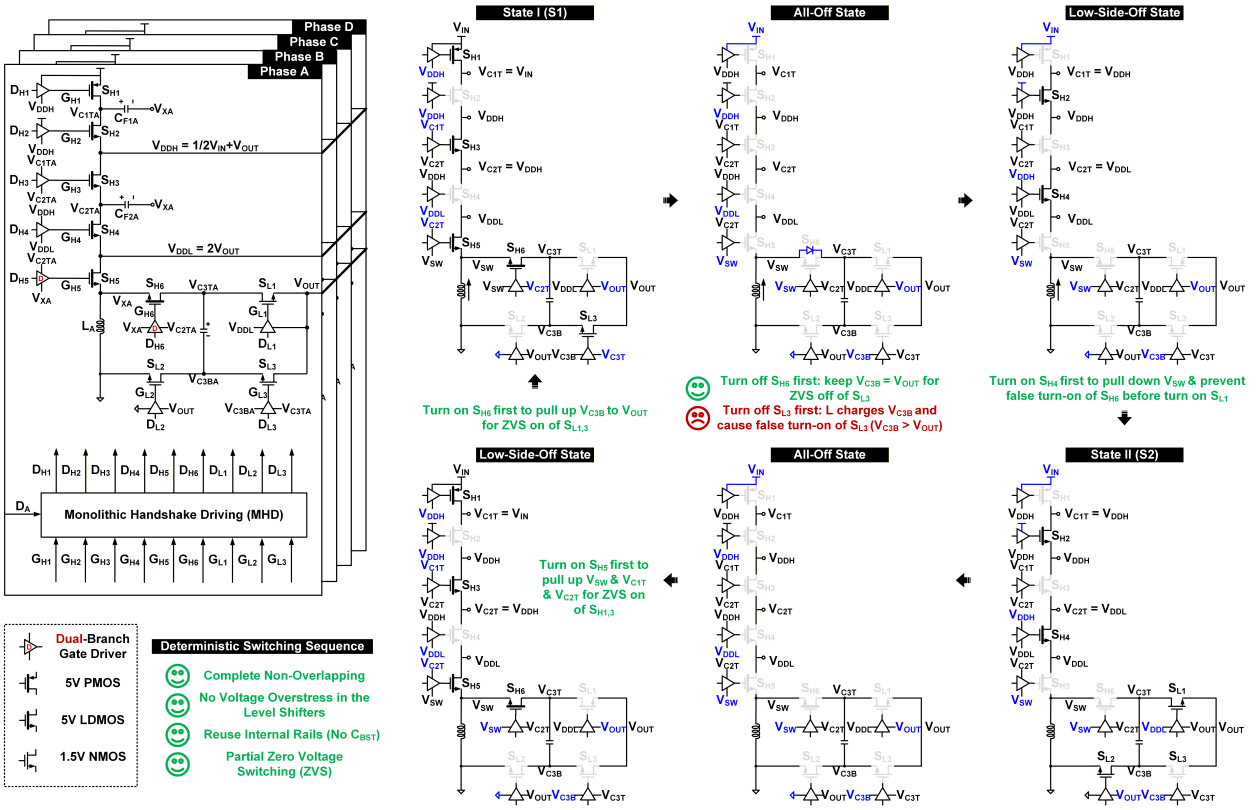

Fig. 7. Overall architecture of the proposed QCC converter (left), and the deterministic switching sequence of the proposed MHD technique (right).

duty cycle of each phase is logically combined with sampled gate signals ($G_{H(L)i}$). This deterministic switching sequence maximizes zero-voltage switching (ZVS) while safeguarding level shifters against false triggering and voltage overstress. The key dead-time sub-intervals are detailed on the right, with active driver rails highlighted in blue. Specifically, when transitioning from State I to All-Off, S_{H6} is deactivated first to clamp V_{C3B} at V_{OUT}, facilitating ZVS for S_{L3}. Without this sequence, the inductor would charge V_{C3B} through S_{H6} (or its body diode), potentially causing the false turn-on of S_{L3} if V_{C3B} exceeds V_{OUT}. Similarly, during the transition from All-Off to Low-Side-Off, $S_{H2,4}$ are engaged to pull down V_{SW} prior to S_{L1} activation, preventing S_{H6} from false turn-on induced by a positive V_{SW} excursion.

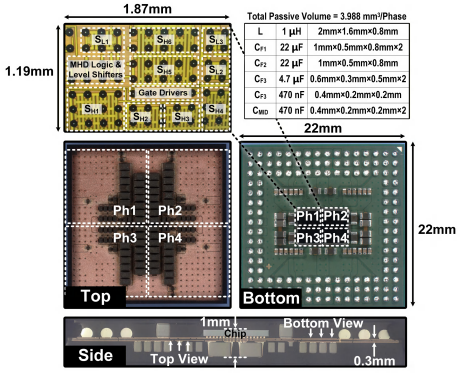

Fig. 8. Chip and package photos of the proposed 4-phase QCC converter.

IV. Measurement Results

The chip micrograph of the proposed QCC converter is depicted in Fig. 8, where the inter-phase power traces are symmetrically routed to the Integrated Passive Devices (IPDs). To comply with the 1-mm interposer height constraint, all flying and decoupling capacitors are implemented using sub-0402 footprints. As illustrated in Fig. 9, the measured switching-node waveforms and simulated MHD control signals exhibit excellent agreement with the theoretical analysis. The proposed QCC converter maintains a peak efficiency of approximately 95% across varying numbers of active phases (Fig. 10). It achieves a maximum I_{OUT} of 8.52 A, the highest among reported SOTA designs, while sustaining an efficiency of 81.8% at full load. Table I provides a comprehensive comparison with recent 12-V-to-1-V MP hybrid converters. Notably, the QCC converter delivers a 3% improvement in peak efficiency (Fig. 11) alongside highly competitive current density, marking a significant advancement in high-density power delivery.

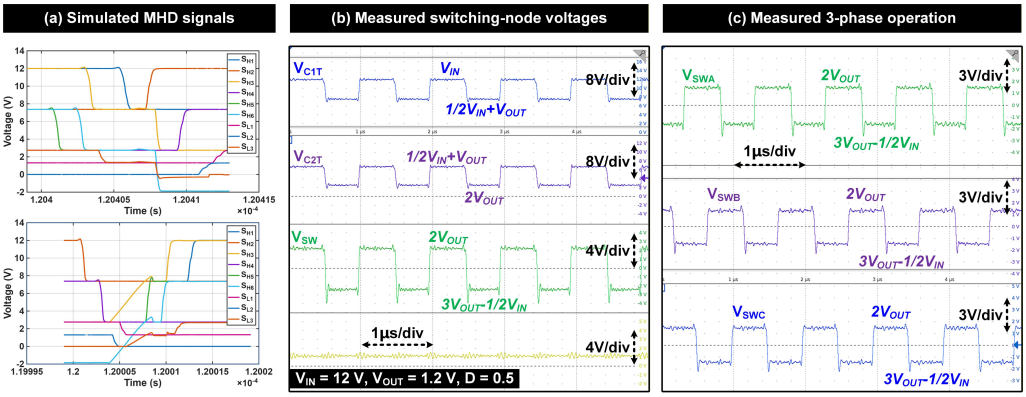

Fig. 9. (a) Simulated MHD signals, (b) Measured switching-node voltages, and (c) Measured 3-phase operation.

TABLE I
COMPARISON WITH SOTA 12-V-TO-1-V MP HYBRID CONVERTERS.

	ISSCC'25 [2]	ISSCC'25 [3]		ISSCC'25 [4]	ISSCC'26 [5]	This Work
Process	180nm BCD	180nm BCD		180nm BCD	180nm BCD	**130nm BCD**
No. phases	3	3		2	6	**4**
Nominal V_{IN} (V)	12	12		12	12	**12**
Nominal V_{OUT} (V)	1-1.8	0.3-1.1		1-1.2	1-1.8	**1-1.5**
Switching Freq. f_{SW} (MHz)	2	1	1.5	1	2	**1**
Max. I_{OUT} (A)	6	7		5	8	**8.52**
Inductor & DCR (per phase)	600 nH & 29 mΩ	680 nH & 17 mΩ	470 nH & 29 mΩ	1 µH & 48 mΩ	900 nH & 26 mΩ	**1 µH & 35 mΩ**
Inductor Volume (mm^3)	3 × 1.92	3 × 16	3 × 1.92	2 × 3.84	6 × 6	**4 × 2.56**
I_L Reduction Ratio (I_L/I_{OUT})	No	No		No	No	**1/(D+2)**
Flying Capacitor (footprint)	6 × 1 µF	2 × 2.2 µF		2 × 10 µF	6 × 2.2 µF	**3 × 22 µF, 2 × 4.7 µF, 1 × 470 nF (per phase)**
C_{OUT} (µF)	10	10	22	2 × 10	20	**8 × 4.7**
Peak Eff. @V_{IN} (V) & V_{OUT} (V)	91.7% @ 12 & 1	91% @ 12 & 1.1	88.3% @ 12 & 1.1	90.2%@ 12 & 1.2	90.5%@ 12 & 1	**94.7% @ 12 & 1.2**
Eff. @I_{MAX} & V_{OUT}	80% @ 6A & 1V	82% @ 7A & 1V	82.8% @ 5.5A & 1V	72% @ 5A & 1.2V	84% @ 8A & 1V	**81.8% @ 8.52A & 1.2V**
Die Area (mm^2)	6	6.3		4.56	11.5	**11.1**
Tot. Passive Volume (mm^3)	8.43	50.3	8.06	36.6	45.4	**16.7**
Peak Current Density	712 A/cm^3	139 A/cm^3	868 A/cm^3	137 A/cm^3	176 A/cm^3	**510 A/cm^3**
Current Density @ Peak Eff.	237 A/cm^3	39.8 A/cm^3	248 A/cm^3	27.3 A/cm^3	33 A/cm^3	**122 A/cm^3**

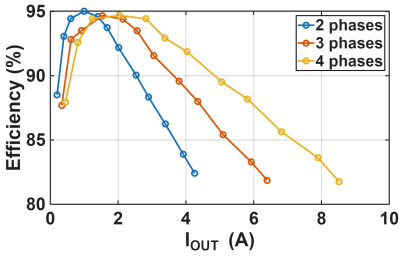

Fig. 10. Measured efficiencies with different numbers of active phases.

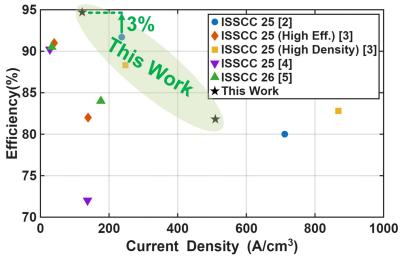

Fig. 11. Efficiency/density trade-offs of SOTA designs.

REFERENCES

[1] J. -W. Chang et al., "A Four-Phase Flying Capacitor Shared Dynamic Hybrid Converter with Hierarchical Power Delivery and Four-Phase Temperature Management," in *IEEE Eur. Solid-State Electron. Research Conf. (ESSERC)*, Sept. 2025, pp. 277-280.

[2] J. Yang, R. P. Martins, and M. Huang, "A Segmented-Interlacing Multi-Phase Hybrid Converter with Inherently Auto-Balanced I_Ls and Boosted I_L Slew Rate During Load Transients," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2025, pp. 378-380.

[3] M. H. K. Hmada, W. -C. B. Liu, G. Pillonnet, and P. Mercier, "Merging Hybrid and Multi-Phase Topologies: A 6-Phase Triple-Step-Down DC-DC Converter Achieving up to a 60:1 Voltage Conversion Ratio and 868A/cm^3 Current Density," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2025, pp. 386-388.

[4] Z. Tong *et al.*, "HOOP: A Scalable Hybrid DC-DC Converter Ring for High-Performance Computing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2025, pp. 1-3.

[5] J. Yang, Z. Tang, R. P. Martins, and M. Huang, "A Multi-Phase Hybrid Converter with Q Samplers Enabling Simultaneous I_L Auto-Balance and Arbitrary Phase Count," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2026, pp. 450-452.

[6] H. Chen, Y. -S. Noh, M. Gong and A. Raychowdhury, "A 0.193A/mm^3 89.8% 24V-1V Dual-path Hybrid Dickson Converter with Fully Integrated Dynamic Charge Transfer Bootstrapped Gate Drivers," in *IEEE Eur. Solid-State Electron. Research Conf. (ESSERC)*, Sept. 2025, pp. 201-204.

[7] Y. Ji, J. Jin, and L. Cheng, "A 12V-Input 1V-1.8V-Output 94.7%-Peak-Efficiency 685A/cm^3-Current-Density Hybrid DC-DC Converter with a Charge Converging Phase," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 458-460.