A 47.9-71 GHz 3.67-dB NF LNA Exploiting Transformer-Based Enhanced Noise Reduction and Dual Gain-Boosting Technique

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***Abstract*—This paper proposes a V-band cascode low-noise amplifier (LNA) exploiting transformer-based enhanced noise reduction and dual gain-boosting technique. Unlike prior cascode LNAs, where the condition for noise reduction or gain boosting generally applies to only one transistor, the proposed topology establishes a single condition under which the noise contributions of both the common-source (CS) and common-gate (CG) transistors are reduced simultaneously. Furthermore, by jointly raising the output impedance and the effective transconductance, the proposed approach accomplishes dual gain improvement without adding further active stages. Fabricated in 28 nm CMOS technology, the proposed LNA achieves a peak gain of 23.0 dB at 65.9 GHz, a 3-dB bandwidth of 47.9 to 71.0 GHz, and a measured NF of 3.67 to 4.11 dB while drawing 12.1 mW from a 0.9 V supply and occupying a core area of 0.15 mm^2.**

***Keywords*—Enhanced noise reduction, dual gain-boosting, CMOS low-noise amplifier (LNA), noise figure (NF), wideband, millimeter-wave (mm-Wave), transformer.**

I. Introduction

Driven by the rapid growth of high-speed wireless systems, the mm-Wave band has become a key enabler for high-data-rate and low-latency WLAN applications [1], [2]. IEEE 802.11ad, operating from 57 to 71 GHz, supports multi-gigabit short-range wireless communication. As a key receiver front-end block, the cascode LNA is attractive for its high gain, good stability, and wide bandwidth. Transformer coupling has been widely employed in mm-Wave cascode LNAs to exploit device parasitics for impedance and noise matching while extending bandwidth and enhancing gain [3]-[5]. However, in these existing cascode LNAs, the condition for gain boosting or noise reduction is specific to a single device rather than the cascode pair. The resulting noise suppression is limited to either the CS or the CG transistor, while gain enhancement is achieved through only a single mechanism, making it difficult to obtain low NF and high gain simultaneously. Moreover, although these works mitigate the noise contribution of the CG transistor, the overall NF improvement remains limited because the CS transistor contributes the dominant noise.

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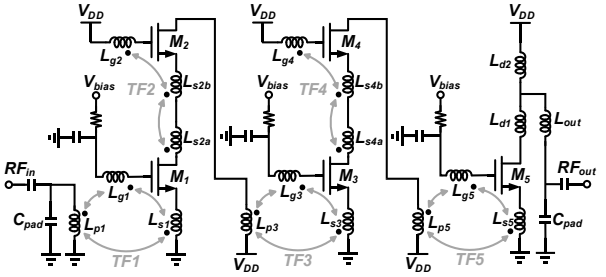


M_1	24μm / 30nm	L_{p1}	166pH	L_{g1}	174pH	L_{s1}	98pH
		$k_{p1,\,g1}$	0.61	$k_{g1,\,s1}$	0.44	$k_{p1,\,s1}$	0.60
M_2	38.4μm / 30nm	L_{s2a}	19pH	L_{g2}	46pH	L_{s2b}	64pH
		$k_{s2b,\,g2}$	0.54	$k_{s2a,\,s2b}$	0.11		
M_3	24μm / 30nm	L_{p3}	137pH	L_{g3}	148pH	L_{s3}	47pH
		$k_{p3,\,g3}$	0.56	$k_{g3,\,s3}$	0.25	$k_{p3,\,s3}$	0.34
M_4	28.8μm / 30nm	L_{s4a}	10pH	L_{g4}	46pH	L_{s4b}	64pH
		$k_{s4b,\,g4}$	0.54	$k_{s4a,\,s4b}$	0.12		
M_5	24μm / 30nm	L_{p5}	155pH	L_{g5}	187pH	L_{s5}	38pH
		$k_{p5,\,g5}$	0.46	$k_{g5,\,s5}$	0.16	$k_{p5,\,s5}$	0.25
C_{pad}	60fF	L_{d1}	63pH	L_{d2}	52pH	L_{out}	58pH

Fig. 1. Schematic of the proposed TF-based enhanced noise reduction and dual gain-boosting LNA.

In this paper, a cascode LNA is proposed that inherently unifies the noise reduction of the CS and CG transistors under a single condition. Moreover, dual gain-boosting is achieved by simultaneously enhancing the effective G_m and the output impedance. The schematic of the proposed LNA is shown in Fig. 1, which consists of two cascode stages followed by one CS output stage. Section II presents the analysis of the enhanced noise reduction and dual gain-boosting technique together with circuit implementation. Section III summarizes the measurement results, and Section IV concludes this paper.

II. Circuit Design

A. Enhanced Noise Reduction Technique

The equivalent model of the proposed LNA is depicted in Fig. 2, where TF2 is replaced by two equivalent inductors and a gate-source feedback amplifier. The equivalent inductors and the feedback coefficient are given by [7]:

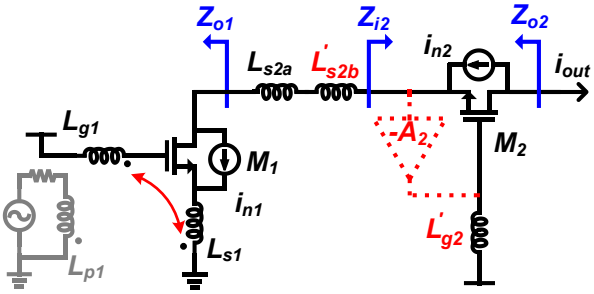


Fig. 2. Equivalent circuit model of the proposed LNA.

$$L'_{g2} \approx \frac{L_{g2} + M_{gs2}\left(1 + C_{sb2}/C_{gs2}\right)}{1 + \omega^2 M_{gs2} C_{sb2}}$$

$$L'_{s2b} \approx L_{s2b} + \frac{M_{gs2}\left(1 + \omega^2 M_{gs2} C_{sb2}\right)}{1 + C_{sb2}/C_{gs2} - \omega^2 L_{g2} C_{sb2}} \tag{1}$$

$$A_2 = \frac{\omega L'_{g2}}{1/\omega C_{gs2} - \omega L'_{g2}} > 0$$

where M_{gs2} is the mutual inductance of L_{g2} and L_{s2b}, and C_{gs2} and C_{sb2} are parasitic capacitances of M_2.

The output noise current is derived as:

$$\overline{i_{n,out}^2} = |A_{n1}|^2 \overline{i_{n1}^2} + |A_{n2}|^2 \overline{i_{n2}^2} \tag{2}$$

where i_{n1} and i_{n2} are the channel noise current of M_1 and M_2, and A_{n1} and A_{n2} are the noise transfer functions of i_{n1} and i_{n2}. According to [6], if the effect of the primary inductor is ignored, the coupling between L_{g1} and L_{g2} forms a feedback path that cancels the output noise current of M_1 at a certain frequency:

$$A_{n1} = 0 @ \omega_0 = \frac{1}{\sqrt{C_{gs1}\left(L_{s1} + L_{g1} + 2M_{gs1}\right)}} \tag{3}$$

where M_{gs1} is the mutual inductance between L_{s1} and L_{g1}, and C_{gs1} is the parasitic capacitance of M_1.

The noise transfer function of i_{n2} is derived as:

$$A_{n2} \approx \frac{Z_{i2} + s\left(L'_{s2b} + L_{s2a}\right)}{Z_{i2} + s\left(L'_{s2b} + L_{s2a}\right) + Z_{o1}} \tag{4}$$

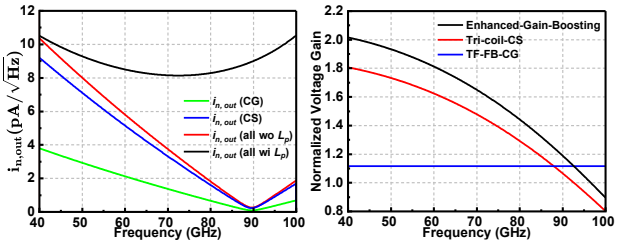
where Z_{i2} is the input impedance looking into the source of M_2, and Z_{o1} is the output impedance looking into the drain of M_1. Z_{i2} and Z_{o1} are derived as:

$$Z_{i2} = \frac{1}{\left(1 + A_2\right) g_{m2}}$$

$$Z_{o1} = r_{o1} + \frac{sL_{s1} + sg_{m1}r_{o1}\left(M_{gs1} + L_{s1}\right) + s^3 C_{gs1}\left(L_{s1}L_{g1} - M_{gs1}^2\right)}{1 + s^2 C_{gs1}\left(L_{s1} + L_{g1} + 2M_{gs1}\right)} \tag{5}$$

At the noise canceling frequency, the denominator of the second term of Z_{o1} becomes zero, leading to an infinite output impedance at the drain of M_1. Hence, the noise transfer function of i_{n2} equals zero in (4), which means the output noise current of M_2 is blocked by the infinite impedance at the drain of M_1.

Therefore, the noise reduction of M_1 and M_2 is inherently unified at a single condition. The noise current of M_1 is canceled by the coupling between L_{g1} and L_{g2} at the frequency given by (3), which also creates a high-impedance node at the drain of M_1 that suppresses the noise current of M_2. The proposed cascode LNA achieves the noise reduction of the CS and CG transistors simultaneously.



(a) (b)

Fig. 3. Simulation results of the proposed LNA. (a) Output noise current. (b) Normalized voltage gain of multiple LNA topologies.

In practice, the primary coil L_{p1} of TF1 in Fig. 2 introduces an additional path that breaks the noise-canceling condition [6]. Nevertheless, the output noise is still reduced around the noise-canceling frequency. Fig. 3 (a) shows the simulated output noise current of the proposed LNA. The output noise currents of M_1, M_2, and the overall output noise exhibit a common null at 90 GHz, indicating that the noise currents of M_1 and M_2 are reduced simultaneously. The noise canceling frequency is set 1.5 times the center frequency to leave sufficient margin against other parasitic effects. M_2 contributes significantly less noise than M_1 owing to the high impedance at the drain of M_1, as given by (4). The black curve illustrates the total output noise with the primary inductor and other parasitic capacitances of the CS stage included. The null disappears due to the additional path, leading to an increase in the output noise. Nevertheless, the in-band noise still exhibits a minimum, which is shifted toward lower frequencies owing to the additional parasitic capacitances.

B. Dual gain-boosting Technique

The tri-coil TF1, consisting of L_{p1}, L_{g1}, and L_{s1}, allows M_1 to operate at a simultaneous CS- and CG mode, thereby boosting the equivalent G_m of M_1 by a factor A_1 compared with the CS mode [6]. A_1 is given by:

$$A_1 \approx \frac{1 + g_{m1}r_{o1} - \omega^2 L_{g1} C_{gs1}}{g_{m1}r_{o1} + \omega^2 L_{s1} C_{gs1}} \frac{M_{ps1}}{M_{pg1}} > 0 \tag{6}$$

where g_{m1} is the transconductance of M_1. The output impedance of the proposed LNA is derived from the equivalent model in Fig. 2:

$$Z_{o2} \approx r_{o2} + \left[1 + g_{m2}r_{o2}\left(1 + A_2\right)\right] \times \left[Z_{o1} + s\left(L'_{s2b} + L_{s2a}\right)\right] \approx g_{m2}r_{o2}\left(1 + A_2\right) Z_{o1} \tag{7}$$

Accordingly, the voltage gain of the proposed LNA is obtained as:

$$A_v = G_{m1} Z_{o2} = \left(1 + A_1\right)\left(1 + A_2\right) g_{m1} g_{m2} r_{o2} Z_{o1} \tag{8}$$

which features dual gain-boosting relative to conventional cascode LNAs. Fig. 3 (b) depicts the normalized gain of different LNA topologies with respect to the conventional

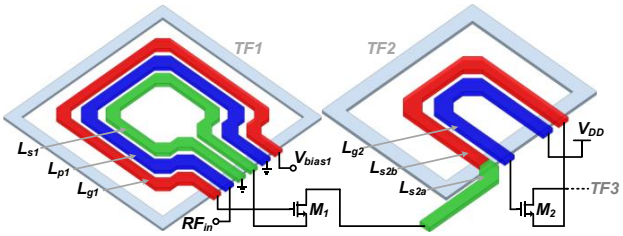


Fig. 4. Transformer implementation of the proposed LNA input stage.

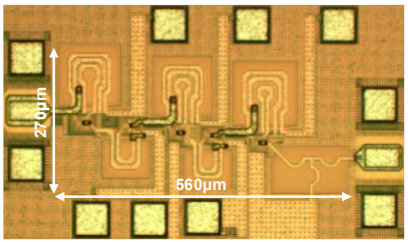


Fig. 5. Chip photograph of the fabricated LNA.

source-degeneration cascode LNA. The red curve represents the gain when M_1 adopts the tri-coil TF-based G_m-boosting technique. The blue curve represents the gain when M_2 adopts the TF feedback cascode technique. Each technique individually boosts the voltage gain across the operating band. The black curve corresponds to the gain of the proposed dual gain-boosting LNA, which achieves the highest gain among the compared LNA topologies.

C. Circuit and Transformer Implementation

As depicted in Fig. 1, the proposed LNA consists of two cascode gain stages and one CS output stage. For power and bandwidth optimization, the sizes of M_2 and M_4 are set to 1.6 times and 1.2 times that of M_1 and M_3 in stages one and two, respectively. This configuration fully exploits the high gain and wide bandwidth provided by the two cascode stages, while the CS output stage offers a large voltage headroom, thereby optimizing the overall linearity of the LNA. Fig. 4 shows the input stage of the LNA, including the 3D layout of TF1 and TF2. A codirectional transformer structure is adopted for both TF, which improves the low-noise performance of the LNA [6].

The gate and source inductors in TF2 increase the LNA bandwidth in addition to delivering improved noise suppression and gain-boosting. A high-frequency pole resulting from a small inductance L_{g2} increases voltage gain and expands the upper bandwidth. Likewise, adequate total source inductance is needed to create a low-frequency pole to extend the lower bandwidth. However, to realize noise reduction and gain boosting, TF2 requires similar inductance values and a large coupling coefficient between its gate and source inductors. To solve this trade-off, the source inductor of TF2 is split into two segments, where L_{s2b} is placed close to L_{g2} with appropriate inductance to ensure a high coupling coefficient for TF2, and L_{s2a} is positively coupled with L_{s2b} to compensate for the remaining inductance required.

III. Measurement Results and Comparison

The proposed LNA was fabricated in the TSMC 28 nm CMOS process. The chip micrograph is shown in Fig. 5. The LNA occupies a core area of 560 × 270 μm^2. The LNA draws 13.4 mA of current from a supply voltage of 0.9 V, consuming a power of 12.1 mW. Fig. 6 depicts the probe testing diagram and the testing instruments connection configuration. The S-parameters, NF, $IP_{1dB,}$ and IIP3 were measured using Keysight N5247B PNA-X network analyzer and mm-Wave frequency extender modules N5260-60003.

An on-chip Line-Reflect-Reflect-Match (LRRM) calibration is prepared for S-parameters measurement. The S-parameters

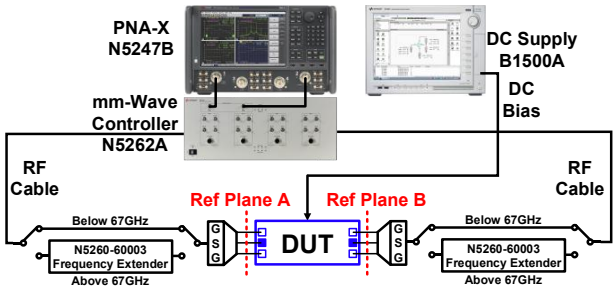


Fig. 6. LNA measurement setup diagram.

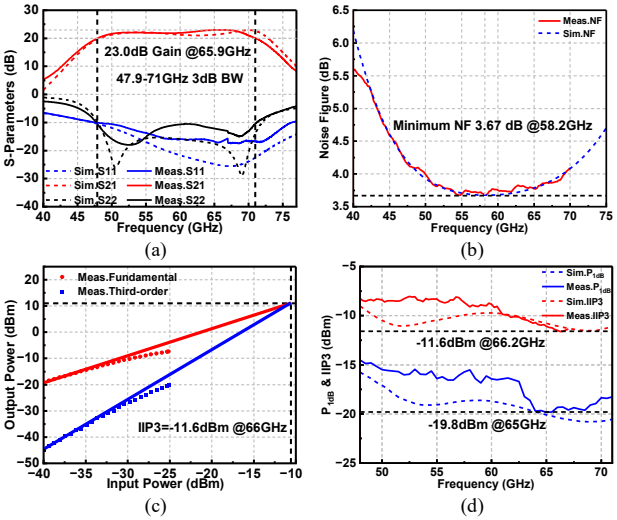


Fig. 7. Measurement and post-layout simulation results of the proposed LNA. (a) S-parameters. (b) NF. (c) IIP3 at 66 GHz. (d) IP_{1dB} and IIP3.

under 67 GHz are measured by N5247B, and the S-parameters above 67 GHz are measured by N5247B and N5260-60003, as illustrated in Fig. 6. The S-parameters measurement result is displayed in Fig. 7 (a). The LNA reaches a 3-dB bandwidth (BW) of 23.1 GHz from 47.9 to 71.0 GHz with a peak gain of 23.0 dB at 65.9 GHz, which fully covers the 802.11ad band (57 to 71 GHz). The measured S_{11} is better than -10 dB from 47.6 to 76.4 GHz, and the S_{22} is better than -10 dB from 47.9 to 71.2 GHz. The S_{11} and S_{22} remain better than -10 dB within the BW. The NF is measured with N5247B and a noise source (Noisecom NC346VX). As shown in Fig. 7 (b), the measured minimum NF is 3.67 dB at 58.2 GHz, and the NF varies from 3.67 to 4.11 dB over the range from 47.9 to 70 GHz. Fig. 7 (c) shows the measured power sweep curves of fundamental and third-order intermodulation products (IMD3) at 66 GHz. The measured IIP3 is -11.6 dBm at 66 GHz. Fig. 7 (d) shows the IIP3 and IP_{1dB} measurement results. The LNA demonstrates an IP_{1dB} and IIP3 of above -19.8 and -11.6 dBm.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART V-BAND LNAS

Ref.	**This work**	TMTT'26 [8]	JSSC'25 [9]	JSSC'24 [10]	MWTL'24 [11]	ESSCIRC'21 [12]	ESSCIRC'21 [13]
Tech.	**28 nm CMOS**	40 nm CMOS	40 nm CMOS	40 nm CMOS	40 nm CMOS	65 nm CMOS	28 nm CMOS
Topology	**2-stage CAS + 1-stage CS Enhanced noise reduction Dual gain-boosting**	3-stage CS	2-stage CS	3-stage CS	3-stage CS	4-stage CS	3-stage CAS
Frequency (GHz)	**47.9–71.0**	50–70.9	70–86	51.6–71.8	70–91	35–50	38.5–60.5
Peak Gain (dB)	**23.0**	23.1	16.5	22.4	16.4	30.5	18
BW_{eff} ^ (GHz)	**23.1**	20.9	16	20.2	21	15	19.5
NF (dB)	**3.67 ~ 4.11**	3.8	4.8	3.78	5.0	4.1	6.2
IP_{1dB} (dBm)	**-19.8 ~ -14.5**	-14.5	-8.5	-14.2	N.R.	-29	-26
IIP3 (dBm)	**-11.6 @ 66.2 GHz**	-4.9*	-0.7*	-4.6*	N.R.	-19.4*	-16.4*
V_{DD} (V)	**0.9**	1.1	1.1	1.1	0.9	1.2	0.9
DC Power (mW)	**12.1**	33	25	34	20.7	63.6	35
Core area (mm^2)	**0.15**	0.076	0.085	0.12	0.163	0.47	0.175
FoM	**20.3**	6.5	2.1	10.5	3.1	5.0	1.4

N.R. = Not Reported. ^BW_{eff}: gain is within 3-dB BW for both $|S_{11}|$ and $|S_{22}|$ < -10 dB. *IIP3 is estimated using IP_{1dB} + 9.6 dB.

$$FoM = \frac{Gain[lin] \times BW_{eff}[GHz]}{\left(NF_{\min}[lin]-1\right) \times P_{dc}[mW]}$$

Table I summarizes the performance comparison between the proposed LNA and prior works. Among the listed designs, the proposed LNA achieves the lowest NF, the widest bandwidth, the lowest power consumption, and the highest FoM, indicating highly competitive overall performance.

IV. CONCLUSION

This paper presents a three-stage single-ended V-band cascode LNA that exploits transformer-based enhanced noise reduction and dual gain-boosting techniques. By establishing a unified condition for simultaneously reducing the noise contributions of the CS and CG transistors while jointly enhancing the effective transconductance and output impedance, the proposed design achieves low NF, high gain, wide bandwidth, and low power consumption. Fabricated in 28 nm CMOS technology, the proposed LNA demonstrates competitive measured performance, making it a promising candidate for V-band mm-Wave receivers targeting IEEE 802.11ad applications.

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