A 140μA, 8.5m°/s/√Hz 3-Axis Always-on Sense MEMS Gyroscope with 260Hz Bandwidth using Phase-locked Dynamic Amplifier Technique

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***Abstract*—A low power (140μA), low noise (8.5m°/s/√Hz), 3-axis always-on sense MEMS gyroscope with 260Hz signal bandwidth and 2000°/s input range enabled by the phase-locked dynamic amplifier (PLDA) technique is presented. Compared to the state-of-the-art, the 1.8X power reduction limitation of the conventional always-on sense mode is improved to 4.4X by the PLDA based always-on sense mode, and the efficiency is improved by 3X from 65.7pJ to 22.1pJ.**

Keywords*—MEMS gyroscope, always-on sense, phase-locked dynamic amplifier (PLDA) technique.

I. Introduction

MEMS gyroscopes are widely used in mobile and wearable devices with human-machine interface for motion detection and indoor navigation [1]. In these applications, the always-on modes including the always-on drive mode and the always-on sense mode (i.e., low power mode) are required to support event-driven operation and extend battery life [2-4]. Conventionally, the burst sensing is commonly used to implement the always-on sense, which is flexible and robust [5]. The conventional open-loop low power MEMS gyroscope is shown in Fig. 1, which is composed of the drive loop and the sense channel [1]. The drive loop guarantees the amplitude-controlled oscillation of the MEMS sensor in a drive axis. With this oscillation, the sense channel can sense the input angular rate signal Ω via Coriolis effect in a sense axis orthogonal to the drive axis. The main system errors (highlighted in blue) to be addressed include the quadrature errors (F_Q, C_Q), the in-phase error (C_I) and the phase shift error (θ_{err}). The F_Q and C_I are formed by the parasitic force coupling and parasitic charge coupling from the drive loop to the sense channel, respectively. The θ_{err} converts the quadrature error into angular-rate signal. To meet the quadrature error challenge, the IQ demodulator with two sense channels is employed, which leads to high power consumption. In detail, during the full power sense mode, the most of the total current supply I_{DD} are consumed by the sense channels (71% of I_{DD} for I_{S1}). Therefore, during always-on sense mode, the burst sensing is conventionally employed with the burst clock Φ_{BT} being the power gate of the sense channel supply current I_{S1}, in order to reduce the power as much as possible. However, this method exhibits the following two limitations. Firstly, although the sense channel's power is reduced by the burst sensing, the drive loop remains in full power. Secondly, additional power and bandwidth sacrifice are required for the averaging operation to reduce the noise aliasing due to the under-sampling of the burst sensing, and for the startup of each burst sensing period. These lead to limited power reduction (e.g., only 1.8X compared to full power mode), deteriorated noise-power efficiency and limited signal bandwidth [4-6].

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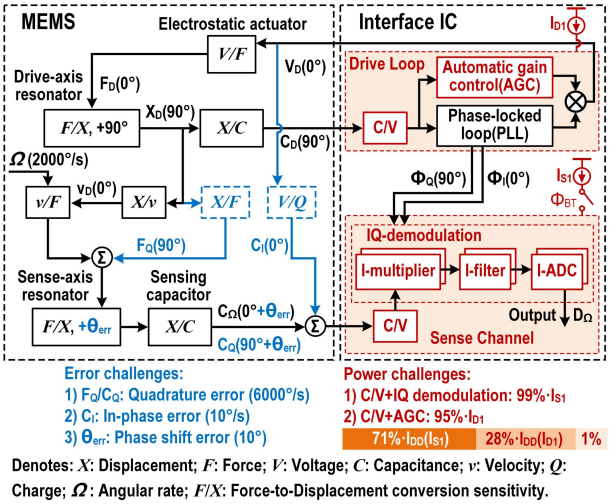

Fig. 1. Conventional open-loop MEMS gyroscope: the dominant error and power challenges

To break these limitations, this paper presents an always-on sense MEMS gyroscope based on the phase-locked dynamic amplifier (PLDA) technique, which achieves a 140μA current consumption and 4.4X power reduction with 8.5m°/s/√Hz noise floor at 260Hz signal bandwidth.

II. Proposed System Architecture

A. Always-on Strategy and PLDA-based Architecture

Fig. 2 (top) shows the always-on sense strategies. The conventional strategy is using the burst sensing with the burst clock Φ_{BT} being the power gate. However, this strategy has two limitations: full power in drive loop and noise aliasing in sense channel. To break the limitations, the proposed strategy is to dynamically synchronize the interface circuit's power with the drive signal C_D via the PLDA.

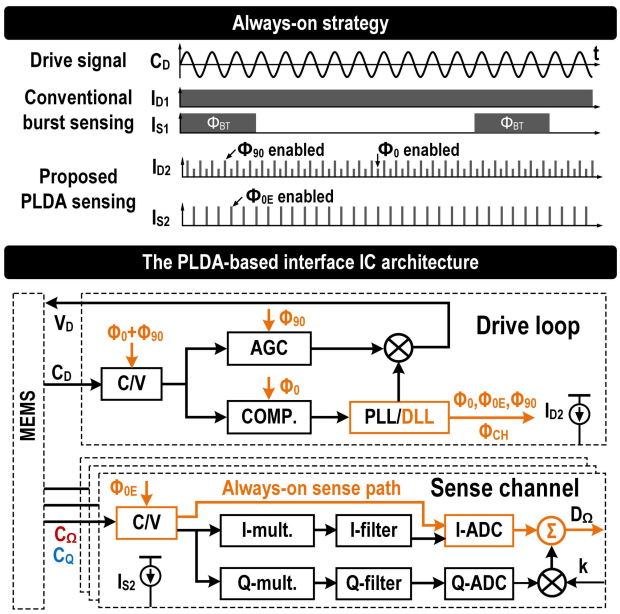

Fig. 2. Proposed always-on strategy and interface IC architecture based on PLDA.

Fig. 2 (bottom) shows the PLDA-based interface IC architecture. During the always-on sense mode, the DLL generates the low-duty-cycle power-gating clocks (Φ_0, Φ_{90}, Φ_{0E}) and the chopping clock (Φ_{CH}) which are dynamically synchronized with the sensor drive signal C_D. These synchronous clocks gate the power of the C/Vs, AGC and comparator to achieve significant power reduction. The always-on sense path bypasses the power-hungry demodulation blocks in sense channel, providing advanced power reduction.

B. *Always-on Sense Channel*

The PLDA based sense channel shown in Fig. 3 has the following four features. Firstly, the C/V's efficiency is maximized via peak-locked detection. As the Coriolis signal C_Ω is an amplitude modulated sinusoidal signal (24kHz), the signal power is periodically (48kHz) maximized at the amplitude peak. Therefore, the C/V can achieve the maximized efficiency if it detects the Coriolis signal C_Ω only at the C_Ω's amplitude peak. Theoretically, compared to the full power C/V, the PLDA C/V improves the efficiency by $\sqrt{2}$X, as the signal peak power is 2X larger than the signal average power. Secondly, the signal chain is simplified via codesign to reduce the power consumption with minimized noise aliasing. Compared to the under-sampling of the burst sensing, the Coriolis-signal-synchronized-sampling of the PLDA sensing significantly reduces the noise aliasing and avoids averaging operation which sacrifices bandwidth. By using pulse clock Φ_{0E}, the PLDA C/V has inherent amplitude demodulation for the amplitude modulated signal C_Ω, which leaves out the IQ-multipliers, the IQ anti-aliasing filter and their power consumptions. Besides, the PLDA based signal chain saves the power consumption of the Q-path ADC, as it blocks the quadrature error C_Q rather than demodulating C_Q. The backend ADC is synchronized to the PLDA (48kHz sampling frequency) and achieves a maximum 14.5b ENOB output with a bandwidth of 260Hz, reducing the power consumption compared to the full power sense mode which uses the asynchronous high frequency clocks (512kHz clock for a maximum 15b ENOB output with a bandwidth of

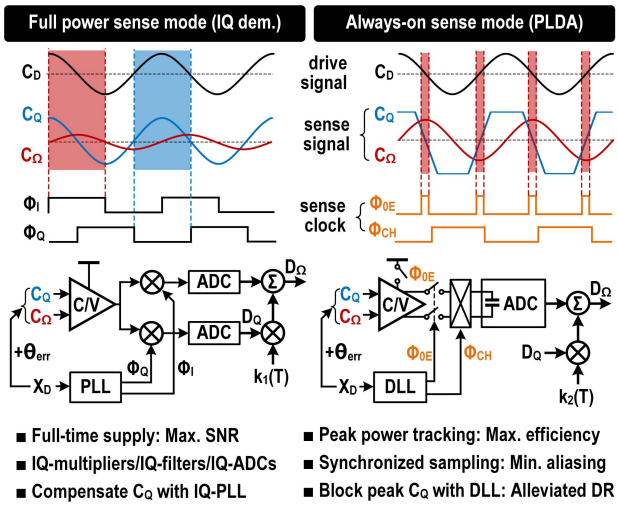

Fig. 3. Principles of the full power sense mode and the PLDA-based always-on sense mode.

550Hz). The aliasing of the chopped 1/f noise is also avoided via the ADC synchronization. Thirdly, the dynamic range of the signal chain is alleviated. The worst-case quadrature error C_Q is several times larger than the full range Coriolis signal C_Ω [8]. This requires high dynamic range redundancy of the C/V. Compared to the full power C/V, the PLDA C/V operates only at the amplitude peak of the Coriolis signal C_Ω, where the amplitude of the quadrature error C_Q is near zero. As a result, the dynamic range and power consumption of the C/V and ADC can be significantly alleviated. Note that there still exists residual quadrature error due to phase error which will be explained later in Fig. 4. At last, the PLDA based always-on sense mode is compatible with the full power sense mode. Similar to the conventional burst sensing, the PLDA sensing also needs only additional switches for the power gate and the signal path, without changing the circuit of the main modules (C/V and ADC), which is important for practical application.

C. *Always-on Drive Loop*

The drive loop employing the IQ-PLDA is shown in Fig. 4, which has the following four design strategies. Firstly, compared to the basic PLDA C/V in the sense channel providing peak-locked detection only, the IQ-PLDA C/V in the drive loop provides additional zero-cross-locked detection (Fig. 5). The peak-locked detection extracts the amplitude information of the drive signal C_D for the sensor resonance amplitude control, with the help of power gate Φ_{90} fed back from the DLL. While the zero-cross-locked detection extracts the phase information of the drive signal C_D for the DLL's reference, with the help of power gate Φ_0 fed back from the DLL. Secondly, the power of the buffer A_1, the error amplifier A_2 and the comparator C_0 are also gated by the Φ_{90}, Φ_{90} and Φ_0, respectively, in order to synchronize with the IQ-PLDA and eliminate the static power consumption. Thirdly, a dual-mode Coarse-Fine DLL is used, which works as a PLL for full power sense mode and works as a Coarse-Fine DLL to generate essential clock for PLDA-based always-on sense mode. Among these clocks, the Φ_0, Φ_{90} are for the drive loop and the Φ_{0E}, Φ_{CH} are for the sense channel. The Φ_{0E} is not only used as the power gate but also used as the Coriolis signal demodulation clock, whose phase shift is important. To be detailed, although the Φ_{0E} helps the

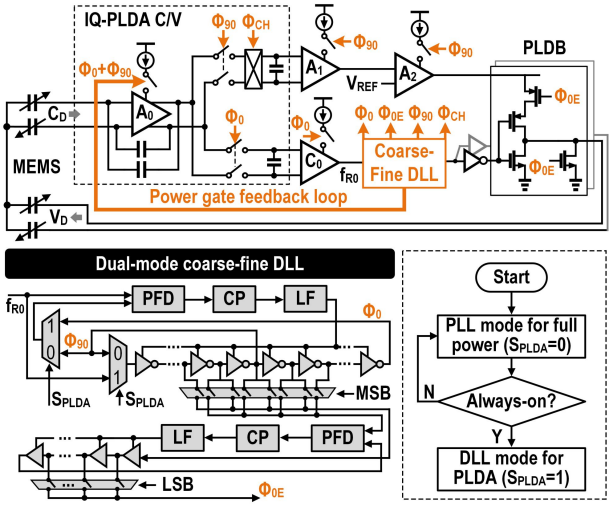

Fig. 4. Circuit design of the IQ-PLDA-based drive loop.

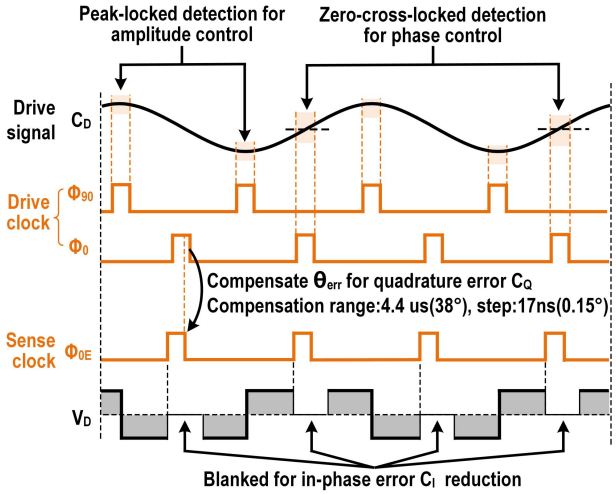

Fig. 5. Operation principle of the IQ-PLDA-based drive loop.

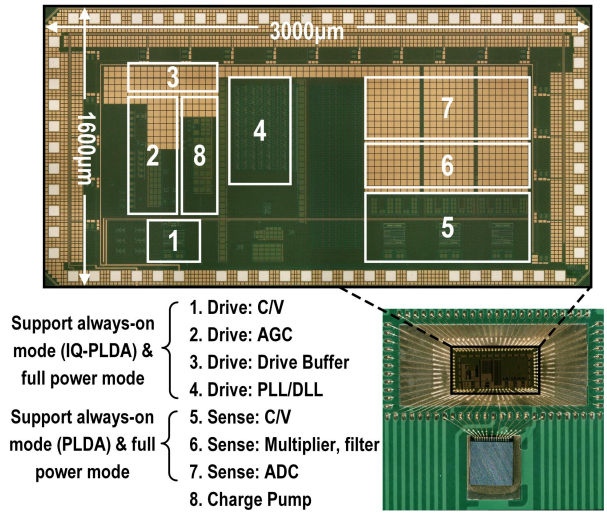

Fig. 6. Chip micrograph.

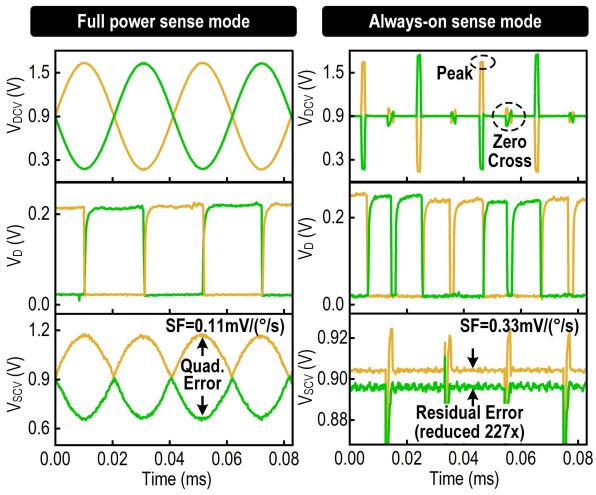

Fig. 7. Measured C/V output with reduced residual ZRO by PLDA.

PLDA C/V blocks the major portion of the quadrature error, there still remains a minor portion of the quadrature error due to the phase error θ_{err}. To solve this problem, the clock Φ_{0E} should be compensated by a phase θ_{err}. This phase compensation is controlled by a dual-mode Coarse-Fine DLL with 17ns (0.15°) step and 4.4us (38°) full range. Fourthly, the drive voltage V_D is outputted by a phase-locked dynamic buffer (PLDB) to reduce the in-phase error C_I. As mentioned in Fig. 1, the error C_I is from the drive voltage V_D. Benefitted from the PLDA, the sense channel is only active with a very short period of Φ_{0E}. Therefore, the error C_I can be avoided by blanking the drive voltage V_D during the short period of Φ_{0E} with the help of PLDB.

III. Measurement Results

As shown in Fig. 6, this work is implemented in 0.18μm BCD process with 4.8mm^2 chip area. As shown in Fig. 7, the residual zero rate output (ZRO) error at the sense C/V output V_{SCV} dominated by quadrature error is reduced by 227X from 5230°/s (575mV, SF=0.11mV/(°/s) at full power sense mode) to 23°/s (7.5mV, SF=0.33mV/(°/s) at always-on sense mode). The 23°/s residual ZRO no longer significantly deteriorates the analog frontend dynamic range, which is left to the digital backend to cancel. As shown in Fig. 8, the reduction of the PLDA duty cycle (the pulse width of the Φ_{0E}, the Φ_0 and the Φ_{90}) has significant improvement on power consumption and the efficiency. With the duty cycle reducing to the minimum value of 6.25%, the always-on power reduces from 616μA to 140μA with a 4.4X maximum power reduction compared to the full power. In contrast, due to the maximum signal power point tracking by the peak-locked detection of the PLDA sense channel, the noise floor is only increased by 3dB from 6m°/s/√Hz to 8.5m°/s/√Hz. The always-on noise-power efficiency (FoM) shows a 2.1X improvement by PLDA sensing, rather than deterioration by conventional burst sensing. The duty cycle smaller than 5% will lead to the instability of the power gate feedback loop from DLL to IQ-PLDA C/V in Fig. 4, which is not preferred. As shown in Fig. 9, the bias-instability by the Allan variance curve is 8°/hr in full power sense mode and 12.5°/hr in always-on sense mode, the slight increase of the bias-instability is due to the slight noise increment. In the full power sense mode, the noise floor and the signal bandwidth are 6m°/s/√Hz and 550Hz, respectively. In the always-on sense mode, the noise floor and the signal bandwidth are 8.5m°/s/√Hz and 260Hz, respectively. As shown in Fig. 10, benefiting from the first-order temperature compensation

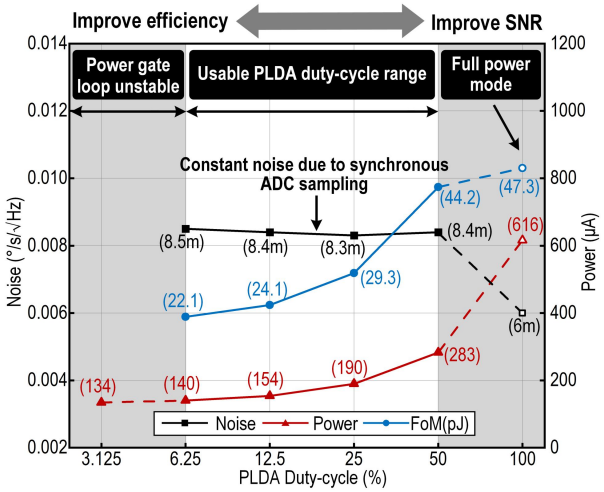

Fig. 8. Measured noise-power efficiency.

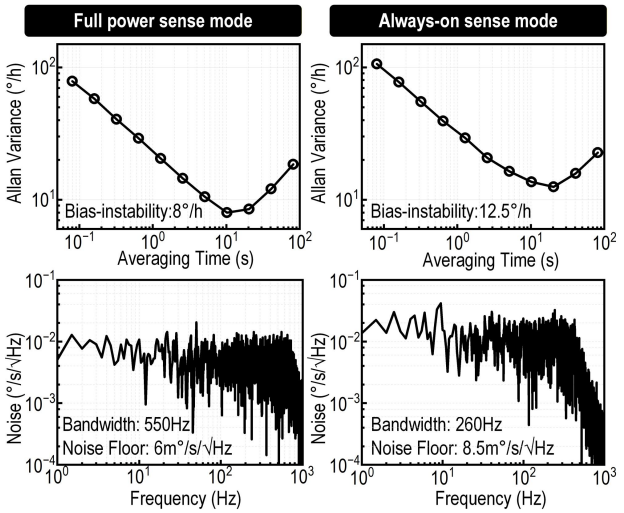

Fig. 9. Measured Allan variance and noise performance.

with the pre-stored quadrature error D_Q (Fig. 3), the temperature coefficient of offset (TCO) in always-on sense mode is similar to that in full power sense mode. Specifically, the TCO distribution across 30 samples demonstrates that the worst-case one-sigma TCO values are 0.042°/s/K and 0.044°/s/K, respectively.

A comparison with state-of-the-art interface ICs is shown in Table 1. Compared to previous works [3-7], the maximum power reduction in always-on mode is improved from 1.8X to 4.4X, and the noise-power efficiency is improved by 3X from 65.7pJ to 22.1pJ.

IV. Conclusion

By dynamically synchronizing the interface circuit's power with the sensor drive signal C_D, the proposed PLDA-based interface IC breaks the noise-power limitation and bandwidth degradation compared to conventional burst sensing based interface IC for the always-on sense MEMS gyroscope. Fabricated in 0.18μm BCD process, the 3-axis

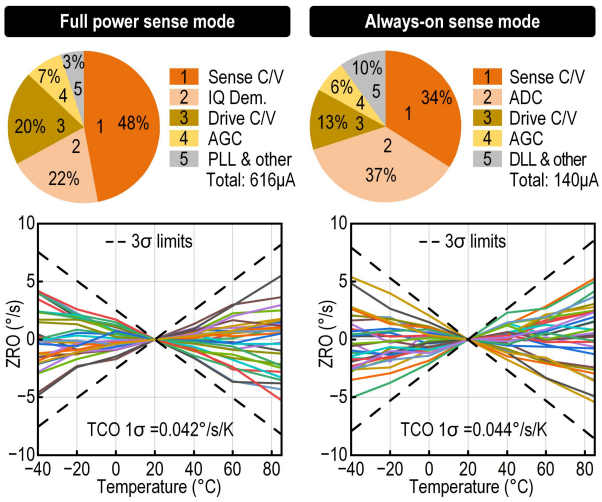

Fig. 10. Measured power breakdown and ZRO temperature drift.

TABLE I. Performance Summary and Comparison

	TIE'19[7]	STM'22 LSM6DSO16IS[4]		Bosch'23 BMI270[6]	TDK'24 ICM45686[5]	ISSCC'25[3]	This work
Process	0.35μm BCD	-		-	-	0.18μm BCD	**0.18μm BCD**
Supply voltage(V)	3	1.8		1.8	1.8	1.8	**1.8**
Number of axis	3	3		3	3	3	**3**
FP* Noise (°/s/√Hz)	-	3.4m		7m	3.8m	-	**6m**
FP* Current (μA)	-	490		900	370	-	**616**
FP* Bandwidth (Hz)	-	-		751	-	-	**550**
Full Range (°/s)	2850	2000		2000	4000	1000	**2000**
AO* Noise (°/s/√Hz)	31m	12m**	24m**	10m	-	6m	**8.5m**
AO* Current (μA)	406	320	290	600	210	539	**140**
AO* Bandwidth (Hz)	50	26**	6.25**	751	25**	500	**260**
AO* Power reduction	-	1.5X	1.7X	1.5X	1.8X	-	**4.4X**
AO* FoM*** (pJ)	624.5	225.9	835.2	65.7	-	86.8	**22.1**

* **FP**=Full power mode; **AO**=Always-on mode (or low power sense for [3,6,7]);

** AO Noise is calculated by RMS-noise / (1.57 × Bandwidth)$^{0.5}$; AO Bandwidth is calculated by ODR/2;

*** $\text{FoM}=\frac{\text{Power}}{\text{Axis}\times\text{Bandwidth}\times\text{DR}}$; $\text{DR}=\frac{\text{Full Range}}{\text{Noise}\times\sqrt{\text{Bandwidth}}}$;

system achieves 8.5m°/s/√Hz noise floor and 140μA current consumption with 260Hz signal bandwidth.

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