A 16-21.5 GHz 1.59-dB NF_{min} LNA Using Truly-Anti-Phase Noise-Cancelling Technique for Satellite Communication in 40nm CMOS

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***Abstract*—This paper proposes a truly-anti-phase noise-cancelling low noise amplifier (LNA) designed for satellite communication applications. Compared to the traditional noise-cancelling LNAs, the proposed LNA exhibits minimal gain-phase mismatch between its two noise paths, thus achieving a lower noise figure (NF). Moreover, a dedicated phase compensation technique is employed to compensate for extra phase difference caused by the inter-stage matching network and transistors. Fabricated in a 40-nm bulk CMOS process, the proposed LNA prototype achieves a measured bandwidth (BW) of 16-to-21.5 GHz (29.3%), NF of 1.59-to-2.1 dB, maximum gain of 19.3 dB, while consuming 23 mA from 1.1 V power supply. The circuit also demonstrates excellent linearity, with EVM below -31 dB for 6-Gbps 64-QAM and 8-Gbps 256-QAM signals.**

***Index Terms*—satellite communication, low noise amplifier, noise cancellation, millimeter-wave, CMOS**

I. Introduction

The need for cost-effective, large-scale phased arrays demands high-performance low-noise amplifiers (LNAs). The noise figure (NF) of the LNA directly determines the system sensitivity and the number of array elements needed for a given signal-to-noise ratio (SNR) [1]. Thus, lowering the NF is crucial for reducing system cost and power in Ka-band downlink satellite communication (17.7-21.2 GHz).

In general, the noise-cancelling architecture can achieve a lower NF. However, many implementations suffer from a degraded NF due to gain-phase mismatch. Fig.1 shows the noise analysis of two conventional noise-cancelling LNA circuits. The noise voltage at the drain of M_1 is $V_{n1} = I_{n1}Z_1$, where I_{n1} denotes the noise current of transistor M_1 and Z_1 is the load impedance at its drain. For cancellation, V_{n1} travels along two paths (the main path and the auxiliary path) to be subtracted at the output. Ideally, V_{n1} can be completely canceled when the magnitudes of the gains along the two paths are equal. However, in practice, a phase error between the paths often persists even with matched gain magnitudes. This gain-phase mismatch results in a timing difference (Δt) between two differential output noise voltage, thus causing incomplete cancellation of V_{n1} and a consequent degradation of the NF. In the dual-path noise-cancelling LNA (Fig.1, top), M_2 employs a resistive feedback configuration, which yields a low input impedance ($Z_{in.M2}$). Consequently, the first major

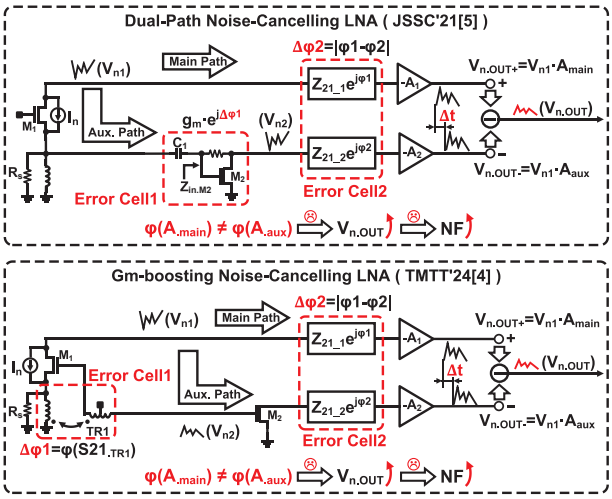

Fig. 1. Noise figure degradation in conventional noise-cancelling LNA topology.

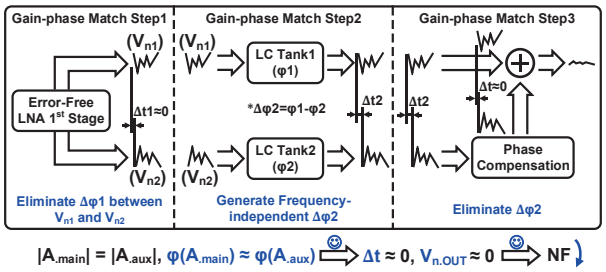

Fig. 2. Operating principle of the proposed truly-anti-phase noise-cancelling LNA.

source of phase difference ($\Delta\phi 1$) is attributed to the voltage division effect of the C_1 and $Z_{in.M2}$. The second primary phase difference ($\Delta\phi 2$) arises from the mismatch in the inter-stage matching network. In the gm-boosting noise-cancelling LNA (Fig.1, bottom), $\Delta\phi 1$ is equal to the phase of the S21 of the input transformer (TR1), and $\Delta\phi 2$ stems from the mismatch in the inter-stage matching network. This introduces a large Δt between the output noise in such conventional structures, which significantly worsens the NF.

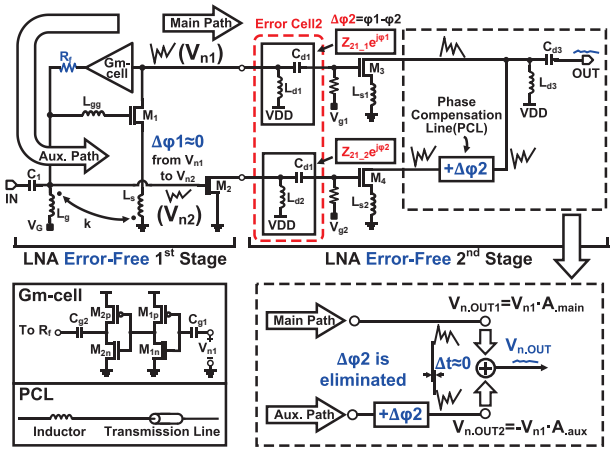

Fig. 3. Circuit schematic of the proposed truly-anti-phase noise-cancelling LNA.

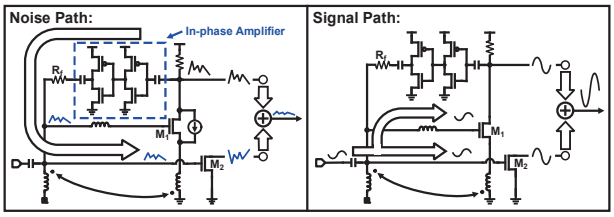

Fig. 4. Phase and gain requirements for noise path and signal path of the proposed LNA.

II. Circuit Implement and Operating Prinlicle

A. Circuit and operating principle of the proposed LNA

To address challenges above and minimizing the NF, a gain-phase match noise cancelling LNA structure is proposed in this paper.

The LNA operating principle is shown in Fig.2. Based on the analysis of conventional noise-cancelling architectures, the degradation of the NF is primarily influenced by two main phase errors. The first phase error typically occurs in the first stage of the LNA, while the second phase error is introduced by the interstage matching network. Therefore, this work designs an error-free first-stage LNA circuit to eliminate $\Delta\phi 1$. A first-order LC network is then employed to generate $\Delta\phi 2$, which is independent of frequency, and this error is subsequently compensated by the phase compensation technique. It is worth noting that the reason for not choosing to compensate for all phase errors solely with the phase compensation technique. It is because that compared to relying entirely on such compensation, an error-free first-stage circuit design is more robust. Moreover, if the phase compensation technique were required to correct an excessive amount of phase error, its associated area cost and loss would become non-negligible.

The full schematic is shown in Fig.3. A noise-canceling topology based on a resistive-feedback common-source (CS) stage is adopt. In the circuit, the Gm-cell is implemented by complementary NMOS-PMOS structure for power saving, while the phase compensation line (PCL) is realized by a series combination of an inductor and a transmission line.

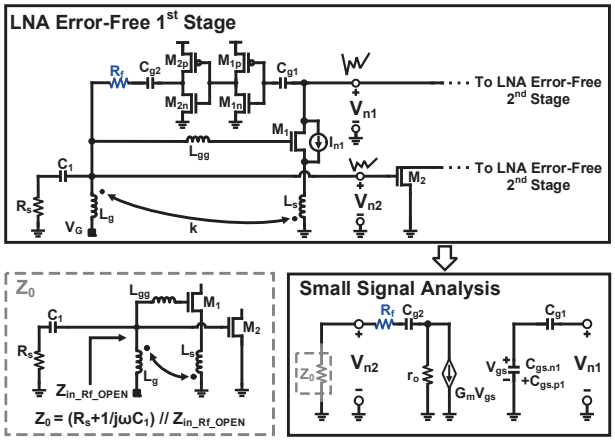

Fig. 5. Operating principle of eliminating phase shift from V_{n1} to V_{n2} in LNA error-free first stage.

Fig.4 explains the phase and gain requirements for noise path and signal path of the proposed LNA. Thanks to the Gm-cell being an inverting amplifier implemented with a two-stage cascaded inverter, the signal and noise at its output satisfy the phase and gain requirements for noise cancellation. This ensures that the noise-cancelling architecture can achieve its intended functionality. Moreover, the high output impedance of the Gm-cell shields the noise from R_f, thereby eliminating the trade-off between the noise contribution of Rf and the input impedance bandwidth [2].

B. The first step in gain-phase matching

The first step in gain-phase matching is to design a first-stage LNA circuit that is inherently free of phase error. Fig.5 shows the schematic of the first-stage circuit proposed in this work, along with its corresponding small-signal equivalent circuit. The figure illustrates the cancellation mechanism of the gain-phase error from V_{n1} to V_{n2}. From the small-signal model, the transfer function from V_{n1} to V_{n2} can be expressed by

$$\frac{V_{n2}}{V_{n1}} \approx \alpha \cdot G_m \cdot r_o \cdot \beta \tag{1}$$

Where α and β are voltage division coefficients, and $G_m \cdot r_o$ is the gain of the Gm-cell. α and β can be expressed by

$$\alpha = \frac{C_{g1}}{C_{g1} + C_{gs.n1} + C_{gs.p1}} \tag{2}$$

$$\beta = \frac{j\omega Z_0 C_{g2}}{1 + j\omega C_{g2}(R_f + Z_0)} \tag{3}$$

Obviously, both α and Gm·ro are purely real. A key design consideration is how to eliminate the phase of β, so that the transfer function shown in equation (1) becomes essentially a

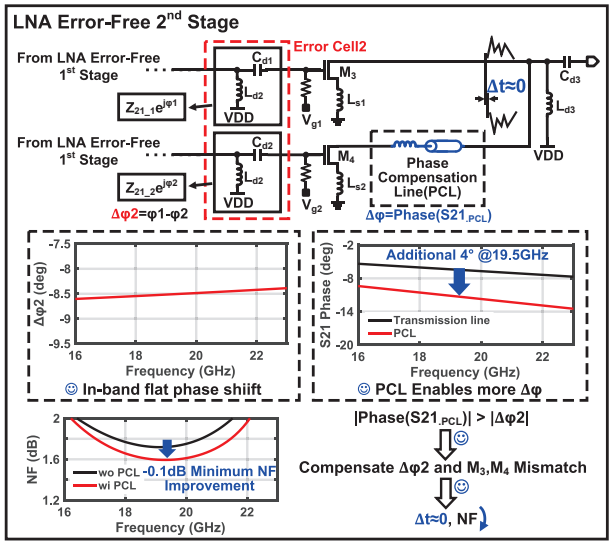

Fig. 6. Circuit schematic of LNA error-free second stage, PCL Implementation and simulated NF with phase compensation.

constant.When the selected R_f is sufficiently large (approximately 10 kΩ), equation (3) can be rewritten as:

$$\beta = \frac{j\omega Z_0 C_{g2}}{1 + j\omega C_{g2}(R_f + Z_0)} \approx \frac{Z_0}{R_f + Z_0} \tag{4}$$

To ensure input matching, the imaginary part of Z_0 will be much smaller than R_f. Consequently, β is approximately equal to the ratio of the real part of Z_0 to R_f, which is a pure real number. This results in negligible gain-phase mismatch between V_{n1} and V_{n2}.

C. The second step in gain-phase matching

Fig.6 illustrates the detailed circuit implementation and corresponding simulation results of the LNA's second stage. In the second step of the gain-phase matching process, the inevitable parasitic effects introduced by the layout and the transistors themselves make a purely analytical design infeasible; therefore, this step is necessarily accomplished with the aid of simulation.

Compared to transformer matching, a first-order LC network is capable of generating a frequency-independent $\Delta\phi 2$. Simulation result shows that the phase error between the two LC networks in this design remains at approximately -8.5° over the 16-to-23-GHz frequency range, which is a very flat phase shift. Fig.6 also shows the PCL implementation and simulation results. Attributed to its series inductor, the PCL achieves a higher phase shift than a transmission line in the same area. It delivers an in-band phase shift of -14° to -10°, which compensates for both $\Delta\phi 2$ and the mismatch from M_3 and M_4, optimizing NF.

III. Measurement Result

The proposed truly-anti-phase noise-cancelling LNA is fabricated in a 40-nm bulk CMOS process. As shown in the die

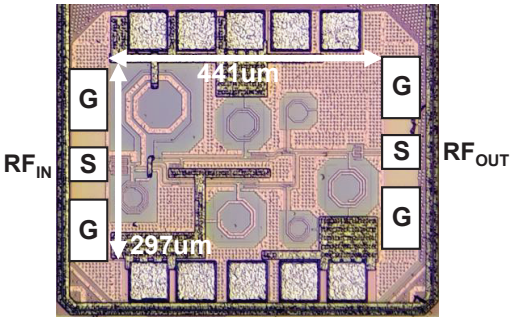

Fig. 7. LNA chip micrograph.

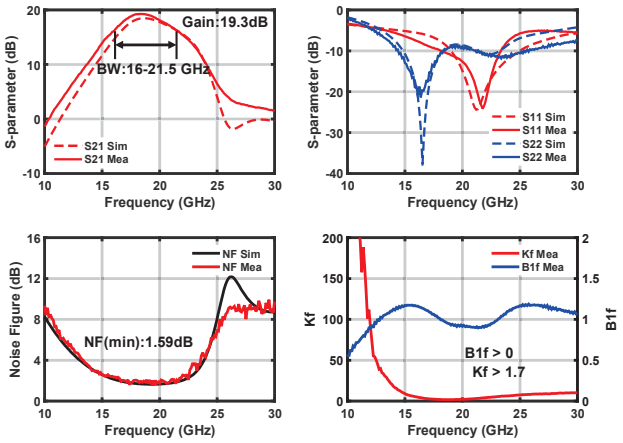

Fig. 8. S-parameter and NF measurement results.

micrograph in Fig.7, the core circuit occupies a compact core area of 0.13-mm^2, demonstrating the area efficiency of the design. The LNA prototype on-chip measurement is conducted in a probe station.

Fig.8 presents the measured performance of the proposed LNA. The S-parameter measurement results, obtained with the LNA drawing 25 mW from a 1.1-V supply, show that the circuit achieves a -3-dB gain bandwidth from 16-to-21.5 GHz. Within this band, the maximum power gain (S21) reaches 19.3 dB. The input reflection coefficient (S11) remains below -10 dB from 18.1-to-23.3 GHz, while the output reflection coefficient (S22) stays below -8.5 dB across an even wider range of 13.8-to-27.6 GHz. On-wafer noise measurement reveals a minimum NF of 1.59 dB with the in-band NF remaining below 2.1 dB across the entire operating band. Meanwhile, the measured stability factors (Kf and B1f) are both greater than 1.7 and 0.5, respectively, from 10 GHz to 30 GHz, confirming unconditional stability throughout the measured frequency range.

Fig.9 depicts the measured error-vector magnitude (EVM) performance of the LNA under high-order modulated signals. When driven by a 6-Gbps 64-QAM signal, the measured EVM is -31.7 dB at 17 GHz, -31.2 dB at 19 GHz, -31.9 dB at 21 GHz respectively. For an 8-Gbps 256-QAM signal, the

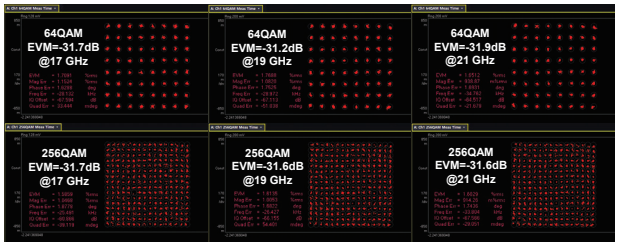

Fig. 9. Measured 6-Gbps 64-QAM and 8-Gbps 256-QAM EVM performances at multiple operation center frequencies.

TABLE I
COMPARSION WITH STATE-OF-ART LNAS

	This work	TMTT'26 [4]	JSSC'21 [5]	TMTT'24 [6]	MWTL'25 [7]
Tech.	40nm CMOS	40nm CMOS	40nm CMOS	40nm CMOS	65nm CMOS
Topology	Error-Free D-P. CS NC	D-P. CG NC	D-P. CG NC	D-P. CG NC	CS+CS
Freq. (GHz)	16-21.5	19.9-25	22.9-38.2	21.9-33.7	16-22.6
Gain (dB)	19.3	14.5	14.5	12.3	16.2
BW (GHz)	5.5	5.1	15.3	12	6.6
NF(dB)	1.59-2.1	2-2.8	2.65-4.62	2.8-4.2	1.95-3.5
NF Flatness (dB/GHz)	0.093	0.157	0.129	0.117	0.263
EVM (dB)	256QAM -31.6 @19GHz	N/A	N/A	N/A	N/A
Pdc (mW)	25	22.4	18.9	8.5	3.6
Area (mm2)	0.13	0.16	0.16	0.26	0.45#

Including Pad

corresponding EVM values are -31.7 dB at 17 GHz, -31.6 dB at 19 GHz, and -31.6 dB at 21 GHz.

Fig.10 provides a comprehensive comparison of the NF performance between the proposed LNA and recently reported state-of-art microwave and millimeter-wave LNAs, with the corresponding measurement data summarized in Table.I. The table highlights the best achieved NF and the lowest NF flatness, where NF flatness is defined as:

$$NF\ Flatness = \frac{NF(max) - NF(min)}{-3dB\ BW} \quad (5)$$

Benefiting from a low gain-phase mismatch and phase compensation technique, the proposed LNA yields significant advantages in terms of both minimum NF and NF flatness. It indicates that the topology is suitable for high performance LNA in large-scale phased array systems.

CONCLUSION

Based on the conventional resistor-feedback common-source noise-cancelling LNA structure, this work achieves a gain-phase matched noise-cancelling LNA architecture by integrating Gm-cell feedback and phase compensation techniques. Fabricated in 40-nm standard CMOS process, the proposed LNA exhibits a peak gain of 19.3 dB, a -3-dB bandwidth from 16 GHz to 21.5 GHz from a 1.1-V supply. Furthermore, this LNA achieves a minimum in-band NF of 1.59 dB with an NF flatness of less than 0.1 dB. Finally, this LNA is measured using 8-Gbps 256-QAM modulation signal

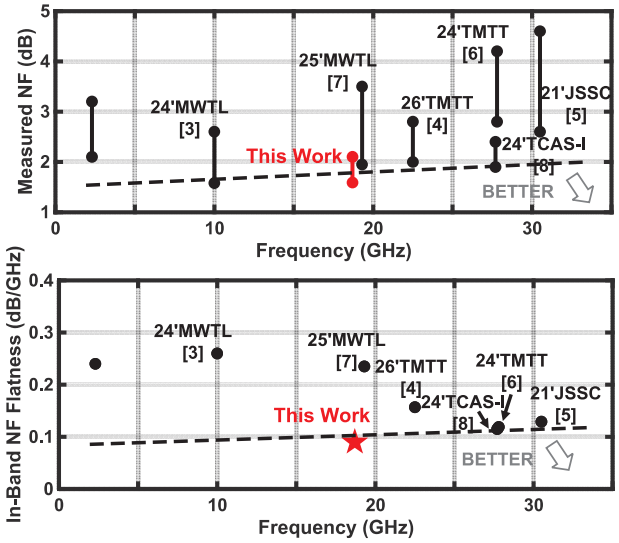

Fig. 10. NF performance compared with state-of-art LNAs

with EVM of -31.6 dB at 19 GHz demonstrating it's capability for ultra high speed satellite communication.

ACKNOWLEDGMENT

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