A 25-GHz Ultra-Compact, VSWR-Resilient Asymmetrical Doherty Power Amplifier with Reconfigurable Inductorless Adaptive Biasing Supporting 12 Gbps 64-QAM

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***Abstract*— This paper presents a 25 GHz ultra-compact asymmetrical Doherty power amplifier (DPA) with high resilience to load voltage standing wave ratio (VSWR) variations, enabled by a simultaneously conjugate- and load-pull-matched Main path. A compact high-speed Reconfigurable Adaptive Biasing (RAB) technique, based on active inductive peaking, is introduced to simultaneously improve linearity under VSWR mismatches and substantially extend the modulation bandwidth without causing much chip area penalty. At 25GHz, the proposed DPA achieves 27.5% PAE at 18.8dBm OP_{1dB}, and 16% and 14.5% PAEs at 6dB and 8dB power back-off (PBO), respectively. Over a 3:1 VSWR circle, the PA shows maximum variations of only 1.45dB in gain and 2.1dB in OP_{1dB}. With a 64-QAM 2-GSym/s modulated signal across a 3:1 VSWR circle, the average output power and PAE vary between 11.6-12.8dBm and 12-13.16%, respectively. To the best of the authors' knowledge, this work reports the first VSWR-resilient PA with data rates up to 12 Gbps, while simultaneously achieving a ∼5× smaller core chip area than prior-art VSWR-resilient PBO efficient PAs.**

***Keywords*— Adaptive Bias, CMOS, Power Amplifiers, VSWR.**

I. Introduction

Next-generation wireless systems, including SATCOM Non-Terrestrial Networks (NTNs) and Terrestrial Networks (TNs), rely on large antenna arrays to overcome severe path losses and meet stringent link-budget requirements. In these systems, dense antenna arrays lead to strong element antenna mutual coupling, causing the active load impedance seen by each power amplifier (PA) to vary with frequency, scanning angle, beam configuration, and element position. Such load variations directly degrade PA linearity, power gain (PG), and efficiency, reducing array linear Effective Isotropic Radiated Power (EIRP), while also complicating array calibrations. These effects are even more critical in 5G/6G TN and NTN links targeting multi-Gb/s modulations with large peak-to-average power ratios (PAPRs).

Consequently, integrating antenna VSWR resilience, high linearity, compactness, deep PBO efficiency, and high modulation speed within a single PA solution would significantly benefit future mm-Wave phased-array systems. Among PBO-efficient architectures, the Doherty power amplifier (DPA) remains one of the most adopted solutions. However, prior load-resilient DPA solutions, such as [1], require large chip area and are not well suited for compact large-scale arrays. Similar limitations apply to Load Modulated Balanced Amplifier (LMBA)-based architectures [2], [3], [4], [5], which rely on multi-path operation and

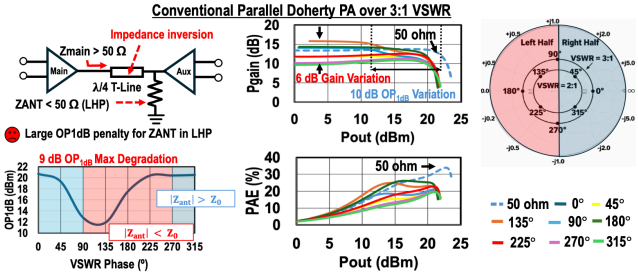

Fig. 1. Power Gain (PG) and PAE variations of a 25-GHz standard parallel DPA extracted/EM-simulated in GF 22nm FDSOI over a 3:1 VSWR circle and its associated linearity degradation in the LHP of the Smith chart.

bulky passive structures. Non-reciprocal interface networks [6], [7] improve load resilience, at the expense of lossy and large on-chip passives. Other compact VSWR-resilient PAs achieve robustness at the expense of output power due to feedback-induced output-impedance reduction [8], or rely on reconfigurable matching networks that degrade efficiency and linearity [9], while none of them addresses the PBO efficiency issue. Conversely, compact DPAs such as [10] and [11] provide good PBO efficiency enhancement, but do not minimize load VSWR sensitivity.

In addition, the achievable modulation bandwidth of DPAs is often limited by the adaptive biasing network. Although adaptive biasing is essential to optimize Auxiliary PA turn-on and preserve linearity and efficiency over PBO, conventional inductorless implementations degrade the envelope response and limit the modulation speed.

To address these challenges, this work proposes an ultra-compact output-matched asymmetrical parallel DPA with a single-transformer footprint output matching network (OMN) and a high-speed inductorless reconfigurable adaptive biasing. The proposed architecture enables both small-signal and large-signal load insensitivity by employing a Main PA with simultaneous conjugate- and load-pull-matching, while maintaining the efficient large signal performance. To improve wideband modulated performance, a compact high-speed reconfigurable adaptive biasing (RAB) circuit is incorporated with active inductive peaking technique. This approach substantially extends the modulation bandwidth without using passive inductors for chip area saving [12]. The RAB circuit is fully reconfigurable to optimize the Aux PA turning-on and thus the whole PA linearity under different

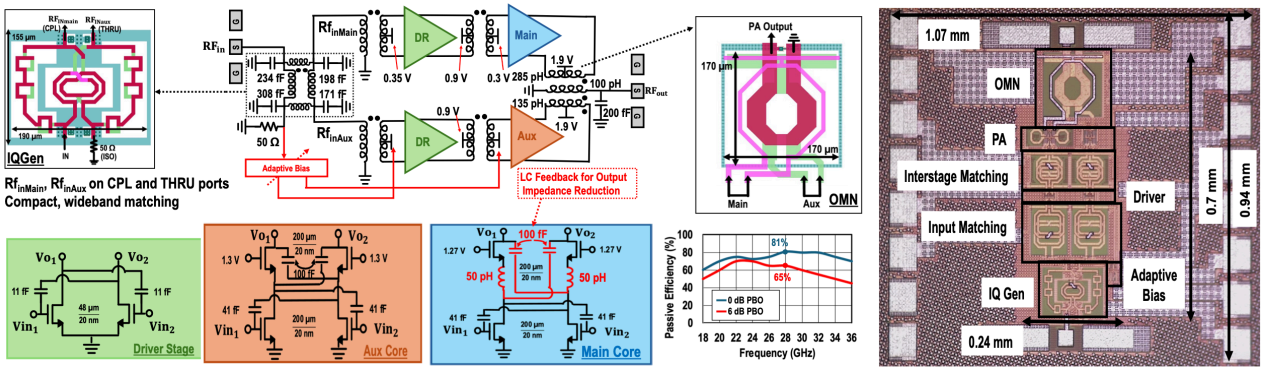

Fig. 2. Top level schematic of the VSWR-resilient DPA, the TFQC IQGen network and the compact parallel Doherty output network and its passive efficiency (Left) and Chip microphotograph (Right).

VSWR conditions. As a result, the proposed PA achieves load insensitivity in both the small- and large-signal regimes, while preserving Doherty PBO efficiency enhancement even over 3:1 VSWR, all in an ultra-compact implementation. To the best of the authors' knowledge, this is the first reported DPA that simultaneously achieves single-transformer ultra-compactness, VSWR resilience, and deep PBO efficiency enhancement while delivering high data rates up to 12 Gbps. This, in turn, makes the proposed DPA a promising candidate for large-scale arrays.

II. PA Circuit Desciption and Reconfigurable Adaptive Biasing Technique

DPAs are sensitive to antenna load variations, particularly in terms of large-signal PG and OP_{1dB}, often due to the impedance inverters in the output networks. Parallel DPAs typically exhibit early compression for mismatched loads in the left half plane (LHP) of the Smith chart, whereas series DPAs often compress early in the right half plane (RHP) [13]. Fig. 1 shows the PG and PAE variations of a 25 GHz standard parallel DPA (SPDPA), which is designed and extracted/EM-simulated in a 22nm FDSOI process over a 3:1 load VSWR circle. The PA exhibits large PG variations of 6dB, large efficiency variations of 15% for PAE_{sat} and PAE_{6dB} and large OP_{1dB} variation of 10 dB, highlighting the severe impact of load mismatches on a conventional parallel DPA.

Fig. 2 shows the proposed ultra-compact VSWR-resilient two-stage parallel DPA. For parallel Doherty PAs, since only the Main PA is on while the Aux PA is off with a high output impedance during small signal operations, an output $|S_{22}|$ matched Main PA can ensure low small-signal $|S_{22}|$ for the entire Doherty PA. For this reason, the Main PA is designed for simultaneous conjugate and load-pull matching over the frequency of interest, employing a complex LC neutralized cascode stage [8]. This network consists of a pair of series inductors and a pair of cross-coupled capacitors to form the neutralization and feedback from the CG drains to the CS drains of the cascode amplifier. In parallel, the Auxiliary PA uses a double-neutralization architecture to maintain a higher output impedance for reduced loading when it is off. The two paths are therefore intentionally unequal: the Main PA is optimized for matching and linearity,

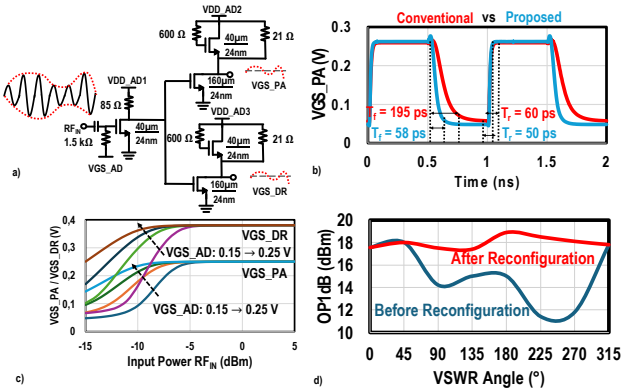

Fig. 3. a) Proposed RAB schematic, b) simulated output rise and fall time of the proposed active inductive peaking (blue) and the conventional adaptive bias (red) using an OOK-modulated signal as PA's input, c) simulated output DC voltage response versus input power when VGS_AD is swept from 0.15 to 0.25 V and d) EM simulated OP_{1dB} variation over 2:1 VSWR before (blue) and after (red) reconfiguration.

while the Auxiliary PA is designed for higher efficiency and delivering more than half of the total PA P_{sat}. Consequently, the proposed Doherty PA is asymmetrical. When only the Main PA is active, its LC-neutralization feedback ensures the overall DPA output matching and therefore its small-signal robustness to antenna VSWR. At the peak power, when both the Main and Auxiliary PAs are active, the same feedback mechanism continues to preserve favorable large-signal output matching, while Doherty active load modulation provides the desired PBO efficiency enhancement. The driver stages are implemented as cross-coupled capacitively neutralized differential common-source amplifiers, while the IQ generator uses a transformer-based quadrature coupler (TFQC) [14], simultaneously achieving a compact implementation with symmetric routing and wideband magnitude/phase balances between the Main and Auxiliary PA paths.

Fig. 3(a) presents the proposed high-speed reconfigurable adaptive-biasing (RAB) circuit. Unlike [12], where the gain peaking effect is achieved using a physical inductor at its second stage with a large area penalty, the proposed RAB adopts an active inductor for significant bandwidth extension and rise/fall-time reduction in a compact implementation

[15]. Fig. 3(b) compares the simulated transient response of the conventional adaptive biasing circuit [10] and proposed RAB under OOK waveform to emulate the extreme cases of envelope variation for complex QAM modulations, which show t_{rise}/t_{fall} as 60ps/195ps vs. 50ps/58ps for conventional AB and RAB respectively, thereby achieving a substantial speed improvement.

Besides extending the AB bandwidth, RAB provides large-signal reconfigurability. As shown in Fig. 3(c), by increasing the DC gate bias of the first stage (VGS_AD), which changes the RAB's output slope response with respect to the input power, the Auxiliary PA turns on at deeper back-off, thereby adapting the impedance modulation seen by the Main PA according to its compression point. This mitigates the early Main-PA compression that occurs for mismatched loads in the LHP of the Smith chart, effectively relaxing the intrinsic load-sensitivity tradeoff of conventional parallel DPAs. Fig. 3(d) reports the EM-simulated OP_{1dB} variation with and without RAB reconfiguration over a 2:1 VSWR circle. Without RAB reconfiguration, the OP_{1dB} variation is as large as 7 dB, whereas reconfiguration reduces it to only 1.5 dB, allowing the Doherty operation to remain close to the matched case even under VSWR variations.

III. Measurement Results

The proposed DPA is implemented in a 22nm FDSOI CMOS technology with a core area of 0.168 mm^2 (Fig. 2). This footprint is approximately 5× smaller than any reported VSWR-resilient PA architectures with enhanced PBO efficiency enhancement [1]-[5], while remaining comparable to the reported ultra-compact DPAs [10], [11]. The small-signal performance is shown in Fig. 4(a). The PA achieves a peak PG of 14 dB at 26 GHz, the S_{11} and S_{22} remain below -10 dB from 24 GHz to 40 GHz and from 25 GHz to 40 GHz, respectively. The large-signal performance at 25 GHz indicates that the DPA achieves an OP_{1dB} of 18.8 dBm with a PAE_{OP1dB} of 27.5 % and a PAE_{6dB} and PAE_{8dB} of 16 and 14.5%, respectively (Fig. 4(b)). The PA is also tested across different carrier frequencies, with the performances summarized in Fig. 4(c).

The VSWR resilience is evaluated using a Maury load-tuner at the PA's output. The load-tuner is swept across 3:1 VSWR circle with 45° phase steps. Fig. 4(d) illustrates the impact of the RAB tuning on the PA's linearity. At a VSWR of 3:1 and a phase of 135°, the OP_{1dB} improves by 8.4 dB following reconfiguration, as indicated by the shifted PG curve (red line) relative to the not reconfigured case (blue line). In contrast, a simulated SPDPA PG (orange line), normalized to the proposed DPA gain, has 9.1 dB lower OP_{1dB} compared to the proposed DPA with RAB. Fig. 4(e) shows the PA performance under a 3:1 VSWR circle at 25 GHz carrier frequency after RAB reconfiguration. The PG, OP_{1dB} and PAE_{6dB} variations remain below 1.45 dB, 2.1 dB and 4%, respectively. A summary of the PAE_{OP1dB}, PAE_{6dB}, PAE_{8dB}, PG and OP_{1dB} across angles is provided in Fig. 4(f). Overall, the PA consistently maintains its competitive performance across all VSWR angles.

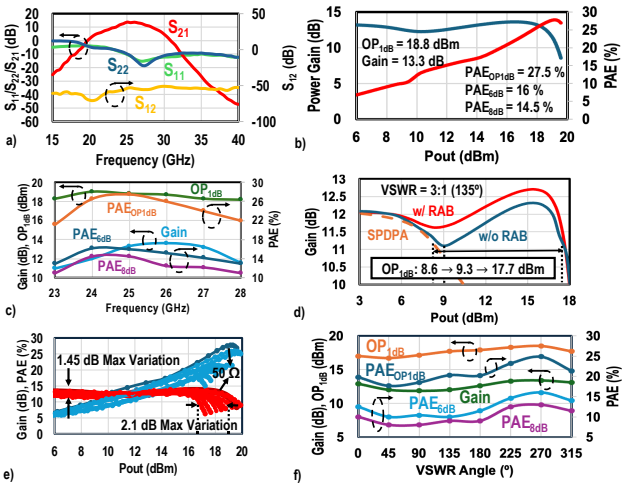

Fig. 4. Measured PA performance: (a) small-signal S-parameters, (b) large signal response under 50Ω at 25 GHz (c) and across frequency, (d) OP_{1dB} recovery with RAB (red) vs. without RAB (blue) and simulated normalized SPDPA gain (orange) under 3:1 VSWR at 135°, (e) PA's gain and PAE at 25 GHz under 3:1 VSWR with a phase step of 45°, (f) Measured PA PG, OP_{1dB}, PAE_{OP1dB}, PAE_{6dB} and PAE_{8dB} under 3:1 VSWR at 25GHz.

The PA is further tested with single-carrier 64-QAM modulation signals at a carrier frequency of 25 GHz. As shown in Fig. 5, for symbol rates of 100 MHz (0.6 Gbit/s) and 2 GHz (12 Gbit/s), the PA achieves average output powers (P_{AVG}) of 13.75 and 13.25 dBm, respectively, with corresponding average efficiencies (PAE_{AVG}) of 15.6 and 15.45% under 50Ω load. Under the 3:1 VSWR circle over 360°, the measured modulation P_{AVG} is 12.05-13.34 dBm with 12.3-13.5% PAE_{AVG} at 100 MHz and is 11.6-12.8 dBm with 12-13.16% PAE_{AVG} at 2 GHz symbol rate. Even for high speed 64QAM modulation (2GHz symbol rate = 12 Gbit/s), the DPA maintains state-of-the-art performances both under 50Ω and 3:1 VSWR, emphasizing the effectiveness of the VSWR-resilient Doherty PA and RAB's high-speed envelope tracking capability.

IV. Conclusion

Fig. 6 compares the proposed ultra-compact VSWR-resilient DPA versus existing state-of-the-art mm-Wave VSWR-resilient PAs with PBO efficiency enhancement in the same frequency band. The proposed design achieves the most compact footprint, while delivering competitive modulated output power and efficiency for 64QAM signals at 2GHz symbol rate (12Gbit/s), resulting in significantly higher power density and modulation speed among others. Fig. 7 compares the power density of the proposed PA versus PAs with PBO efficiency enhancement with and without VSWR resilience. In addition, the PA exhibits significantly reduced PG variations over 3:1 VSWR, enabled by simultaneous conjugate and load-pull matching of the main PA. To the best of our knowledge, this work reports the first Doherty PA that is simultaneously ultra-compact (single-transformer footprint),

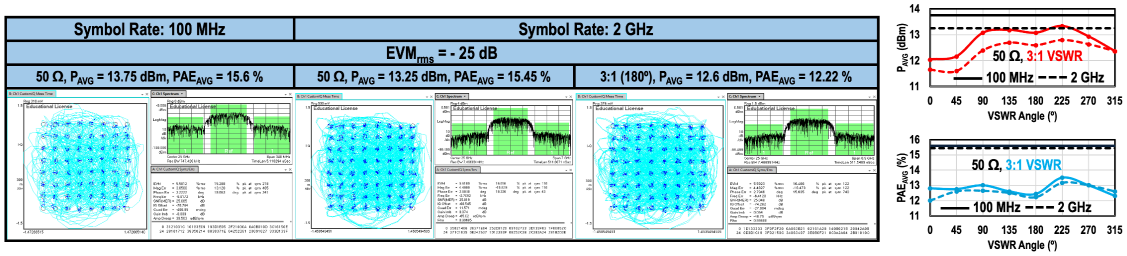

Fig. 5. Modulation results with 200 MHz and 2 GHz single-carrier 64-QAM signals at 25 GHz for 50Ω and 3:1 VSWR loads with EVM_{rms} = -25 dB.

	This Work				M. Pashaeifar ISSCC 2021 [5]		G. Diverrez EuMC 2022 [2]#		G. Diverrez RFIC 2024 [3]#		C. Chappidi VLSI 2019 [16]#	
Technology	22 nm SOI				40 nm		28 nm SOI		28 nm SOI		65 nm	
Architecture	S_{22}-Matched Ultra-Compact Asymmetrical Doherty PA				TX with Doherty Balanced PA		Balanced PA		Inductive Doherty PA		Broadband Doherty-like	
Supply (V)	1.9				1		2		2		1.1	
Freq. (GHz)	25				26		26		28		28	
Gain (dB)	13.3				21.8 (TX)		20		22		15*	
OP1dB, 50Ω (dBm)	18.8				20		20.5[b]		19.8		19	
OP1dB, 3:1 VSWR (dBm)	> 16.7				N/A		18.5 - 19.5[a,b]		> 18.2[a]		> 17 (4:1 VSWR)	
PAE1dB, 50Ω (%)	27.5				29[a]		39[a]		34.4[a]		21.6	
ΔPG, 3:1 VSWR	1.45				1.3		N/A		N/A		2*	
Modulation	Single-Carrier 64-QAM				Single-Carrier 64-QAM		64-QAM 5G NR FR2		64-QAM 5G NR FR2		64-QAM OFDM	
Load Impedance	50Ω		3:1 VSWR		50Ω	3:1 VSWR	50Ω	3:1 VSWR	50Ω	3:1 VSWR	50Ω	3:1 VSWR
Frequency (GHz)	25				27		29	N/A	24	N/A	28	N/A
Symbol Rate (MHz)	100	2000	100	2000	800	100	500	N/A	200	N/A	1000	N/A
EVM_{rms} (dB)	-25	-25	< -25	< -25	-24.6	< -25	-21.37	N/A	-22	N/A	-22.2	N/A
$Pout_{avg}$ (dBm)	13.75	13.25	12.05 - 13.34	11.6 - 12.8	11.36	> 10*	11.58	N/A	11.8	N/A	7.5	N/A
PAE_{avg} (%)	15.6	15.45	12.3 - 13.5	12 - 13.16	17.6[b]	N/A	N/A	N/A	11.9	N/A	5.1	N/A
Core Area (mm^2)	0.168				1.38		0.9		0.82		1.35 (chip area)	
CW Power Density (W/mm^2)***	0.45		> 0.278		0.072	N/A	0.125	> 0.078	0.116	> 0.08	0.058	> 0.037
Modulation Power Density (W/mm^2)****	0.14	0.125	> 0.095	> 0.094	0.01	> 0.0072	0.016	N/A	0.018	N/A	0.004	N/A

* Estimated from plots
** EVMrms = - 24 dB
[a] Psat or PAEsat
[b] Drain Efficiency
*** CW Power Density = OP1dB (W)/Corea Area (mm^2)
**** Modulation Power Density = P_{AVG} (W)/Corea Area (mm^2)
# No Modulation Measurements over VSWR

Fig. 6. Comparison table with the state-of-the-art mm-Wave VSWR-resilient PAs with PBO-enhancement techniques across 24-28 GHz.

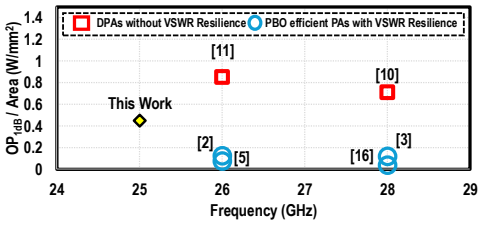

Fig. 7. CW Power Density ($\frac{OP_{1dB}}{Area}$) compared to the state-of-the-art PA designs with PBO efficiency enhancement.

fully VSWR resilient and able to deliver data rates up to 12 Gbps, key features for next-generation phased arrays.

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REFERENCES

[1] N. S. Mannem, M.-Y. Huang, T.-Y. Huang, and H. Wang, "A reconfigurable hybrid series/parallel doherty power amplifier with antenna vswr resilient performance for mimo arrays," *JSSC*, vol. 55, no. 12, pp. 3335–3348, 2020.

[2] G. Diverrez, E. Kerhervé, and A. Cathelin, "A 24-31ghz 28nm fd-soi cmos balanced power amplifier robust to 3:1 vswr for 5g application," in *EuMC*, 2022, pp. 496–499.

[3] G. Diverrez *et al.*, "A 22-44 ghz 28nm fd-soi cmos 5g doherty power amplifier with wideband pae6dbpbo enhancement and 3:1 vswr resiliency," in *RFIC*, 2024, pp. 131–134.

[4] M. Pashaeifar *et al.*, "A 25.2dbm psat, 35-to-43ghz vswr-resilient chain-weaver eight-way balanced pa with an embedded impedance/power sensor," in *ISSCC*, vol. 67, 2024, pp. 532–534.

[5] ——, "A 24-to-30ghz double-quadrature direct-upconversion transmitter with mutual-coupling-resilient series-doherty balanced pa for 5g mimo arrays," in *ISSCC*, vol. 64, 2021, pp. 223–225.

[6] M. Ghorbanpoor *et al.*, "33.2 an infinite-loop cmos-compatible isolator enabled true vswr-resilient power amplifier for 6g fr3 in massive mimo and phased-array systems," in *2026 ISSCC*, vol. 69, 2026, pp. 564–566.

[7] M. Pashaeifar *et al.*, "A millimeter-wave power amplifier with an integrated cmos isolator/circulator/receiver," *JSSC*, pp. 1–13, 2025.

[8] M. Eleraky, T.-Y. Huang, and H. Wang, "An ultra-compact wideband load-insensitive complex-cascode lc-neutralized power amplifier for 4:1-vswr-resilient operations in large-scale phased arrays," in *ISSCC*, vol. 68, 2025, pp. 1–3.

[9] E. Liu, F. Svelto, and H. Wang, "A 24 ghz compact 3:1 vswr-resilient power amplifier with a reconfigurable output matching network and integrated power sensors," in *ESSERC*, 2025, pp. 621–624.

[10] E. Liu and H. Wang, "32.9 an ultra-compact 28ghz doherty power amplifier with an asymmetrically-coupled-transformer output combiner," in *ISSCC*, vol. 67, 2024, pp. 536–538.

[11] H. Oh *et al.*, "32.2 a 24.25-to-29.5ghz extremely compact doherty power amplifier with differential-breaking phase offset achieving 23.7% paeavg for 5g base-station transceivers," in *ISSCC*, vol. 67, 2024, pp. 522–524.

[12] X. Zhang, H. Guo, and T. Chi, "A millimeter-wave four-way doherty power amplifier with over-ghz modulation bandwidth," *JSSC*, vol. 59, no. 12, pp. 3898–3914, 2024.

[13] S. Hu, S. Kousai, and H. Wang, "Antenna impedance variation compensation by exploiting a digital doherty power amplifier architecture," *TMTT*, vol. 63, no. 2, pp. 580–597, 2015.

[14] B. A. Abdelmagid and H. Wang, "A compact 48–63 ghz 3-db transformer-based quadrature coupler with arbitrary transformer coupling coefficient in 22-nm cmos fdsoi," *MWTL*, vol. 34, no. 10, pp. 1155–1157, 2024.

[15] B. Razavi, "The active inductor [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 12, no. 2, pp. 7–11, 2020.

[16] C. R. Chappidi *et al.*, "Multi-port active load pulling for mm-wave 5g power amplifiers: Bandwidth, back-off efficiency, and vswr tolerance," *TMTT*, vol. 68, no. 7, pp. 2998–3016, 2020.