# A 14-b 3-MS/s ±5-V 9.2-nV/√Hz Cryo-CMOS Digital-to-Analog Converter for Ion Shuttling

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***Abstract*—This work presents a Digital-to-Analog Converter (DAC) designed to control the DC electrodes in ion-trap quantum computers at cryogenic temperatures down to 4 K. It uses an R-βR DAC comprising high-voltage switches and linearized resistors to generate a high-voltage output without relying on a noisy analog output amplifier, thus achieving both low noise and low power. Implemented in 160-nm technology, the chip dissipates 2.85 mW from a ±5-V supply with a DAC area of 0.23 mm². After calibration, it reaches ±0.3 LSB INL and ±0.5 LSB DNL at 14-b resolution over a ±5-V output range, an SFDR of 84 dBc at an output data rate of 3 MS/s, and an output noise of 9.2 nV√Hz at 100 kHz. These results establish this architecture as a strong candidate for scaling trapped-ion quantum computers.**

***Keywords*—*Trapped-Ion Quantum Computing, Ion Shuttling, Digital-to-Analog Converter, Cryogenic Electronics***

## I. Introduction

Trapped-ion quantum computers (TIQC) are a promising architecture for large-scale quantum computing thanks to their long coherence times, high fidelity gate operations, and all-to-all connectivity [1]. Quantum information is stored in the electronic states of several ions. To enable proper operation, such ions are cooled to cryogenic temperatures and trapped in the potential well created by a high-voltage RF signal and the DC voltages applied to the respective RF and DC electrodes, as shown in Fig. 1 [2]. By properly varying the voltages on the DC electrodes, the electric field changes to shuttle the ions along the x-axis. This *ion-shuttling* operation is used to bring ions into specific regions, e.g., for reading them out or for interacting with other ions, thus representing a crucial component of any TIQC.

Controlling the voltages on these DC electrodes poses several challenges. To enable high-fidelity qubit operations suitable for a practical computation, the noise on the DC electrodes must be kept sufficiently low (< 10 nV/√Hz) to prevent ion heating [3], especially around the axial trap frequency (in the range of a few hundred kHz), thus asking for low-noise drivers. Additionally, a high resolution (> 12b) is required to precisely position the ions [1]. Bipolar high voltages of several volts are required to achieve sufficient trapping strength, while fast-shuttling operations demand DACs with MS/s sampling rates. Furthermore, while moderate-sized cryogenic TIQCs can be directly wired to room-temperature DC-electrode drivers, this approach is not suitable for large-scale TIQCs intended for practical computation, which host hundreds of DC electrodes and would require an unfeasibly large number of wires. Operating the DC drivers at cryogenic temperatures near the qubits alleviates the wiring bottleneck, but, as the cryostat's cooling power is limited, it imposes a significant power constraint on the DC electrode drivers. In addition, CMOS transistors suffer from several cryogenic non-idealities, such as kinks in the output characteristics, subthreshold humps, and increased mismatch [4], thus making analog design challenging.

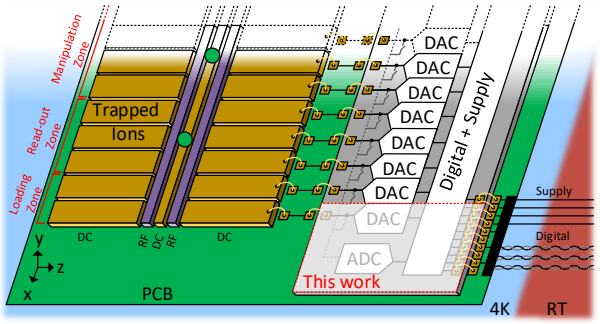


Fig. 1. Architecture of the proposed system, highlighting the focus of this paper: the DC electrodes of the ion trap are driven by the cryo-CMOS DACs presented in this paper, thus avoiding any sensitive signals wired to room temperature.

Previous DC electrode drivers address some of these challenges, but cannot satisfy all the requirements simultaneously. Conventional architectures [5] adopt DACs and amplifiers operating at room temperature that achieve high output voltages at reasonable update rates, thanks to the lack of stringent power constraints at room temperature. However, the large number of wires into the cryostat limits scalability due to thermal leakage [6]. Integrated cryogenic drivers operating inside the cryostat are then preferred for scalability [3, 7, 8, 9, 10]. To reach the required high voltages, output buffers fabricated using high-voltage processes [3] or LDMOS devices [7] are combined with a low-power R-2R DAC, which provides sufficient resolution. However, such high-voltage output amplifiers are the dominant source of thermal and flicker noise. Other architectures focus on extremely low noise, but their low update rate severely limits the ion-shuttling speed [8], or they target a much lower output voltage range [9]. The design in [10] reaches a high update rate with high resolution, but the poor INL limits the effective resolution to 11b. Moreover, the low output voltage necessitates an external high-output amplifier, which, in turn, would increase noise and power consumption.

To address those limitations, this work presents an on-chip cryogenic DAC to control the DC electrodes (Fig. 2). It employs a calibrated R-βR ladder with linearized N-poly resistors, achieving ±0.3 LSB INL and ±0.5 LSB DNL at 14b resolution, with an SFDR of 84 dBc. The throughput is 3 MS/s, while achieving 9.2 nV/√Hz at 100 kHz with a flicker-noise corner at 10 kHz when operating at 4 K, without relying on a complex output filter that would limit shuttling speed. The resistors and switches achieve ±5-V output swing with 5-V devices in a standard 160-nm technology. Thanks to the proposed high-voltage DAC architecture, noisy high-power output amplifiers are avoided, thus achieving the lowest reported noise floor at high throughput without requiring a high-voltage process or dissipating excessive power.

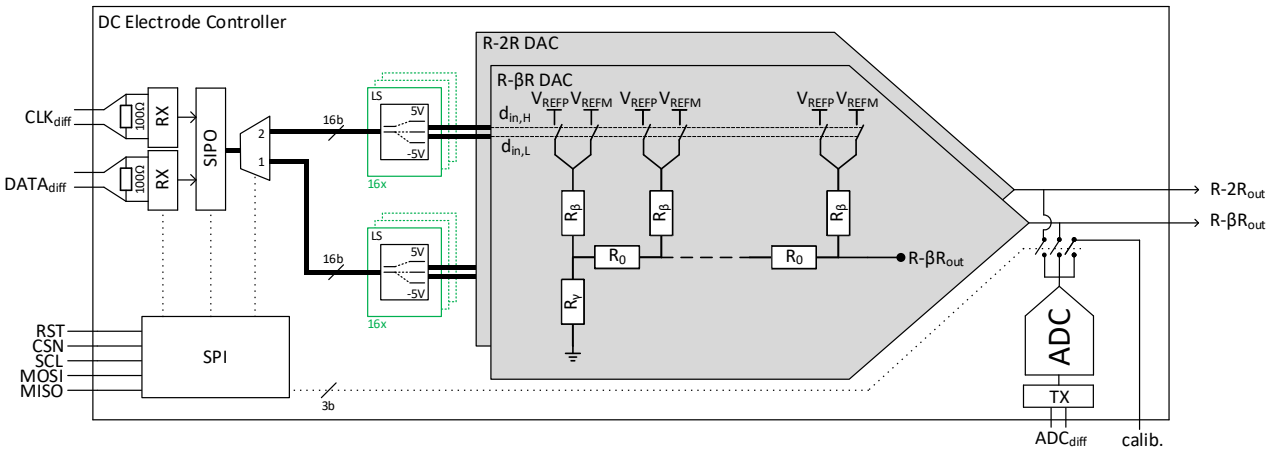


Fig. 2. Block diagram of the DC Electrode Controller. With differential LVDS receiver for CLK and DATA input, serial-input-parallel-output (SIPO), ±5V level-shifter (LS) with $d_{in,H}$ = [+5, 0] V and $d_{in,L}$ = [0, -5] V, SPI register for control settings, calibration ADC with LVDS transmitter, HV calibration switches, R-2R DAC and R-βR DAC with external reference voltages $V_{REFP}$ and $V_{REFM}$.

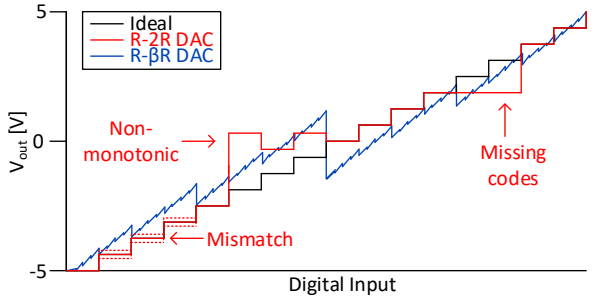


Fig. 3. Example comparison between ideal N-bit DAC characteristics vs. R-2R DAC output with non-idealities and the output of an R-βR DAC with M elements (M > N).

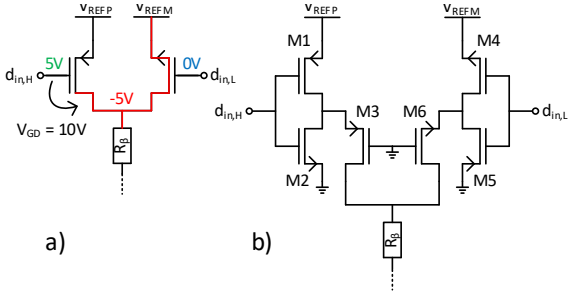


Fig. 4. Conventional HV DAC switch (a) and proposed HV DAC switch (b), $d_{in,H}$ = [+5, 0] V and $d_{in,L}$ = [0, -5] V.

## II. Proposed Digital-to-Analog Converter

### A. Architecture

Resistive R-2R ladders offer simplicity, low power, low area, and constant output impedance. However, mismatch, PVT, switch resistance, and supply impedance make them susceptible to nonlinearity, which degrades monotonicity and causes missing codes (Fig. 3). This adversely impacts the feasibility of achieving 14b resolution even at room temperature. Moreover, this effect is exacerbated at cryogenic temperatures due to the increased resistor mismatch [4]. Other architectures, such as ΣΔ DACs, can achieve high resolution and good monotonicity but require complex output filters to suppress out-of-band noise. Moreover, limit cycles and high switching activity can cause spurs that may impact qubit fidelity when they occur near the axial trap frequency.

This work uses an R-βR DAC architecture (Fig. 2). It benefits from the advantages of an R-2R DAC, while facilitating high-resolution applications after calibration, provided that the resistor ratio is carefully selected. The constant output impedance over the entire output range makes this a suitable driver for capacitors without affecting linearity and obviating the need for an output amplifier. The resistive ladder employs an M-bit binary ladder, calibrated to N-bit resolution, with $R_\beta = \beta \cdot R_0$ and $R_\gamma = \gamma \cdot R_0$. By selecting $\beta \neq 2$, $\gamma \neq 2$, and M > N, a redundancy of M-N bits is realized with overlapping steps, as depicted in Fig. 3. This enables not only robustness to mismatch [11], but also to PVT, switch resistance, and supply impedance, resulting in lower INL and DNL compared to conventional N-bit R-2R DACs. Moreover, the R-βR DAC is monotonic and exhibits no missing codes after calibration. To achieve 14b resolution, a DAC with M = 16 is selected via simulations. The resistor $R_0$ = 50 kΩ is sized as a trade-off between noise and power, with fixed β = 2.076 and γ = 2.019. The simulations used a custom-developed cryo-PDK, based on device measurements conducted at cryogenic temperatures.

To calibrate the DAC at cryogenic temperatures, an on-chip ΣΔ Analog-To-Digital Converter (ADC) can be used to measure all $2^{16}$ DAC outputs (Fig. 2). The measured transfer curve can then be projected onto an ideal N-bit DAC response using least-mean-squares regression. An additional external input signal allows calibration of the ADC. Individual DAC channels are multiplexed to the ADC via switches, allowing calibration of multichannel electrode drivers and enabling scalability.

### B. Circuit Implementation

A conventional DAC switch (Fig. 4a) with $V_{REFP}$ = 5 V and $V_{REFM}$ = -5 V requires MOS devices with a voltage rating of $V_{GDmax}$ = 10 V and $V_{DS,max}$ = 10 V. LDMOS devices can withstand such voltages, but their Lightly Doped Drain (LDD) region suffers from substrate freeze-out that results in very high on-resistance at low $V_{DS}$ but a lower output resistance at high $V_{DS}$ [12]. This makes them unsuitable as a low-ohmic, linear switch at cryogenic temperatures. Fig. 4b shows the proposed DAC switch that uses standard CMOS devices with a $V_{GDmax}$ = 5.5 V and $V_{DS,max}$ = 5.5 V. When the switch is in the conducting state, the voltage on $R_\beta$ is 5 V, while data inputs $d_{in,H}$ = 0 V and $d_{in,L}$ = -5 V. M1 and M3 are

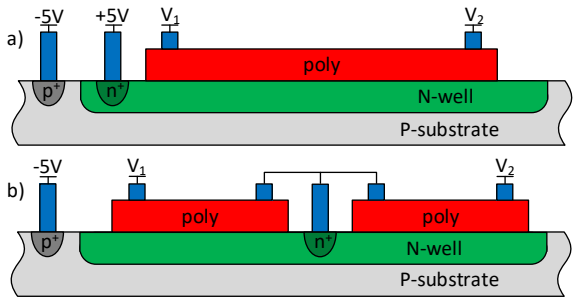


Fig. 5. Conventional N-poly resistor with bulk connection (a) and proposed N-poly resistor with split resistor (b).

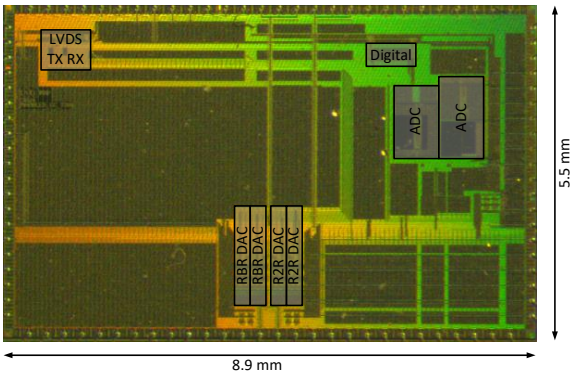


Fig. 6. Die micrograph of the prototype chip.

switched on, since the gate of M3 is connected to 0 V (= GND), whereas M2 remains off. On the contrary, M4 and M6 are off, while M5 is turned on. The critical role of M5 is to force the drain of M4 and source of M6 to 0 V, while the output is at 5 V. An analogous behavior holds when the switch is in the off state. This makes this DAC switch suitable for reference voltages that are twice the voltage rating of the transistor.

To provide the correct voltages to the data inputs, level shifters are placed between the digital controller and the switch. Conventional level shifters, such as [13], require cascode transistors to accommodate the voltage drop. This increases complexity due to the risks of overvoltage during start-up. Also, being susceptible to mismatches in rise and fall times can lead to nonlinearity in the DAC output. Therefore, a floating level shifter is used with a matching rise/fall time [14].

### C. *Linearized Resistor*

The DAC N-poly resistors suffer from voltage dependency [15]. An N-well connection, as shown in Fig. 5a, in combination with a high-voltage swing, results in significant signal-dependent resistance, leading to severe DAC nonlinearity. To mitigate this effect, the N-poly resistors are split in half, with their N-well connected in the middle via an N-well contact, as shown in Fig. 5b. This cancels the resistor voltage dependence since both resistor halves experience an almost equal opposing effect. Simulations of a 50 kΩ resistor for bias voltages from -5 V to 5 V at 4 K showed that a conventional resistor with its N-well connected to +5 V changes 18 Ω over 10 V, whereas the split resistor with N-well connection in the middle achieves 1.8 mΩ change over 10 V, thus reducing the overall voltage dependency by ~10.000× over the entire voltage range. This comes at the cost of coupling the resistor to the parasitic capacitance from the N-well to the P-substrate.

## III. Measurement Results

The fabricated 160-nm CMOS prototype occupies an active area of 6.2 mm$^2$ (Fig. 6) on a 49-mm$^2$ chip, with the area of a single R-βR DAC of 0.23 mm$^2$. The circuits exhibit a combined static power consumption of 2.85 mW when operated from a ±5 V supply. To enable 4-K noise and SFDR measurements, the chip was placed inside a Lake Shore CRX-4K cryostat, for all other measurements, the chip was submerged in liquid helium. Fig. 7 shows the INL and DNL of the R-βR DAC after calibration at 14b, performed with external equipment. Over the entire ±5 V range, the chip achieves ±0.3 LSB INL and ±0.5 DNL. The regular pattern of the INL curve shows the DAC monotonicity and the absence of missing codes. For comparison, a conventional R-2R DAC with $R_0$ = 50 kΩ and a similar layout was placed next to the R-βR DAC, achieving an INL and DNL of ±10 LSB and ±7 LSB, respectively, equivalent to a resolution of ~10.5b. This comparison shows the benefit of the R-βR architecture. Fig. 8 shows the Noise Spectral Density (NSD) at mid-code: the measured noise is 9.2 nV/$\sqrt{\text{Hz}}$ at 100 kHz with a flicker noise corner at 10 kHz at 4 K, while the NSD is 18.4 nV/$\sqrt{\text{Hz}}$ at 100 kHz at room temperature (RT). The output spectrum for a 1.275-kHz full-scale sinewave in Fig. 9 shows an SFDR of 84 dBc after calibration for an output data rate of 3 MS/s.

Table I summarizes the performance of the designed R-βR DAC and compares it with state-of-the-art cryogenic DC electrode drivers for TIQCs. Compared to designs with similar update rates [3, 7, 9, 10], this design achieves the lowest NSD.

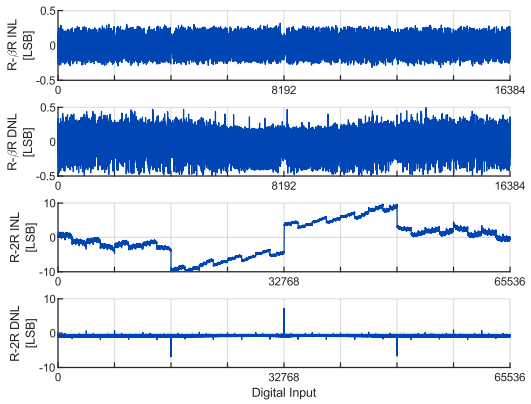


Fig. 7. INL and DNL of R-βR (after calibration) and R-2R DAC, an LSB is referenced to a 14-b resolution at full scale.

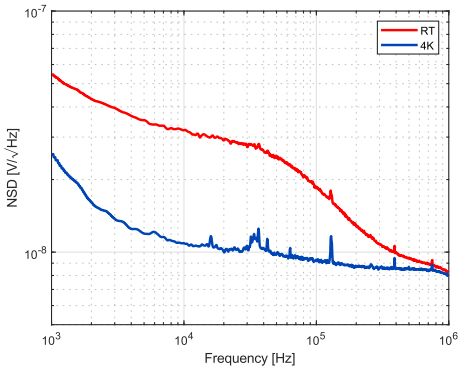


Fig. 8. Measured NSD at RT and 4 K at mid-code. The spurs at 35 kHz and 130 kHz are measurement artifacts due to coupling inside the cryostat.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

| | **This Work** | | *TIM '25* [9] | *ESSERC '24* [10] | *ESSERC '24* [8] | *ESSERC '24* [7] | *Phys. Rev. App '19* [3] |
|---|---|---|---|---|---|---|---|
| **Architecture** | **R-βR** | **R-2R** | R-2R | ΔΣ | R-2R + IDAC | R-2R + Amp | R-2R + Amp |
| **Tech (nm)** | **160** | | 130 | 130 | 180 | 130 | 180 |
| **Temperature (K)** | **4** | | 4.6 | 13 | 4 | 4.3 | 77 |
| **Resolution (bits)** | **14** | **16** | 12 | 16 | 11.06 | 12 | 12 |
| **INL (LSB)** | **±0.3** | **±40** | -2.6/+1.7 | ±40 | 0.5 | - | - |
| **DNL (LSB)** | **±0.5** | **±40** | -0.5/+4.0 | - | 1.6 | - | - |
| **SFDR (dB)** | **84** | - | 61.9 | - | - | 50[e] | - |
| **NSD (nV/$\sqrt{\text{Hz}}$)** | **9.2**[d] | | 29[d] | 140 | 1.617 | 600 | 4500[b,c] |
| **Active Area (mm$^2$)** | **3.8** | | 0.84 | 0.1 | 9.553 | 1.1 | 0.04 |
| **Output range (V)** | **±5** | | 1.8 | ±0.8 | -10 to 16 | 17 | 16 |
| **Power (mW)** | **2.85** | | 1.5 | 1.5 | 68.60 | 8.8[a] | 31.3[a] |
| **$f_s$ (MS/s)** | **3** | | 1 | 6.4 | 0.0012 | 1 | 0.25 |

[a] Per channel, [b] EIS switch closed, [c] estimated at 100 kHz [1], [d] measured at 100 kHz, [e] $f_{out}$ = 6 kHz, [f] from 100 Hz to 500 kHz

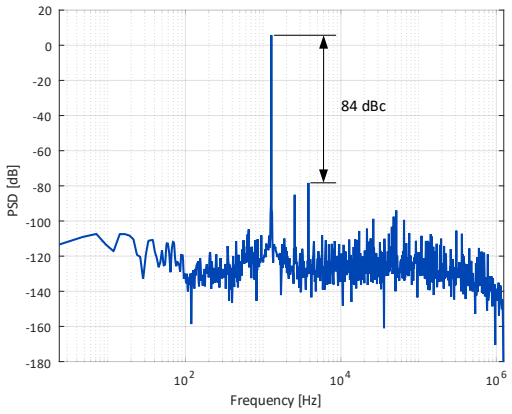


Fig. 9. Output spectrum of the calibrated R-βR DAC, reaching 84 dBc SFDR with a FS 1.275 kHz sinewave input.

Though [8] achieves a very low NSD, it has an extremely low output rate and achieves lower resolution. The DAC in [9] shows a reasonable NSD, but its low output range demands an output amplifier, which, in turn, contributes to noise and power. Also, their INL and SFDR limit the linearity.

## IV. CONCLUSIONS

This paper presents a DAC for DC electrode control of ion-shuttling operations in TIQCs at 4 K. By using a simple R-βR DAC architecture in combination with a linearized resistor, high-voltage active analog circuits are avoided, thus achieving low noise and 14-b resolution with low power dissipation. Thanks to its 3 MS/s update rate and ±5 V output swing, this design enables fast shuttling while maintaining good ion control. Compared to prior high-rate cryogenic DACs, this cryogenic design achieves the lowest NSD and highest SFDR published to date. These results enable high-fidelity qubit operations and pave the way for future large-scale practical TIQCs.

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