258-GS/s Analog Demultiplexer with *pnp* SiGe HBTs on the Data Path

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***Abstract*— A new 1-to-2 analog demultiplexer (ADEMUX) topology is explored to assess the benefits of a complementary SiGe BiCMOS process for fiber-optic receivers operating at symbol rates above 200 GBaud. Although slower than *npn* HBTs, *pnp* SiGe HBTs are used for higher-linearity feedforward cancellation and as 50-Ω output drivers to reduce the supply voltage while minimizing leakage current on the hold capacitors and maintaining the highest reported bandwidth above 110 GHz. The ADEMUX utilizes *npn* switched-emitter followers that operate on complementary phases of the external clock signal, amplified by a clock amplifier with a record 129-GHz bandwidth. SNDR > 30 dB was measured at the maximum linear input voltage swing of 600 mV_{ppd} for sinusoidal inputs up to 111 GHz, with the corresponding ENOB remaining above 5, 4, and 3 bits at 225, 240, and 258 GS/s, respectively. To demonstrate its functionality in a fiber-optic receiver, a 150-GBaud (300-Gb/s) PRBS-13 PAM-4 input stream, the highest reported to date and limited by the test setup and the available commercial 256-GS/s AWG, was demultiplexed into two 75-GBaud PAM-4 streams with expanded eye openings. NRZ bit streams up to a record 198 Gb/s were also demultiplexed. The chip consumes 0.8 W from 3.3 V.**

***Keywords*— analog demultiplexer, ENOB, heterojunction bipolar transistor, *pnp*, switched-emitter follower, SiGe BiCMOS, SNDR, track-and-hold**

I. Introduction

Beyond the current generation of 1.6/3.2-Tbps fiber-optic systems [1], research has already started into 6.4-Tbps transceivers whose electronic circuits need to operate at 300-to-400 GBaud symbol rates. While MOSFET speed continues to marginally improve relative to 3nm FinFET technology with the recent introduction of 2-nm nanosheet CMOS [2], it remains slower than that of state-of-the-art SiGe or InP HBTs. Therefore, for the coming generation of 400-GBaud fiber-optic receivers, the first layer of time- or frequency-domain demultiplexing will likely be implemented in an HBT process, just like the transimpedance amplifier (TIA) and optical modulator driver. One solution is to employ a linear 1-to-2 analog demultiplexer (ADEMUX) after the TIA to deserialize a full-rate PAM-n data stream into two half-rate streams that can then be processed by the 2-nm CMOS ADCs. To this end, a number of *npn*-only InP and SiGe HBT ADEMUX circuits have been reported in recent years [3]–[5], as well as a 22-nm FDSOI CMOS circuit using *p*-MOSFETs on the data path [6]. This paper investigates whether *pnp* HBTs can be beneficial when placed on the high-speed data path of the 1-to-2 ADEMUX topology without compromising bandwidth or sampling rate compared to *npn*-only topologies. A measured data-path bandwidth above 110 GHz and aggregate sampling rates up to 258 GS/s are achieved.

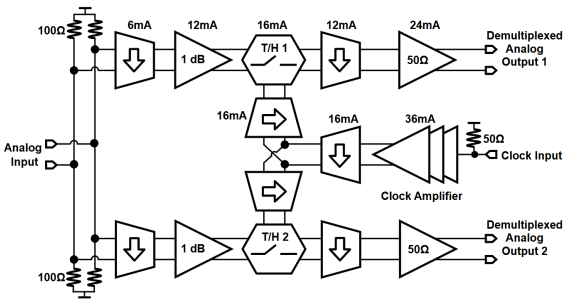


Fig. 1. Block diagram of the 1-to-2 ADEMUX.

II. Circuit Design

Fig. 1 shows the block diagram of the 1-to-2 ADEMUX. It consists of two track-and-hold (T/H) amplifiers that operate on opposite phases of the same clock signal, followed by 50-Ω unity-gain buffers to facilitate RF testing. The track and hold signals are provided by an ultra-broadband amplifier with high common-mode rejection ratio (CMRR), which converts the single-ended external clock signal to differential format.

A. Linear Data Path

The ADEMUX stages in Fig. 2 were designed for linear operation at input signal amplitudes up to 600 mV_{ppd}. To reduce the input capacitance and maximize the input matching bandwidth, the two T/H lanes are driven in parallel from the input pads via short 80-Ω μ-strip lines terminated on 100-Ω resistors and shunt peaking inductors. Small emitter follower (EF) buffers biased at 3 mA (at 0.75×peak-f_T current density) further minimize the input capacitance and drive a resistively-degenerated linear cascode buffer stage with shunt capacitive peaking across the degeneration resistors to

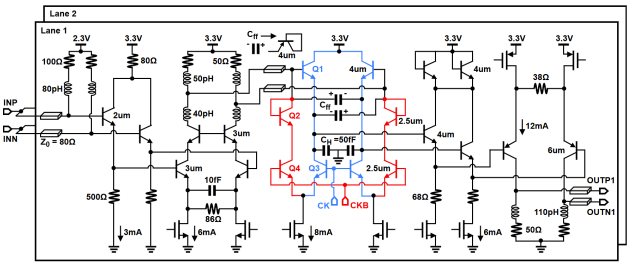


Fig. 2. Schematic of track-and-hold lane with input and output buffers.

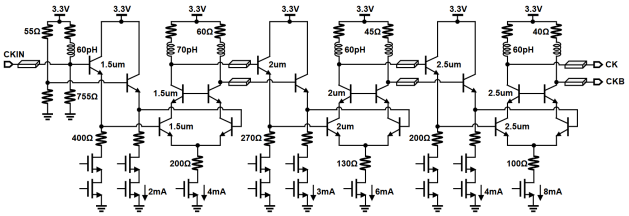


Fig. 3. Schematic of the limiting-mode clock amplifier with single-ended input and differential output.

compensate for input connection losses at frequencies above 70 GHz. The switched-emitter follower (SEF) is biased with an 8-mA tail current source to switch from 0 to the peak-f_T current density. It employs npn-HBT CML switches for maximum switching speed and 50-fF hold capacitors for good SNR while still meeting the bandwidth requirements.

It was found through simulation that, unlike in the traditional approach based on feedforward capacitors, C_{ff}, formed with a series-parallel configuration of four diode-connected npn transistors [7], the signal feedthrough can best be canceled with a reverse-biased diode-connected pnp with the same size as Q_1. This shrinks the layout footprint by a factor of four and reduces hold-mode distortion due to the complementary nature of the npn and pnp HBTs. A 4-µm emitter length EF with a 6-mA current source is placed between the hold capacitor and the output buffer to minimize pedestal droop.

The output buffer consists of a pnp differential pair with resistive emitter degeneration and 50-Ω load resistors with a common-mode voltage of 300 mV. Compared to npn-only HBT topologies [7], it reduces the power supply voltage by avoiding a triple stack of npn HBTs on the signal path and allows DC coupling to measurement instruments or downstream CMOS ADCs without the need for an ultra-broadband DC-blocking capacitor [8]. Each T/H lane consumes 231 mW.

B. Limiting Clock Amplifier

The limiting clock amplifier in Fig. 3 features three cascaded ECL stages with cascode inverters and 320-mV_{pp} logic swing per side. To minimize the input capacitance, which would otherwise limit the bandwidth of the entire amplifier, the emitter length of the HBTs in the first stage is set to 1.5 µm. The role of the cascode inverters is to maximize the bandwidth, facilitate level shifting, and prevent collector-emitter (CE) breakdown, which would occur in a standard ECL topology with CE inverter implementation. Resistors are placed in series with the n-MOSFET tail currents to improve stability and the CMRR at mm-wave frequencies. This is confirmed by the simulated CMRR after layout parasitics extraction which remains higher than 40 dB up to 110 GHz. The clock amplifier drives double EFs that are placed adjacent to the T/H circuits. As depicted in Fig. 1, the clock signal is split at the penultimate EF stage of the clock amplifier to minimize skew mismatch between the two T/H circuits. In total, the clock signal distribution circuits consume 277 mW.

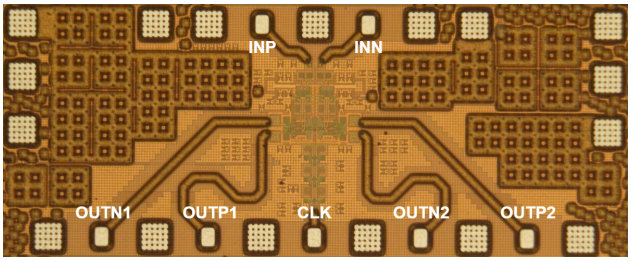


Fig. 4. Die micrograph. The circuit has an area of 470µm × 1170µm.

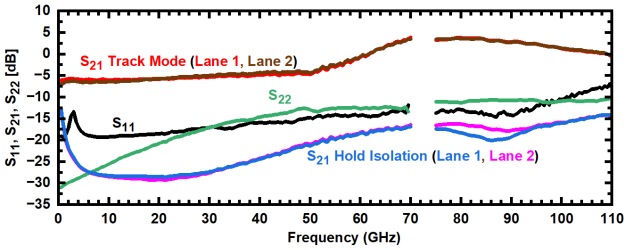


Fig. 5. Measured single-ended S-parameters in track and hold modes from the input to the output of each of the two lanes.

III. Measurements

The IC, whose die photograph is depicted in Fig. 4, was fabricated in a complementary 130-nm BiCMOS technology featuring high-speed npn and pnp SiGe HBTs [9]. Including bias circuits, it consumes 0.8 W from a single 3.3-V supply.

A. S-Parameter Measurements

The single-ended S-parameters, shown in Fig. 5, were measured on die across two VNA bands from DC to 67 GHz and from 75 GHz to 110 GHz, respectively, without de-embedding the pads and interconnect. The track- and hold-mode (isolation) small-signal responses from the input to both OUTP1 and OUTP2 outputs are included, demonstrating excellent lane-to-lane match. The data-path bandwidth exceeds 110 GHz, while S_{11} and S_{22} remain below -10 dB up to 100 GHz. According to simulation, the circuit isolation is further improved to 30 dB in differential mode when the feedforward cancellation takes effect.

B. Large Signal Measurements

Fig. 6 is a photo of the large-signal measurement setup. The clock signal was generated from a low-phase-noise

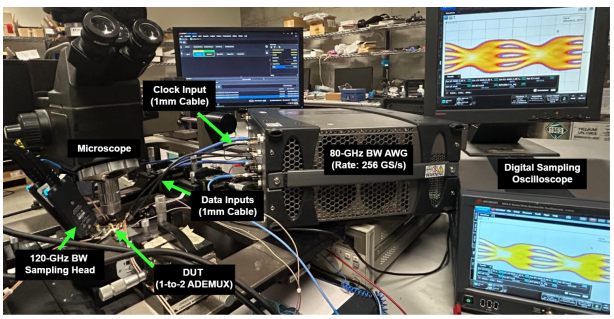


Fig. 6. Setup for on-die large-signal time- and frequency-domain testing.

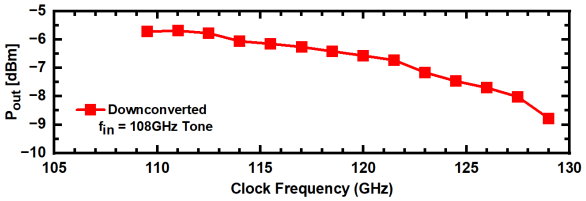


Fig. 7. Measured large-signal clock-path bandwidth.

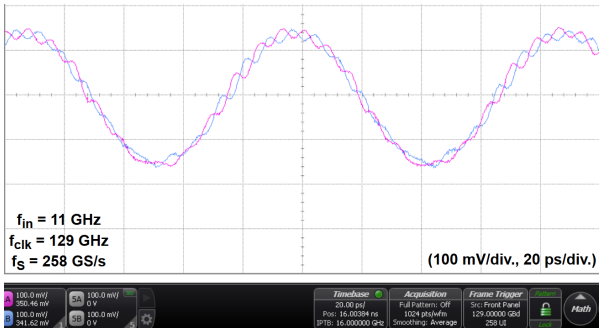


Fig. 8. Measured single-ended waveforms at the two demultiplexed outputs when sampling an 11-GHz input tone at an aggregate rate of 258 GS/s.

synthesizer followed by a 3× multiplier, while an arbitrary waveform generator (AWG) and a pair of 6× frequency multipliers were used to generate W-band differential tones up to 113 GHz, which were applied at the ADEMUX input. To cancel any mismatch between the p and n-sides of the differential input, the amplitude and phase of the multiplied tones were adjusted independently.

The large signal 3-dB clock-path bandwidth of 129 GHz was obtained by sweeping the clock signal frequency with a fixed 108-GHz sinusoidal signal applied to the ADEMUX input and measuring the power of the downconverted fundamental tone at the output of one of the two lanes, as illustrated in Fig. 7. Fig. 8 shows the measured single-ended waveforms at the outputs of the two lanes captured on a 120-GHz bandwidth sampling oscilloscope when an 11-GHz sinusoidal input signal is applied to the ADEMUX and sampled with an external 129-GHz clock signal. The corresponding differential spectra are displayed in Fig. 9. Additionally, to demonstrate the linearity at the upper edge of the input bandwidth, Fig. 10 reproduces the output spectra for a 105-GHz input and a sampling clock of 112.5 GHz. The measured SNDR and the corresponding ENOB are plotted in Fig. 11 as a function of input signal frequency up to 111 GHz for three different sampling rates of 225, 240, and 258 GS/s. To calculate the SNDR, the noise was integrated up to the Nyquist frequency and the setup losses were de-embedded from the measured output spectrum. The circuit achieves an SNDR > 30 dB for 600-mV_{ppd} inputs up to 111 GHz, with the ENOB > 5, 4, and 3, respectively, at 225 GS/s, 240 GS/s, and 258 GS/s, respectively.

As shown in Fig. 6, a commercial 256-GS/s AWG was used to generate the PAM-4 PRBS-13 inputs at symbol rates up to 160 GBaud, limited by the AWG and setup losses. Figs. 12 and 13 demonstrate the increased eye openings

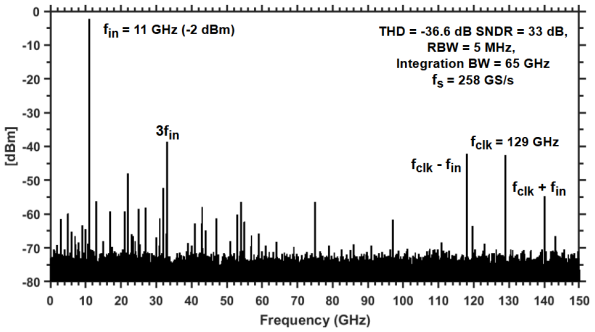


Fig. 9. Measured differential spectra at OUT1 for an 11-GHz input sampled by a 129-GHz clock signal.

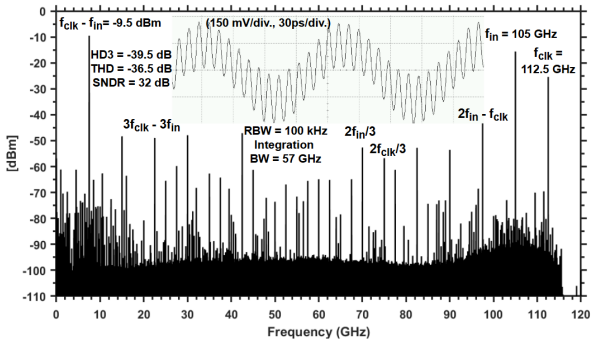


Fig. 10. Measured differential waveform and spectra at OUT1 for a 105-GHz input sampled by a 112.5-GHz clock signal.

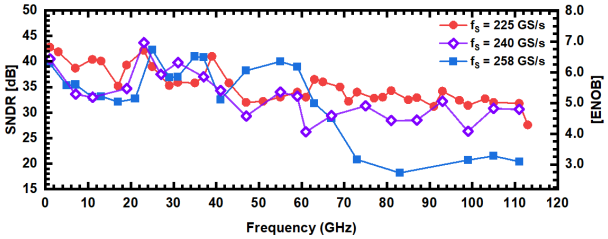
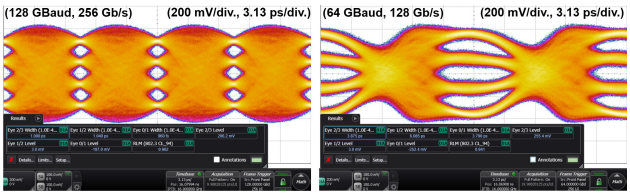


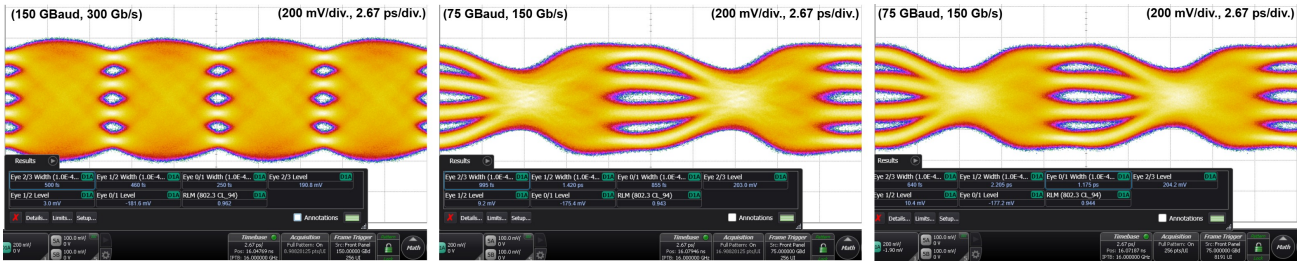
Fig. 11. Measured ADEMUX SNDR and ENOB over input signal frequency with a fixed input amplitude of 600 mV_{ppd} at 225, 240, and 258 GS/s.



(a) (b)

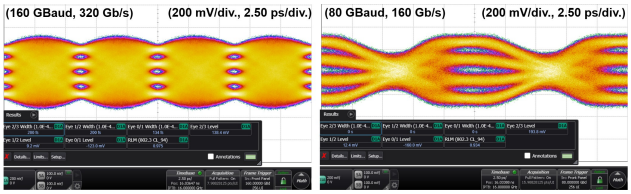
Fig. 12. Measured eye diagrams for a) PAM-4 128-GBaud input passed through the circuit without sampling and b) the demultiplexed PAM-4 64-GBaud eye diagram at OUT1.

of the demultiplexed half-rate output streams compared to those of the full-rate 128-GBaud and 150-GBaud PAM-4 input streams, respectively. The error rate is better than 10^{-4} up to 150 GBaud. At 160 GBaud, as shown in Fig. 14, the input and output eye diagrams have higher error rates, suggesting that the bandwidth and ENOB of the AWG are insufficient. However, they remain adequate to



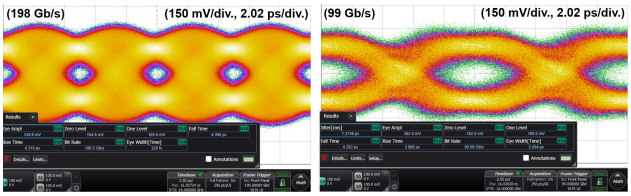
(a) (b) (c)

Fig. 13. Measured eye diagrams for a) PAM-4 150-GBaud input passed through the circuit without sampling and the corresponding demultiplexed 75-GBaud half-rate streams at b) OUT1 and c) OUT2.



(a) (b)

Fig. 14. Measured eye diagrams for a) PAM-4 160-GBaud input passed through the circuit without sampling and b) the demultiplexed PAM-4 80-GBaud eye diagram at OUT1.



(a) (b)

Fig. 15. Measured eye diagrams for a) 198-Gb/s PRBS-13 input and b) the corresponding half-rate retimed 99-Gb/s eye diagram at OUT1.

generate 198-Gb/s NRZ PRBS-13 inputs, which were correctly demultiplexed into 99-Gb/s output streams, as illustrated in Fig. 15. No de-embedding of setup losses or post-processing was applied in these eye-diagram measurements. Table 1 compares this work with other recently published ADEMUX circuits. This circuit achieves the highest data-path bandwidth and sampling rate and operation with the highest PAM-4 and NRZ symbol and bit rates.

IV. Conclusion

A new 1-to-2 ADEMUX topology was demonstrated in a complementary 130-nm SiGe BiCMOS process. It uses *pnp* HBTs on the high-speed path to enhance linearity and reduce voltage headroom without compromising bandwidth or sampling rate compared to *npn*-only implementations. The over 110-GHz data-path and 129-GHz clock-path 3-dB bandwidths are the highest reported to date. At 600-mV_{ppd} sinusoidal inputs, the measured SNDR exceeds 30 dB up to 111 GHz, with the ENOB above 5, 4, and 3 bits at 225, 240, and 258 GS/s, respectively. Operation at 150-GBaud (300 Gb/s) PAM-4 symbol rates, limited by the performance of the 256-GS/s AWG and by the test setup, was also demonstrated for the first time for an ADEMUX.

Table 1. State-of-the-art ADEMUX circuits.

	[3]	[4]	[6]	[5]	**This**
Techn.	250-nm InP HBT	130-nm SiGe BiCMOS	22-nm FDSOI	130-nm SiGe BiCMOS	130-nm SiGe CBiCMOS
Function	1:2	1:2	1:2	1:4	1:2
BW (GHz)	110	>71.8	60	>67	>110
f_S (GS/s)	128	100-128	60-204	200-256	128-258
SNDR (dB) @ ~50GHz	N/A	28.3, $0.5V_{ppd}$	32, $0.32V_{ppd}$	33.2, $0.5V_{ppd}$	29, $0.6V_{ppd}$
PAM-4 (Gb/s)	N/A	N/A	256	256	>300
P_{DC} (W)	1.1	0.6	0.157	1.1	0.8

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