A 48µW 15-bit 10kHz BW Rail-to-Rail Input Capacitively-Coupled Gm-C Delta-Sigma Modulator-Based Sensor Interface with Online Gm-Nonlinearity Self-Calibration Technique

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***Abstract*— This paper proposes a sensor interface based on a capacitively-coupled Gm-C delta-sigma modulator (DSM) featuring Gm nonlinearity self-calibration. The design includes a PVT-robust Gm linearity calibration circuit, a self-updating Gm-calibration look-up table, a Gm input prediction circuit, and a Gm nonlinearity correction circuit. The self-calibration technique effectively extends the linear input range of Gm, enabling a rail-to-rail DSM input range while maintaining a signal-to-noise-and-distortion ratio (SNDR) of 90.7 dB, resulting in a figure of merit (FoM) of 173.9 dB—an improvement of 13 dB compared to the design without self-calibration.**

Keywords—Gm-C, nonlinearity, delta-sigma modulator, continuous-time, self-calibration, robustness

I. Introduction

Continuous-time delta-sigma modulators (CT DSMs) based on Gm-C integrators have become a popular choice for sensor interfaces due to their inherent anti-aliasing properties and high power efficiency [1-7]. However, the nonlinear behavior of the transconductance (Gm) stage remains a key bottleneck, limiting the achievable linearity and dynamic range (DR), especially in more advanced technology nodes. The nonlinearity manifests in two main forms: the first is integration errors induced by switching transients during chopping or feedback, which can be suppressed using techniques like deadband [2-4] or duty-cycled Gm [3]. The second is signal-dependent Gm nonlinearity. This effect is exacerbated in weak inversion, where noise efficiency is optimal, and directly limits the achievable linear input range. Fig. 1(a) shows the signal-dependent nonlinearity of the Gm. It demonstrates that the Gm operates more ideally when its input range is reduced. Fig. 1(b) shows the open-loop Gm-C-based DSM, where the SNDR degrades as the Gm input range increases. To mitigate the Gm signal dependence, adaptive biasing [8], double-differential pairs [9], and local feedback [10] have been proposed, but with limited effectiveness. Resistor degeneration and its variations [4-7,11,12] enhance Gm linearity but result in a limited Gm linear range, reduced effective transconductance, and hence less power efficiency. Lastly, a Gm-nonlinearity calibration technique proposed in a split-ADC [13] extracts the Gm nonlinearity by feeding a known signal into a dual-path structure. However, it is not suitable for continuous operations, and its assumption of a linear error to the output path makes it unsuitable for Gm calibration in a DSM.

This work proposes a sensor interface based on capacitively-coupled Gm-C DSM employing a Gm-nonlinearity self-calibration technique, which incorporates three key parts: 1) a PVT-robust Gm-linearity calibration circuit (Gm-LCC) that measures the real-time Gm nonlinearity and generates a self-updated Gm-calibration look-up table (Gm-LUT). 2) a Gm input prediction circuit (Gm-IPC), which is updated before each conversion cycle. 3) a Gm-nonlinearity correction circuit (Gm-NCC), which linearizes Gm based on the Gm-LUT and the Gm-IPC output. Implemented in a 65nm CMOS technology, the Gm-nonlinearity calibration technique effectively extends the Gm linear input range, enabling a rail-to-rail DSM input range and achieving a 90.7dB SNDR—13dB improvement over the design without self-calibration—over a 10kHz bandwidth, while consuming 48µW and yielding a Schreier FoM of 173.9dB.

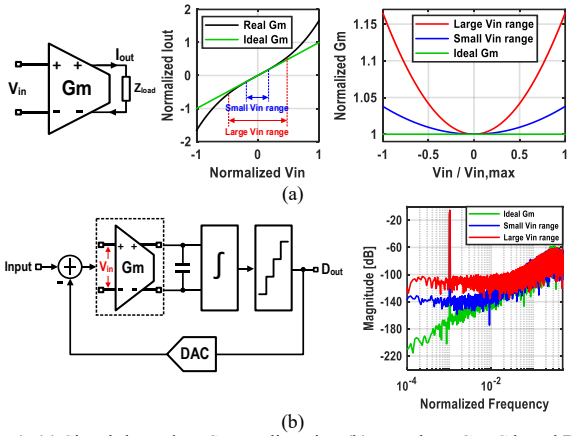


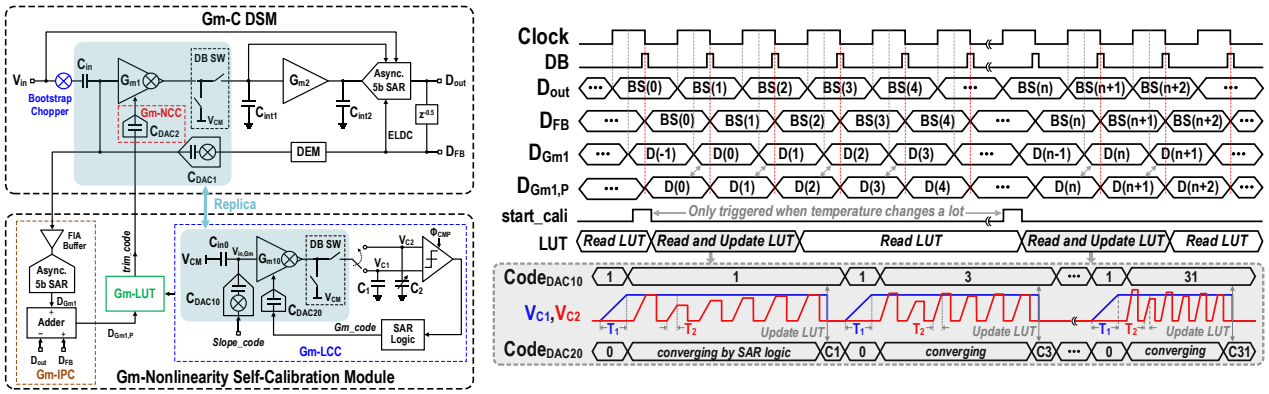
Fig. 1. (a) Signal-dependent Gm nonlinearity; (b) open-loop Gm-C based DSM and the output spectrum vs. Gm input range.

II. Proposed DSM with Self-Calibration

Fig. 2(a) shows the proposed system, which consists of a capacitively-coupled chopper 2nd-order Gm-C DSM with a CIFF topology, and a Gm-nonlinearity self-calibration module that consists of the Gm-LCC, the Gm-LUT, the Gm-IPC, and the Gm-NCC. The DSM employs a 5-bit quantizer to keep the input G_{m1}'s input within a calibrated range (±62.5mV). The quantizer is implemented using an asynchronous SAR ADC, which also serves as the adder for the feedforward and excess-loop-delay compensation (ELDC) paths [14].

A. Gm Design

The Gm-C integrator is implemented by a gain-boost current-reuse pseudo-differential OTA, as shown in Fig. 3 [2]. The chopped input and feedback signals are AC-coupled to $M_{1\text{-}4}$ through input capacitor C_{in} and a feedback capacitor DAC C_{DAC1} (C_{in}=C_{DAC1}=3pF). To offer a rail-to-rail input range, the input chopper employs a bootstrap low leakage switch [15]. To set the DC bias current of $M_{1\text{-}4}$, duty-cycled resistors (R=1MΩ with 1% duty-cycle) operated at f_s are used to couple the gate bias voltage VBP and VBN. Dead-band (DB) switches are placed at the output of the G_{m1}, which block the nonlinear charges during chopping and DAC settling. The Gm/Id of G_{m1} is designed as 30S/A to achieve a good noise efficiency.



(a) (b)

Fig. 2. (a) System architecture of Gm-C DSM with Gm nonlinearity self-calibration; (b) system timing diagram.

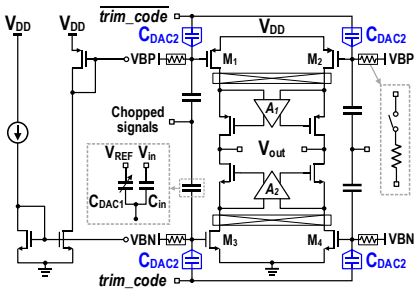


Fig. 3. Schematic of the main transconductor G_{m1}.

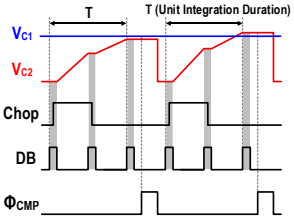
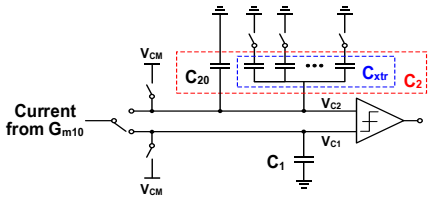


Fig. 4. Gm-LCC timing diagram.

B. Gm Nonlinearity Extraction

To realize real-time Gm linearity calibration, the nonlinearity of G_{m1} is extracted by Gm-LCC, as shown in Fig. 2(a) bottom-right. This is done by sweeping the input of a replica Gm (G_{m10}) under the same biasing condition with a series of quantized input signals via a slope signal generator C_{DAC10}. To maximally mimic the input of G_{m1}, C_{in0}, C_{DAC10} and C_{DAC20} are matched to C_{in}, C_{DAC1} and C_{DAC2} in the main DSM, respectively. C_{in0} and part of C_{DAC10} (27-LSBs) are always connected to V_{CM}, while the remaining C_{DAC10} (4-LSBs) toggles between V_{REFP} and V_{REFN} to produce a differential input covering ±62.5mV of the G_{m1} input range. Since G_{m1}'s input signal is not always at quantized signal levels, the remaining C_{DAC10} is split into 5bits (1LSB=2mV) to limit the calibration quantization error for a >10dB SNDR improvement.

As shown in Fig. 2, the Gm nonlinearity extraction works as follows: 1) C_{DAC10} applies a 2mV differential input to G_{m10}, which is within its linear range. The output current of G_{m10} is then integrated onto C_1 during T_1, resulting in a voltage V_{C1}, which will later serve as a reference. 2) The input of G_{m10}, $V_{in,Gm}$ is then swept across the input range (±62.5mV) using C_{DAC10} and its output current is integrated on C_2 for T_2 (=T_1) to obtain V_{C2}.



Time-Capacitance Co-scaling Table

Vin (mV)	2	6	10	14	18	22	26	30	34	38	42	46	50	54	58	62
C_{DAC10} code	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
T_2 (# of T)	17	6	4	3	2	2	2	2	1	1	1	1	1	1	1	1
C_2 (pF)	17	18	20	21	18	22	26	30	17	19	21	23	25	27	29	31
C_{xtr} (pF)	0	1	3	4	1	5	9	13	0	2	4	6	8	10	12	14

C_{20}=C_1=17pF T_1=17T

Fig. 5. Proposed time-capacitance co-scaling technique.

By scaling C_2 in proportion with $V_{in,Gm}$, a V_{C2} is obtained for each input, which should ideally be the same as V_{C1} but will deviate due to Gm-nonlinearity. 3) For each $V_{in,Gm}$, the SAR logic adjusts C_{DAC20} to modulate the G_{m10} value such that V_{C2}=V_{C1}. By doing so across all $V_{in,Gm}$, a "linearized" G_{m10} is obtained, and the corresponding C_{DAC20} and C_{DAC10} codes are stored in the Gm-LUT for real-time calibration. The offset of G_{m10} will result in a calibration error since it alters V_{C1} and V_{C2} in a nonlinear fashion. Chopping is applied in each unit integration duration (T=1μs) to cancel the offset effect (Fig. 4).

To ensure G_{m10} operates in the appropriate output swing region, the peak value of V_{C1} and V_{C2} is set as ~100mV. Due to leakage and parasitic effects, C_1 should be larger than 10pF to maintain accuracy. Since C_2 needs to be a scaled-up version of C_1, this would require C_2 to be larger than 310pF, incurring a large area overhead. To address this, a time-capacitance co-scaling technique is proposed, as shown in Fig. 5. During each calibration cycle, both T_2 and C_2 are jointly adjusted such that the integration result (I_{Gm10}·T_2/C_2) remains constant. With C_1 and T_1 fixed as 17pF and 17T and C_2 ranging from 17pF to 31pF, the maximum C_2 is reduced by 10×, minimizing chip area.

C. Gm Input Prediction Circuit

With Gm-LUT being available, a Gm-IPC is proposed to predict the rough input signal of G_{m1} and hence determine the corresponding Gm-LUT code for linearity calibration before each conversion cycle. As shown in Fig. 2(a), it consists of a dedicated 5-bit SAR ADC, an ADC input buffer, and a digital adder. The SAR ADC, replicating the DSM quantizer, is used to

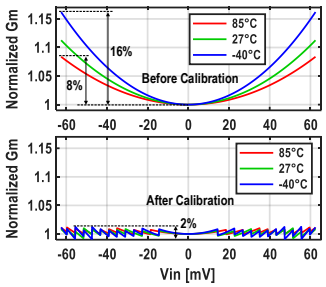


Fig. 6. Simulated Gm-nonlinearity before and after calibration across temperature.

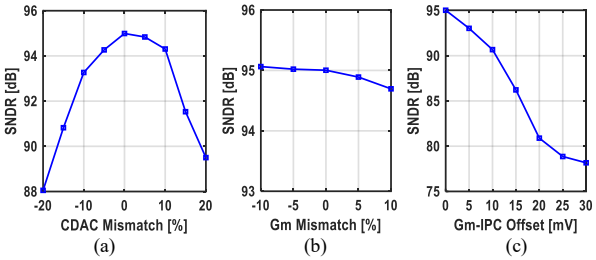


Fig. 7. Simulated (a) SNDR vs. CDAC mismatch; (b) SNDR vs. Gm mismatch; (c) SNDR vs. Gm-IPC offset.

directly digitize the current G_{m1} input into D_{Gm1}. To avoid kickback and excessive loading, a unity-gain buffer based on a floating inverter amplifier (FIA) is used to isolate the SAR input sampling capacitance from the Gm input while minimizing power consumption.

The system timing diagram is shown in Fig. 2(b). Thanks to the half-cycle delay of the feedback in DSM, the next G_{m1} input can be predicted as

$$D_{Gm1,P}(N+1) = D_{Gm1}(N) - D_{out}(N+1) + D_{FB}(N) \approx D_{Gm1}(N+1)$$

where D_{out} and D_{FB} are the DSM output and feedback codes, respectively. Simulation shows that the Gm-IPC results in a final prediction error as small as ~2mV and consumes 6µW, which is marginal compared to the entire DSM. Finally, according to the Gm-IPC output, a correction code from Gm-LUT is fed to Gm-NCC: a common-mode (CM) DAC C_{DAC2} (replica of C_{DAC20}), to change the CM biasing of G_{m1} and thus linearize it.

D. PVT Robustness and Mismatch Effect

In a typical case, simulation shows that the proposed Gm-nonlinearity self-calibration technique can improve the uncalibrated DSM SNDR (~78dB) by ~17dB, mainly limited by the Gm-IPC accuracy and the finite resolution of $C_{DAC10,20}$. However, Gm-nonlinearity varies with temperature, as shown in Fig. 6. A coarse low-power diode-based temperature sensor is implemented on chip to refresh the Gm-LUT when a certain amount of temperature drift is present, which could degrade SNDR. This sensor consumes 2µA.

A complete update of Gm-LUT takes ~700µs, which is fast enough to adapt to the speed of temperature drift in most applications. The Gm-LCC is only activated when the temperature drifts a certain amount; otherwise, it stays powered off, resulting in negligible power consumption in most use cases, e.g., assuming a maximum temperature drift of 10°C can occur in 5s, and the Gm-LCC is activated per 5°C drift, the averaged power consumption of the Gm-LCC circuit will be only 4nW. Supply variation has a negligible impact, since the Gm bias voltages VBN and VBP in Fig. 3 will track the supply variation, thereby maintaining the same transconductance and trim code.

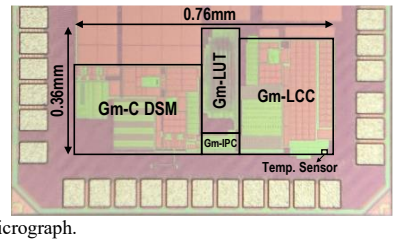


Fig. 8. Die micrograph.

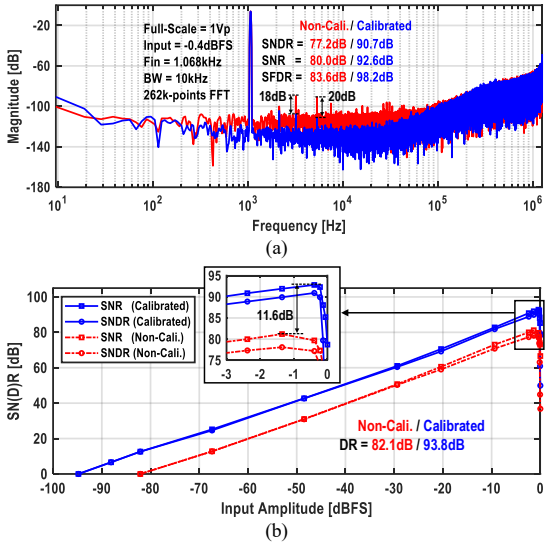
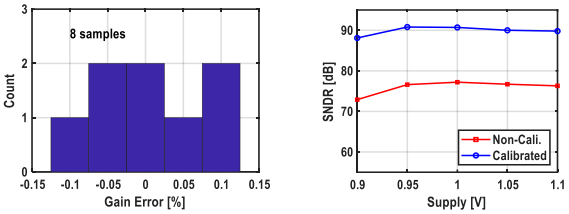


Fig. 9. (a) Measured spectrum, and (b) measured DR.

In reality, replica Gm and CDACs will exhibit mismatches and therefore could affect the calibration effectiveness. However, both have very limited effects on the SNDR as shown by Monte Carlo simulations in Fig. 7. Gm mismatch would change the absolute values of V_{C1} and V_{C2} simultaneously, but since G_{m10} still follows similar nonlinear characteristics of G_{m1}, the relative relation between V_{C1} and V_{C2} remains the same; therefore, the Gm-LUT remains largely valid. CDAC mismatch can result in a slight difference in the calibrated biasing condition between G_{m1} and G_{m10}. However, a 20% mismatch would lead to Gm deviating from the target region by only 3%, therefore resulting in a small degradation in SNDR. As a result, the proposed Gm self-calibration method does not rely on careful layout matching beyond common practice. An offset in the Gm-IPC can also result in a calibration error, but as Fig. 7(c) shows, this is not prominent as the offset can be easily kept within a couple of mV by proper device sizing and layout.

III. Measurement Results

A prototype is fabricated in a 65nm CMOS process, with an active area of 0.274mm² (Fig. 8). The Gm-LCC area can be further reduced by implementing G_{m10} as a scaled fraction of the G_{m1} stage, as the mismatch between the two is not very critical. This will automatically scale down the integration capacitors that are currently relatively area-consuming. The modulator operates at a 2.5MHz sampling rate from a 1V supply. Fig. 9(a) shows the measured output spectrum with a –0.4dBFS 1.068kHz input. With Gm-calibration, the SNR is improved by 12.6dB,



(a) (b)

Fig. 10. (a) Measured gain error; (b) measured SNDR vs. supply variation.

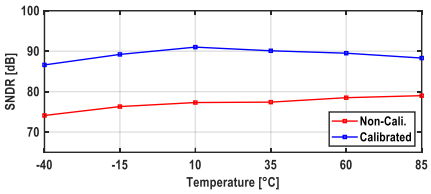


Fig. 11. Measured SNDR over temperature variation.

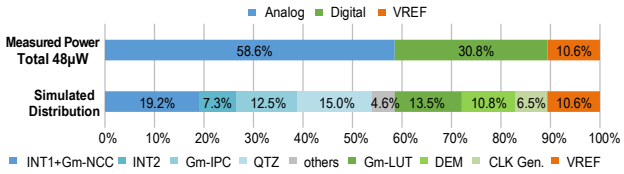


Fig. 12. Measured power consumption and simulated power distribution.

from 80dB to 92.6dB; and the SNDR is improved by 13.5dB, from 77.2dB to 90.7dB over a 10kHz bandwidth, respectively. The SFDR exceeds 98dB across the signal band. Fig. 9(b) shows SNDR and SNR vs. input amplitude, with calibration, the DR is improved to 93.8dB from 82.1dB.

Fig. 10(a) shows that the measured gain error is within ±0.15%. Fig. 10(b) shows the SNDR improvement (>10dB) under ±10% supply variation, where the DSM is calibrated once under the nominal supply, demonstrating supply insensitivity. Fig. 11 demonstrates the SNDR improvement is ~10dB over –40°C to 85°C. The total DSM power consumption is 48µW (Fig. 12), with the detailed distribution based on simulation. The Gm-LCC power is not included because it is only activated when a relatively large temperature drift occurs, and it consumes 15µW when activated.

Table. I summarizes the performance of the proposed DSM and compares it with the state-of-the-art capacitively-coupled Gm-C DSMs. Compared to [1-3,5], this design concurrently addresses both signal-dependent Gm nonlinearity and switching-induced transients. Furthermore, it demonstrates a significantly wider Gm linear input range compared to [1,2,4] (±62.5mV vs. ±15mV), enabling a rail-to-rail DSM input range while maintaining high SNDR and FoM. The online self-calibration improves the SNDR and DR by 13.5dB and 11.7dB compared to the design without it, while also ensuring a stable performance over PVT variation, enhancing robustness compared to [1,3,5].

IV. Conclusion

This paper proposes a sensor interface based on capacitively-coupled Gm-C DSM with a PVT-robust Gm-nonlinearity self-calibration. The self-calibration technique effectively extends the Gm linear input range, which enables a rail-to-rail DSM input range while maintaining a 90.7dB SNDR, resulting in a 173.9dB FoM.

TABLE I Comparison with State-Of-The-Arts

	This work	[1]	[2]	[3]	[4]	[5]
Technology [nm]	65	180	130	180	180	180
Area [mm²]	0.274	0.55	0.29	0.14	0.38	2.28 (full chip)
Supply [V]	1	1	0.9	1.2/1	1.8	1.2
Input range [V]	±1	±180m	±80m	±1.2	±33.2m	±500m
Gm input range [V]	±62.5m	±10m	±10m	-	±15m	-
Fs [Hz]	2.5M	12.8k	1M	1.6M	5.12M	64k
BW [Hz]	10k	100	3.9k	10k	10k	100
Power [W]	48µ	6.5µ	21µ	9.7µ [a]	504µ	6.01µ
Signal-dependent Gm linearization?	Yes, online self-calibration	No	No	No	Yes, tail resistor	Yes, source degeneration
Nonlinear switching transient block?	Yes, Deadband	No	Yes, Deadband	Yes, Deadband & Duty-cycled Gm	Yes, Deadband	No
PVT Robustness	Yes	No	Yes	No	Yes	No
SNDR [dB]	90.7 / 77.2*	91.3	85.0	90.1	-	70.1
DR [dB]	93.8 / 82.1*	92.3	86.2	90.1	87	-
FoM_{SNDR} [dB]	173.9 / 160.4*	163.2	167.7	180.2 [a]	-	142.3
FoM_{DR} [dB]	177.0 / 165.3*	164.2	168.9	180.2 [a]	160.0	-

$FoM_{SNDR} = SNDR + 10\log(\frac{BW}{Power})$ $FoM_{DR} = DR + 10\log(\frac{BW}{Power})$

* Before calibration [a] Not include reference power

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