A 1.64-NEF Discrete-Time Closed-Loop Series-Parallel Amplifier for Biopotential Recording with 139-V_{PP} Common-Mode Interference Tolerance

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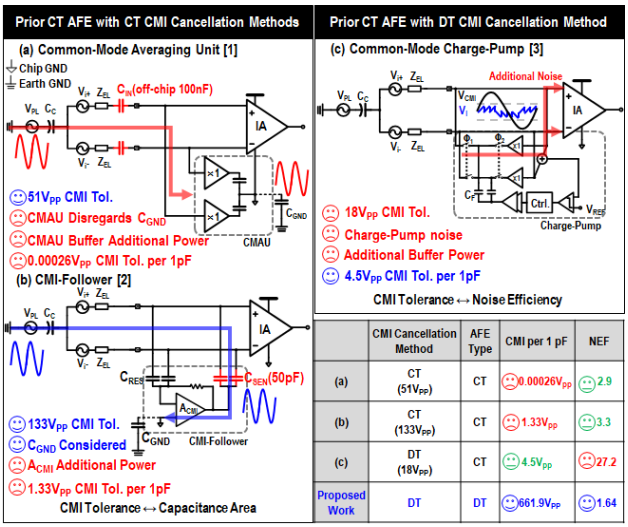
***Abstract*—This paper presents an analog front-end (AFE) for biopotential recording that achieves a noise efficiency factor (NEF) of 1.64 and common-mode interference (CMI) tolerance of 139V_{PP}. The proposed AFE employs a discrete-time (DT) closed-loop series-parallel amplifier (CL-SPA) to deliver a voltage gain of 46dB while maintaining low noise and high CMI tolerance. To achieve robust CMI tolerance, a switched-capacitor-based discrete-time CMI tracking scheme is introduced. By decoupling the sampling phase from the CMI tracking phase in the time domain, the noise generated during the CMI tracking process is separated from the desired signal. Fabricated in a 180-nm CMOS process, the proposed integrated circuit (IC) consumes 2.55µW per channel from a 1.2V supply at a sampling frequency of 500kHz, achieving an input-referred noise (IRN) of 0.289µV_{rms}.**

Keywords— Analog front-end (AFE), biopotential amplifier, common-mode interference (CMI), discrete-time (DT) amplifier, noise efficiency factor (NEF), two-electrode recording

I. Introduction

Continuous and long-term monitoring of physiological signals, such as electrocardiogram (ECG) and electroencephalogram (EEG), is becoming increasingly important for wearable and mobile healthcare applications. To improve user convenience and ease of daily use, two-electrode recording systems are preferred over traditional three-electrode systems. However, two-electrode recording systems electrically isolate the human body, making it more vulnerable to power-line coupling. As a result, the analog front-end (AFE) in two-electrode systems can be exposed to common-mode interference (CMI) exceeding 100-V_{PP} [1]–[7], causing the front-end amplifier to saturate if not properly suppressed.

Fig. 1 shows prior continuous-time (CT) and discrete-time (DT) CMI tolerance enhancement techniques along with their trade-offs among area, noise, and CMI tolerance performance. To provide a fair comparison, we introduce area efficiency, defined as the tolerated CMI amplitude normalized by the required capacitance (V_{PP}/pF). Under this metric, the CT CMI tolerance techniques, such as the common-mode averaging unit (CMAU) [1] and the CMI-Follower [2], exhibit poor area efficiency due to the need for forming a low-impedance CM path at the low fixed frequency (50 or 60Hz) of power-line interference, despite tolerating 51V_{PP} and 133V_{PP}, respectively. The CMAU relies on two off-chip 100nF capacitors [1], corresponding to 0.00026V_{PP}/pF, while the CMI-Follower uses two 50pF on-chip sensing capacitors [2],



	CMI Cancellation Method	AFE Type	CMI per 1 pF	NEF
(a)	CT (51V_{PP})	CT	0.00026V_{PP}	2.9
(b)	CT (133V_{PP})	CT	1.33V_{PP}	3.3
(c)	DT (18V_{PP})	CT	4.5V_{PP}	27.2
Proposed Work	DT	DT	661.9V_{PP}	1.64

Fig. 1. Prior architectures for CMI cancellation and their limitations, which the proposed design aims to overcome.

corresponding to 1.33V_{PP}/pF. In contrast, DT techniques, such as the common-mode charge pump (CMCP), exploit frequency-dependent impedance scaling to implement a lower equivalent impedance, achieving a higher area efficiency of 4.5V_{PP}/pF [3]. However, their NEF performance degrades due to the switching noise from the CMCP circuit.

To address these limitations, this paper proposes a DT-based CMI-tolerant AFE architecture. The proposed system employs a phase-decoupled CMI-tolerant input capacitor network, a closed-loop series-parallel amplifier (CL-SPA), and a time-division-multiplexed (TDM) instrumentation amplifier (IA). By separating the sampling and CMI-tracking phases, the proposed architecture suppresses CMI without directly introducing tracking noise into the signal path, while the CL-SPA enables low-noise DT amplification. Consequently, it achieves 0.289µV_{rms} input-referred noise (IRN) and 139V_{PP} CMI tolerance using only two 105fF CMI-tracking capacitors, corresponding to 661.9V_{PP}/pF. The TDM IA further reduces per-channel power consumption to 2.55µW, resulting in an NEF of 1.64.

II. Proposed Low-NEF CMI-Tolerant AFE

A. Overall AFE Architecture

Fig. 2 shows the overall architecture and timing diagram of the proposed two-channel AFE. The two channels share a TDM IA, where their amplification phases operate alternately, thereby saving per-channel power and ensuring a compact

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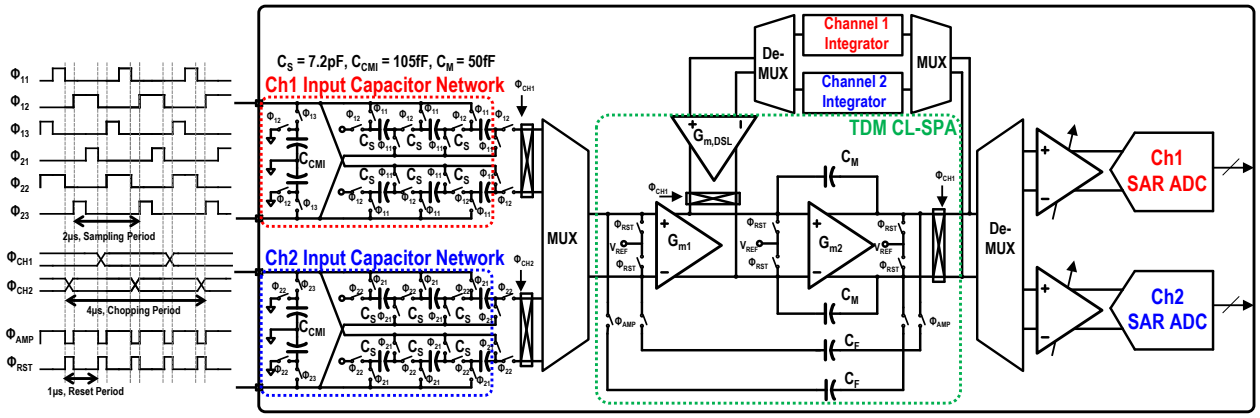


Fig. 2. Proposed AFE architecture.

design. After amplification, the signals are demultiplexed and routed to the programmable gain amplifier (PGA) and analog-to-digital converter (ADC) of each channel. Section II-B describes the input capacitor network and its three-phase operation, Section II-C explains the operating principle of the proposed CL-SPA, and Section II-D presents the IA structure and current-domain DC servo loop (DSL).

B. Input Capacitor Network

The input capacitor network of each channel consists of three 7.2pF sampling capacitors (C_S) and one 105fF CMI-tracking capacitor (C_{CMI}) for each differential input node (P and N), connected in parallel through switches. As shown in Fig. 3, the proposed system operates in three phases: sampling, amplification, and CMI tracking.

During the first phase (Φ_1, sampling phase), the top and bottom plates of C_S are connected to $V_{IN,P}$ and $V_{IN,N}$. This allows C_S to sample only the differential input voltage, thereby achieving passive CM cancellation. Therefore, the sampled charge is $3C_S{\cdot}(V_{IN,P}–V_{IN,N})$ in the P-node network and $3C_S{\cdot}(V_{IN,N}–V_{IN,P})$ in the N-node network.

In the second phase (Φ_2, CL-SPA amplification phase), the parallel-sampled capacitors (C_S) are reconfigured in series. To form this structure, the bottom plate of the leftmost capacitor is tied to V_{REF}, while its top plate is connected to the bottom plate of the adjacent capacitor. The top plate of the rightmost capacitor is then connected to the virtual-ground node of the IA through a chopper, which is used to suppress low-frequency noise, particularly 1/f noise. This series-connected capacitor structure transfers the sampled charge to the output node through the feedback capacitor C_F. At the same time, both terminals of C_{CMI} are reset to chip ground.

In the third phase (Φ_3, CMI-tracking phase), the top plates of the reset C_{CMI} capacitors are connected to $V_{IN,P}$ and $V_{IN,N}$, respectively, while their bottom plates remain connected to the chip ground. As this operation repeats, the input nodes are periodically connected to the chip ground (V_{GND}) through an equivalent switched-capacitor resistance. This creates a low-impedance path that allows the chip ground to follow the CMI.

C. Operating Principle of CL-SPA

Fig. 4 compares the operating principles and structures of the conventional series-parallel amplifier (SPA) and the proposed CL-SPA. The conventional SPA [9] typically employs a 1:2 ping-pong architecture with four SP cells, each composed of eight sampling capacitors. In both structures, the input sampling mechanism is identical: the differential input pair is sampled across the capacitor. This differential sampling

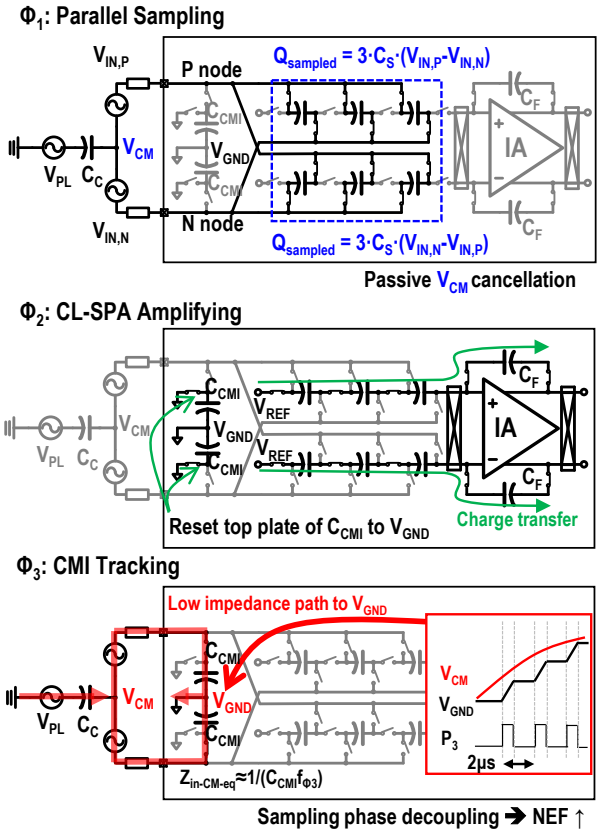


Fig. 3. Operation of the input capacitor network in each phase.

inherently provides passive CM cancellation. In addition, reconfiguring the capacitors in series during the amplification phase generates voltage gain while consuming only switching power, thereby improving the NEF.

However, the amplification phase of the conventional SPA and the proposed CL-SPA operate differently. In the conventional SPA, the output of the series-connected capacitors is directly coupled to the input capacitor of the following IA. The series capacitor array operates as a DT passive transformer, with its voltage gain proportional to the number of capacitors, N. According to [9], achieving high voltage gain while reducing IRN requires increasing both the number and the total capacitance of the sampling capacitors, resulting in significant area overhead. Moreover, without any dedicated CMI tolerance techniques, the conventional SPA remains vulnerable to CMI.

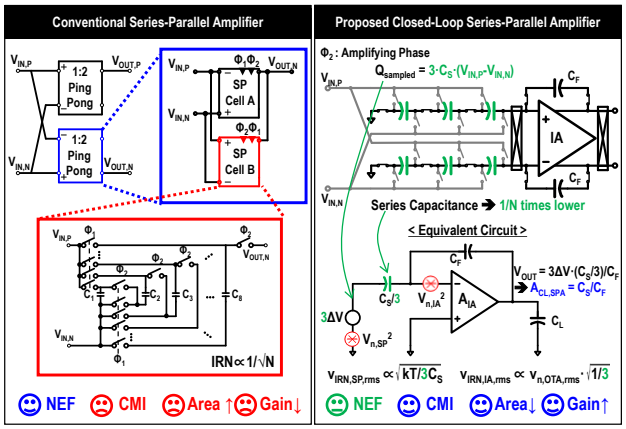


Fig. 4. Comparison between the conventional SPA and the proposed CL-SPA, and equivalent-circuit analysis.

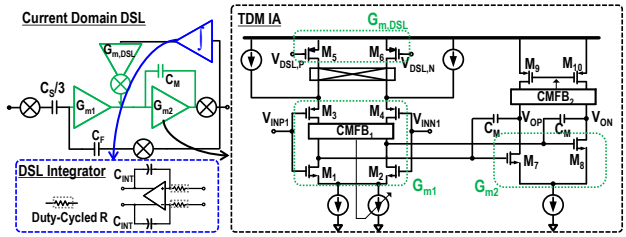


Fig. 5. Block diagram of the proposed IA with a current-domain DSL, and circuit schematic of the main amplifier.

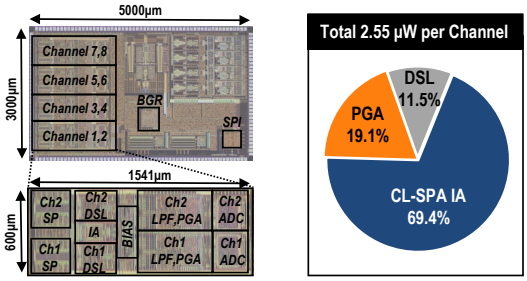
To address these limitations, the proposed CL-SPA adopts a closed-loop amplification method. As shown in Fig. 4 (top-right), during the amplification phase, one terminal of the series-connected capacitor is connected to V_{REF}, and the other terminal is connected to the virtual ground node of the IA. This configuration transfers the sampled charge to V_{OUT} through the feedback capacitor C_F, thereby generating the desired voltage gain. As shown in the single-ended equivalent in Fig. 4 (bottom-right), the voltage across the three sampling capacitors is 3ΔV, and the equivalent series capacitance is $C_S/3$. Therefore, the transferred charge is $C_S\Delta V$, resulting in a closed-loop gain of C_S/C_F. In the fully differential architecture, the system gain is $2C_S/C_F$. In this design, with C_S=7.2pF and C_F=72fF, a gain of 46dB is achieved.

With this configuration, the proposed AFE preserves the key advantage of SPA, *i.e.*, IRN decreases as the number of sampling capacitors increases, while achieving high voltage gain without requiring an excessive number of capacitors. In addition, the phase-decoupling technique implemented by the DT operation provides CMI tolerance. This enables the recording of weak biopotential signals under large CMI.

D. Structure of IA and Current-Domain DC Servo Loop

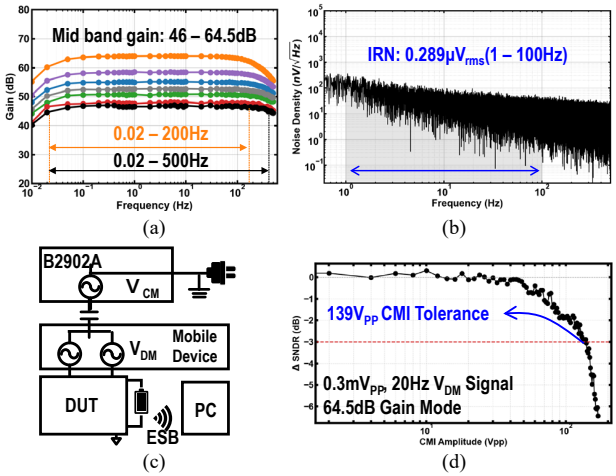
Since the proposed CL-SPA operates as an SC amplifier, the accumulated charge from the EDO and the inherent offset present at the input stage must be removed to prevent saturation in subsequent stages. In conventional designs, a voltage-domain DSL directly subtracts the EDO at the IA input. However, in the proposed configuration, the equivalent series capacitance at the IA is $C_S/3$, which increases the noise introduced by the voltage-domain DSL and degrades the overall noise performance.

To avoid this noise degradation, the proposed architecture employs a current-domain DSL, as shown in Fig. 5. The IA adopts a modified current-reusing G_{m1} stage, in which



(a) (b)

Fig. 6. (a) Chip micrograph, (b) measured total power consumption and power breakdown of the proposed AFE.



(a) (b) (c) (d)

Fig. 7. (a) Measured frequency response, (b) input-referred noise, (c) CMI tolerance measurement setup, (d) CMI tolerance performance.

transistors M_5 and M_6 act as transconductance cells for the DSL. By injecting the feedback current directly into the amplifier, the proposed method avoids the noise amplification associated with the voltage-domain method. Furthermore, the DSL integrator utilizes a duty-cycled resistor that produces a much larger resistance value than its physical value [10]. This provides a large time constant required for a low high-pass corner frequency without excessive area overhead. After amplification by the IA, the output signals are demultiplexed according to the timings assigned to each channel. The demultiplexed signals are then processed by the PGA and ADC of the corresponding channel for more amplification and signal digitization.

III. Measurement Results

The proposed IC was fabricated in a 180-nm CMOS process and occupies an active area of 0.462mm² per channel, as shown in Fig. 6. Operating from a 1.2V supply, the AFE consumes 2.55µW per channel. Fig. 7(a) shows the measured frequency response of the AFE. The mid-band gain is programmable from 46 to 64.5dB. At the highest gain setting, the AFE exhibits a bandwidth of 0.02–200Hz. Fig. 7(b) shows the measured IRN spectrum. The integrated IRN over 1–100Hz is 0.289µV_{rms}, resulting in a NEF of 1.64 and a power efficiency factor (PEF) of 3.20. To evaluate robustness against CMI, the signal-to-noise-and-distortion ratio (SNDR) degradation was measured as the CMI amplitude increased, as shown in Fig. 7(d). As shown in the measurement setup of Fig. 7(c), a precision source/measure unit was used to generate the CMI through a 220pF coupling capacitor, while a mobile device provided the DM signal to the device under test. The

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

Parameters	[4] VLSI'23	[5] TBioCAS'25	[6] JSSC'21	[3] JSSC'23	[1] ISSCC'20	[2] JSSC'25	This Work
Technology [nm]	180	180	180	180	180	110	180
Area/Channel [mm^2]	3.8[a]	6.6[a]	0.606[b, c]	0.878[b, c]	0.044[f]	0.468[b]	0.462[b]
Supply Voltage [V]	1.8	1.2	1.2	1.2	0.9 / 1.2	1 / 1.5	1.2
Power/Channel [µW]	6.63[d, e]	44	12.3[d, e]	43.3	7.4	4.6[d]	2.55[d]
Midband Gain [dB]	25.8	20-47	45	54	56/62/68	54.5-67.9	46-64.5
Analog Front-End Type	CT (CBIA)	CT (CBIA)	CT (CBIA)	CT (CCIA)	CT (OPPGA)	CT (CMA-CR-OTA)	DT (CL-SPA)
CMI Cancellation Method	DT CMIC & CAF	DT Pseudo RLD	DT CMCP	DT CMSL	CT CMAU	CT CMI-Follower	DT CMI Tracker
CMI Tolerance [V_{PP}]	22	40	15	18	51	133	139
CMI Tolerance per Unit Capacitance [V_{PP}/pF]	N/A	N/A	4.69[e]	4.5[e]	0.00026[e]	1.33[e]	661.9
CMI Circuit Occupying Area [mm^2]	0.307	N/A	0.378	0.602	Off-chip(200nF)	0.038	0.005
IRN (Bandwidth) [μV_{rms}]	2.23 (1-100Hz)	0.62 (1-150Hz)	1.67 (1-100Hz)	1.9 (1-100Hz)	0.269 (0.5-100Hz)	0.43 (0.5-100Hz)	0.289 (1-100Hz)
NEF (PEF)	16.58(495)[d, e]	9.6(110.56)	20.72(515)[d, e]	27.2 (887.8)	2.9 (N/A)	3.3 (12.54)[d]	1.64 (3.20)[d]

[a] Full chip area [b] AFE core area [c] Estimated from data [d] Excluding ADC and biasing circuit [e] Calculated from given data [f] Instrumentation amplifier only

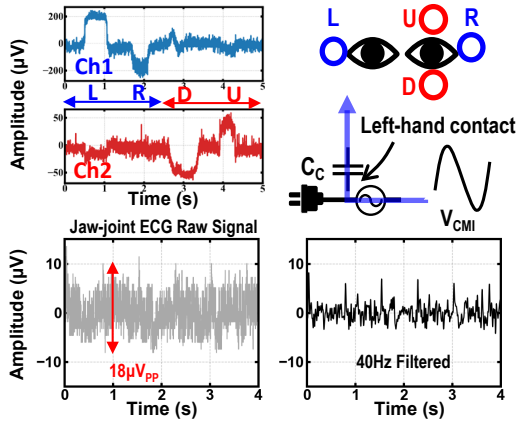


Fig. 8. Electrode placement and measured biosignals.

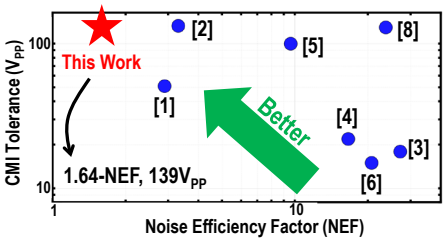


Fig. 9. Comparison with state-of-the-art designs: CMI tolerance versus NEF.

proposed architecture tolerates up to 139V_{PP} CMI, at which the SNDR decreases by 3dB.

Fig. 8 shows the electrode placement and measured biosignals. The proposed AFE successfully records electrooculogram (EOG) signals that remain clearly distinguishable even under large CMI coupling conditions. As indicated in [11], ECG signals measured near the jaw-joint region are tens of times smaller than those of standard limb leads. Despite their small amplitude and practical common-mode coupling, the prototype IC also captures jaw-joint ECG signals without being obscured by noise and interference.

IV. CONCLUSION

In this work, we presented a CMI-tolerant AFE based on the CL-SPA architecture. Table I and Fig. 9 summarize the performance of the proposed AFE and compare it with state-of-the-art CMI-tolerant recording ICs. The prototype achieves a CMI tolerance of 139V_{PP} while maintaining an IRN of 0.289μV_{rms}. With an NEF of 1.64 and a PEF of 3.20, the proposed architecture enables low-noise, low-power recording of weak biopotential signals even in the presence of large CMI.

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