A 0.075-pJ/b/dB Isolation-Enhanced 56/2-Gb/s Asymmetric SBD Transceiver for 30.2-dB Loss Automotive Links

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Abstract*—This paper presents a 56-Gb/s PAM-4 / 2-Gb/s NRZ asymmetric simultaneous bidirectional (SBD) transceiver for 30.2-dB loss automotive links, which introduces a hybrid with an isolation-enhancing scheme combining both amplitude- and frequency-domain techniques that tackle severe channel attenuation and self-interference, eliminating the need for a power-hungry echo canceller. The architecture leverages a high-swing (1.29 Vpp) 2xVDD stacked driver for the forward channel and an ultra-low-swing (0.11 Vpp) driver for the back channel. This swing asymmetry enables strong amplitude-domain isolation, while spectral filtering ensures frequency-domain rejection of self-interference. This robust, echo-canceller-free isolation supports error-free (BER < 1e-12) operation over a 30.2-dB loss channel at 14 GHz. The transceiver achieves a state-of-the-art Figure of Merit (FoM) of 0.075 pJ/bit/dB.

Keywords*—simultaneous bidirectional (SBD), asymmetric swing, passive resistive hybrid, spectral filtering.

I. Introduction

The evolution of automotive camera links and next-generation display interfaces demands a substantial increase in bandwidth, as shown in Fig. 1. These links, however, often rely on long cables with multiple connectors, creating high-loss channels (>20 dB) that severely limit bandwidth [1]. To push data rates beyond 25 Gb/s over such legacy infrastructure, advanced modulation such as PAM-4 becomes mandatory. Moreover, delivering control signals alongside high-speed data over a single cable necessitates asymmetric simultaneous bidirectional (SBD) architectures, which are confronted with two formidable challenges: compensating for the severe channel loss in the high-speed forward channel while simultaneously cancelling strong self-interference from the local echoes.

Prior solutions such as frequency-division multiplexing (FDM)-based schemes [2] require complex passive designs, while conventional hybrids [3, 4] suffer from either noise vulnerability or output swing attenuation, which degrade the signal-to-noise ratio (SNR) and limits the channel compensation capability to moderate losses, e.g., 18.3 dB in [3].

This paper presents a 56-Gb/s PAM-4 forward channel (FC) / 2-Gb/s NRZ back channel (BC) asymmetric SBD transceiver in 28-nm CMOS. A hybrid isolation-enhancing scheme that combines an asymmetric swing architecture (1.29-V_{PP} FC vs. 0.11-V_{PP} BC) with spectral filtering is proposed to provide superior intrinsic isolation against self-interference and maximizes the SNR over a high-loss channel of 30.2 dB, eliminating the need for a power-hungry echo canceller (EC) in the high-speed FC receiver, and thus achieving exceptional energy efficiency.

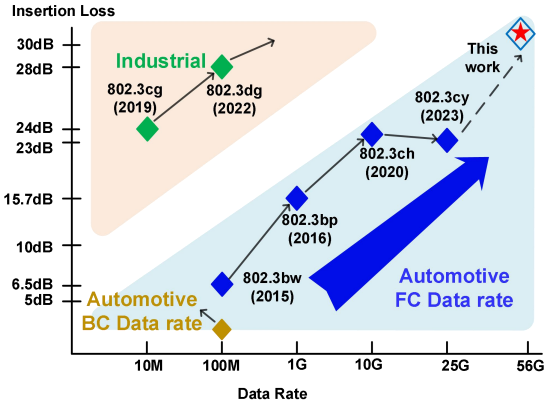


Fig. 1. Evolution of asymmetric SBD Ethernet PHY standards

II. System Architecture

Fig. 2 illustrates the architecture of the proposed asymmetric SBD transceiver, which supports concurrent 56-Gb/s PAM-4 FC and 2-Gb/s BC transmission.

In Transceiver A, the 56-Gb/s forward-channel transmitter (FC_TX) employs a quarter-rate architecture. Data from an on-chip pseudo-random-bit-sequence (PRBS) generator is serialized by a 4:1 multiplexer (MUX) that drives a 2xVDD high-swing output stage with a reconfigurable 3-tap feed-forward equalizer (FFE). A passive resistive hybrid couples the transmitted FC signal onto the channel and routes the 2-Gb/s in-bound BC signal to the local BC receiver (BC_RX). To suppress the strong out-of-band echo due to the 56-Gb/s TX_FC data, the BC_RX front-end employs an active low-pass filter (LPF). The filtered in-bound 2-Gb/s data is subsequently passed to a continuous-time linear equalizer (CTLE), followed by a variable-gain amplifier (VGA) and slicers.

In Transceiver B, the in-bound 56-Gb/s PAM-4 data is boosted by a CTLE and a VGA in the half-rate FC receiver (FC_RX), and then sampled by even/odd slicers, with a 3-tap decision-feedback equalizer (DFE) in each path to mitigate the residual inter-symbol interference (ISI). The digitized data is de-serialized by a 2:16

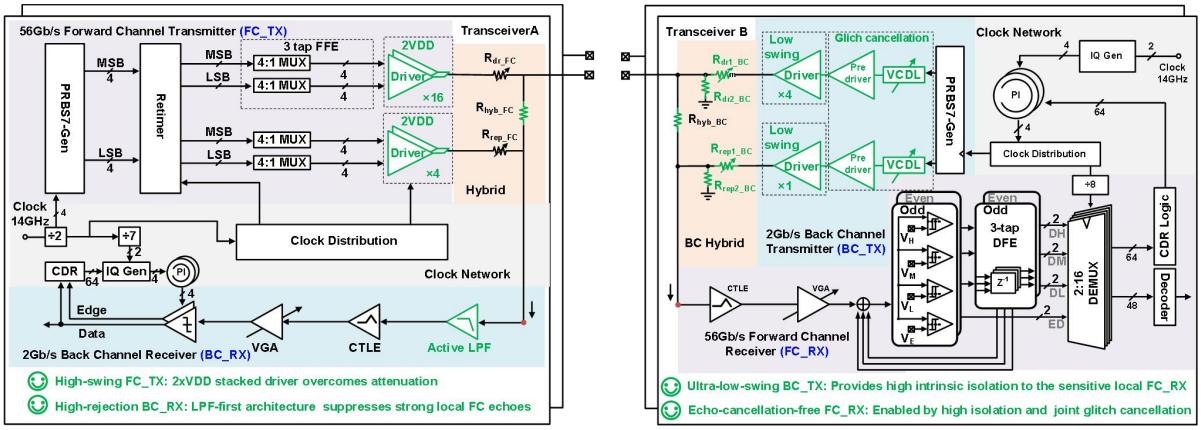


Fig. 2. Asymmetric SBD transceiver architecture.

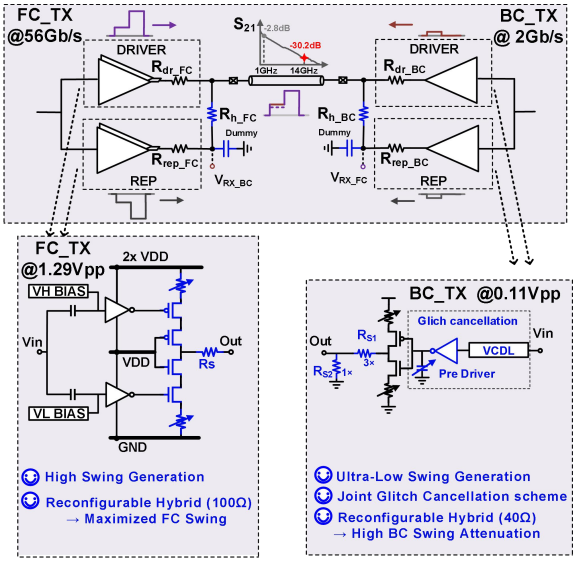


Fig. 3. Hybrid circuit implementation.

demultiplexer (DEMUX) before being sent to the clock and data recovery (CDR) logic. Correspondingly, the 2-Gb/s back-channel transmitter (BC_TX) incorporates an ultra-low-swing driver to achieve high isolation and low power.

III. Passive Resistive Hybrid Design

The hybrid circuit is critical in achieving high self-interference cancellation (SIC). A passive resistive hybrid topology valued for its inherent linearity and zero static power is employed in this design as depicted in Fig. 3, making it highly suitable for PAM-4 signaling. The resistor values (R_{dr}, R_{rep}, R_h) are selected to meet both constraints of 50-Ω impedance matching and local out-bound signal cancellation [5]. The intuition behind designing a reconfigurable, versatile hybrid topology lies in two distinct purposes: amplitude enhancement for the 56-Gb/s PAM4 high-speed FC and swing attenuation for the 2-Gb/s NRZ low-speed BC. This approach significantly simplifies the overall design compared with employing respective dedicated solutions for FC and BC as in prior arts. On the same channel, a large voltage swing compensates for the high insertion loss of the high-speed FC, while a small swing is used for the low-speed BC for ultra-low-power operation, given its minimal channel loss.

The 56-Gb/s FC_TX and 2-Gb/s BC_TX are shown in Fig. 3, where a 2xVDD stacked driver generates a 1.29-V_{PP} high-swing signal to overcome the inherent 5.4-dB amplitude attenuation introduced by the passive hybrid network. This compensates for the transmission loss and maximizes the signal-to-noise ratio. The driver employs an AC-coupled pre-driver where VH and VL bias set the DC levels required for the level-shifting inverters to properly drive the stacked PMOS and NMOS output stage. In contrast, the 2-Gb/s BC, driven by a standard inverter, adopts a two-step attenuation strategy for output swing suppression. First, R_h of 40 Ω is selected to intrinsically halve the swing to 0.45-V_{PP}. Second, the output swing is further attenuated by an on-chip 1:4 resistive divider composed of R_{S1} and R_{S2}, leading to an ultra-low-swing line signal of 0.11-V_{PP}. To ensure robust SIC performance across process, voltage, and temperature (PVT) corners, current-starved variable MOS resistors are incorporated in both drivers, enabling digital calibration of the hybrid network.

The reconfigurable hybrid design allows for path-specific optimization by selecting different resistor values for the FC and BC. Fig. 4 illustrates the output voltage swing versus the hybrid resistance (R_h). Specifically, the hybrid resistance for the back channel (R_{h_BC}) is set to 40 Ω to attenuate its swing down to 0.11 V_{PP}. Resistance lower than that would severely increase the hybrid network's sensitivity to process and impedance variations, worsening the mismatch between the main and replica drivers. For the forward channel, a 100-Ω resistance (R_{h_FC}) is employed to obtain a higher signal swing of 1.29 V_{PP}, and resistance larger than that may violate the bandwidth requirement at 56-Gb/s data rate.

To suppress the residual BC edge glitches—which can severely

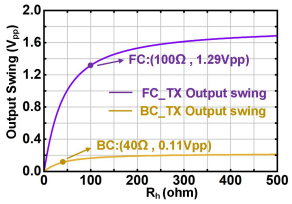
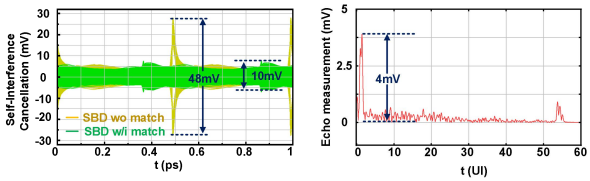
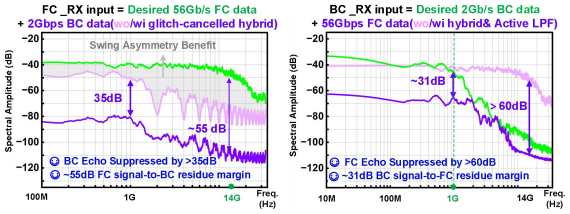


Fig. 4. Path-specific optimization of the output swing for FC and BC.



(a) (b)

Fig. 5. (a) Self-interference cancellation of 2-Gb/s BC: Eye diagram at FC_RX. (b) Channel TDR measurement.



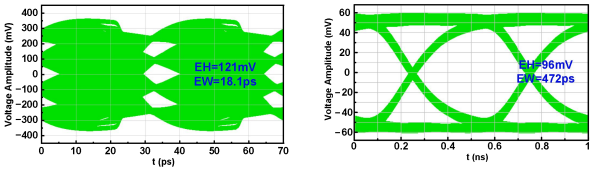
(a) (b)

Fig. 6. Simulated signal spectrum at (a) the FC receiver and (b) the BC receiver.

degrade signal integrity in SBD systems [6]—a joint glitch cancellation technique is implemented. Residual glitches arising from mismatched charge/discharge dynamics between the main- and replica-driver paths of the BC_TX could be highly destructive to the high-speed in-bound signal at FC_RX. Thus, as shown in the Fig. 3 BC_TX driver, the delay is adjusted using a voltage-controlled delay line (VCDL) to align the transitions between the main- and replica-driver path. The slew rate is compensated via a dummy capacitor to mimic the main-path load, and fine-tuned by the varactors. As verified in Fig. 5(a), the peak glitch is reduced from 48 mV down to ~10 mV by the joint glitch cancellation. Accordingly, the high-speed FC_TX does not require such complex matching, since the glitches it induces are inherently suppressed by the low-pass filtering of BC_RX, obviating the need for dedicated circuitry.

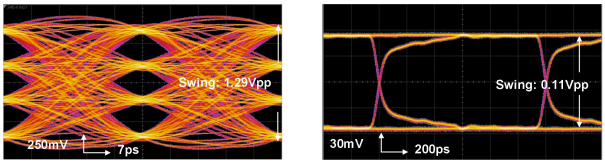
IV. Amplitude-And Frequency Isolation Validation

The large swing asymmetry (1.29 V_{PP} vs. 0.11 V_{PP}) provides 21.4 dB of intrinsic isolation from the amplitude domain, plus an extra 2.5-dB isolation from the hybrid network, bringing the total isolation to 23.9-dB between BC_TX and FC_RX in transceiver B. The time-domain reflectometry (TDR) measurement result as shown in Fig. 5(b), confirms the less than 4-mV residual echoes thanks to the ultra-low BC swing, which eliminates the necessity of a dedicated BC echo canceller in the FC receiver, thus achieving a low-power design. Furthermore, the swing asymmetry allocation inherently provides extra SNR (shaded in Fig. 6(a)) for the



(a) (b)

Fig. 7. Simulated SBD eye diagrams for (a) the 56Gb/s PAM-4 Forward Channel and (b) the 2Gb/s NRZ Back Channel.



(a) (b)

Fig. 8. Measured eye diagrams of (a) Forward Channel 56-Gb/s PAM4 TX Eye Diagram and (b) Back Channel 2-Gb/s NRZ TX Eye Diagram.

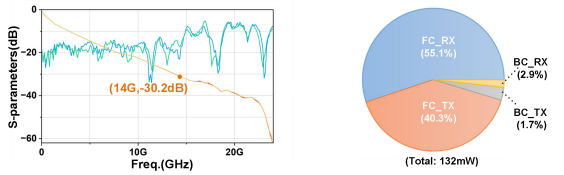
high-speed PAM-4 FC relative to the NRZ BC. By coupling the amplitude isolation with the aforementioned joint glitch-cancelling technique, an average FC signal-to-BC residue margin of 55.4 dB is achieved, as demonstrated in the Fig. 6(a) spectrum.

Correspondingly, the FC-to-BC signal interference is dominantly suppressed in the frequency domain within transceiver A. The 56-Gb/s FC echoes are attenuated first by the passive hybrid and subsequently by the active LPF at the BC_RX, which provides over 60-dB rejection at high frequencies, as illustrated in the Fig. 6(b) spectrum. This yields an average in-band BC signal-to-FC residue margin of 31.11 dB within the 1-GHz BC Nyquist frequency. Ultimately, this superior bidirectional isolation ensures the signal integrity of the high-priority 56-Gb/s FC data, allowing the FC equalization circuitry—comprising a 3-tap TX-FFE, a CTLE, and a 3-tap DFE—to compensate for the severe channel loss [7].

Simulated SBD eye diagrams over a high-loss channel of 30.2-dB are shown in Fig. 7(a) and (b) respectively, demonstrating 121-mV FC PAM-4 eye height and 18.1 ps eye width after the 3-tap DFE, and 96-mV BC NRZ eye height and 472 ps eye width after the LPF, CTLE and VGA.

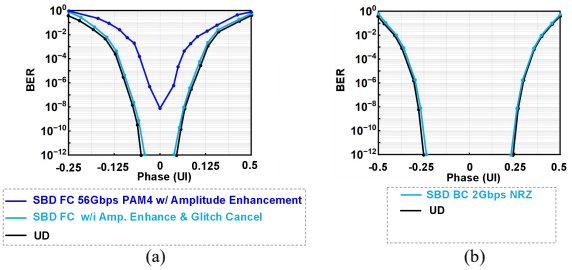
V. Measurement Results

The two asymmetric SBD transceivers were fabricated in 28-nm CMOS. The measured eye diagrams at the output of 56-Gb/s FC_TX and 2-Gb/s BC_TX are shown in Fig. 8(a) and (b), respectively, exhibiting 1.29 V_{PP} and 110 mV_{PP} differential swing. In SBD operation, transceiver A and transceiver B are connected through a 4-m coaxial cable, which introduces an insertion loss of 30.2-dB at Nyquist frequency of 14-GHz, as plotted in Fig. 9(a). Fig. 10(a) depicts the measured bathtub curve of the FC_RX in transceiver B, achieving a bit-error rate (BER) of 1e-12 in SBD mode with BC glitch cancellation enabled, nearly identical to the bathtub curve in unidirectional operation. Similarly, the BC_RX demonstrates robust performance as verified in Fig. 10(b), with a measured eye margin of 0.49 UI at 1e-12 BER. The die micrographs shown in Fig. 12.



(a) (b)

Fig. 9. (a) Channel measurement and (b) power breakdown.



(a) (b)

Fig. 10. Measured BER and bathtub curves of (a) forward channel and (b) back channel.

TABLE I PERFORMANCE COMPARISON

		ISSCC'06[8]	JSSC'20[9]	JSSC'21[3]	ISSCC'21[10]	VLSI'22[4]	This work
Technology		110-nm CMOS	28-nm CMOS	130-nm BiCMOS	14-nm CMOS	40-nm CMOS	28-nm CMOS
SBD Type		Symmetric	Symmetric	Asymmetric	Symmetric	Asymmetric	Asymmetric
Signaling		NRZ	NRZ	NRZ	PAM-4	PAM-4 & NRZ	PAM-4 & NRZ
Data rate (SBD)	FC	10 Gb/s	16 Gb/s	24 Gb/s	56 Gb/s	12 Gb/s	56 Gb/s
	BC	/	/	312.5 Mb/s	/	125 Mb/s	2 Gb/s
Driver Mode		Current mode	Voltage mode	Voltage mode	Voltage mode	Current mode	Voltage mode
SBD Architecture		R-gm hybrid	R-gm hybrid & EC	Single-ended Common-mode	Passive hybrid	WLR hybrid(BC) ∑α hybrid & LPF(FC)	Passive Resistive Network
VDD		1.2	0.9	2.5	0.8	0.9,1.1,1.2	0.9,1.8
Amplitude (FC+BC)		0.80 V_{pp}	0.40 V_{pp}	0.88 V_{pp}	/	0.85 V_{pp}	**1.29V_{PP}**
Channel IL (dB)		5	10.2	18.3	35dB	15.9	**30.2**
Area (mm^2)		1.11	0.36	0.23	/	0.24	0.46
Power Consumption (mW)	FC ONLY					67.2	126
	FC+BC	266	29.2	45	994	78.4	132
Power Efficiency(pJ/b)	FC+BC	26.6	1.83	18.76	17.75	6.5	2.28
FoM** (pJ/bit/dB)	FC+BC	5.32	0.18	1.03	0.51	0.41	**0.075**
BER		<1e-12	<1e-12	<1e-12	<1e-12	<1e-6	<1e-12

* FoM=Power Efficiency/channel IL;

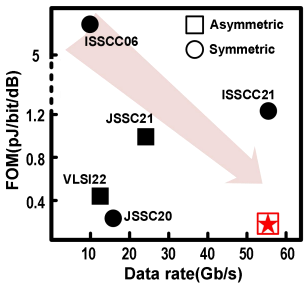


Fig. 11. Performance comparison.

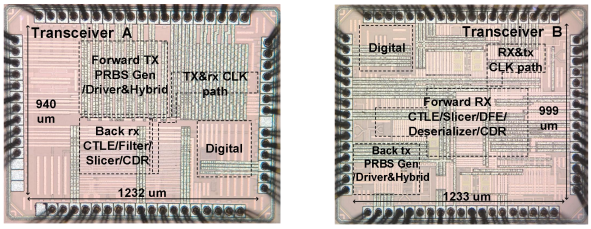


Fig. 12. Die micrographs of (a) transceiver A: FC_TX&BC_RX and (b) transceiver B: FC_RX&BC_TX.

VI. CONCLUSION

Table I and Fig. 11 benchmark this work with state-of-the-art SBD transceivers. This work achieves simultaneous 56-Gb/s FC and 2-Gb/s BC operation over a channel with 30.2-dB loss at 14-GHz. To the best of our knowledge, this work achieves both the highest FC and BC data rates with over 30-dB channel loss, among all reported asymmetric SBD transceivers, delivering a state-of-the-art FoM of 0.075 pJ/bit/dB.

ACKNOWLEDGMENT

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