A 16.5-Tb/s/mm Noise-Tolerant Transceiver with Crosstalk-Equalized Twisted Channel and Paired Pseudo-Differential Signaling

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***Abstract*—This paper presents a 16.5-Tb/s/mm single-ended 8-channel transceiver employing a crosstalk (XT)-equalized twisted channel structure for high-density chiplet interconnects. Combined with paired pseudo-differential (PPD) signaling, the proposed twisted 8-channel structure suppresses approximately 75% of crosstalk and nearly all simultaneous switching noise (SSN) in dense channel environments. The proposed PPD coding enables pseudo-differential operation with reduced driver current, shallow logic depth, and relaxed skew sensitivity. Fabricated in a 28-nm CMOS process, the prototype transceiver achieves 8×16.5 Gb/s aggregate throughput with an energy efficiency of 1.03 pJ/b under severe XT and SSN stress.**

Keywords—Chiplet, crosstalk cancellation (XTC), noise-tolerant, paired pseudo-differential (PPD) signaling, parallel I/O, single-ended transceiver, twisted-channel.

I. Introduction

With advances in packaging technologies such as silicon interposers and chiplet-based integration, modern high-bandwidth interfaces increasingly employ dense parallel I/O with finer pitch and higher channel density [1]. In such interfaces, aggregate bandwidth is often increased by scaling the I/O count rather than relying solely on higher per-lane data rates. However, as the channel pitch on the interposer shrinks to the micrometer range, the I/O structures become increasingly dense, exacerbating interference among adjacent channels. As a result, single-ended parallel interfaces are exposed to a severe noise environment.

Fig. 1 shows that both crosstalk (XT) and simultaneous switching noise (SSN) increase with edge-bandwidth density. In the dense I/O environments, their combined impact significantly degrades signal integrity. First, XT arising from electromagnetic coupling among adjacent lanes becomes more severe as channel spacing shrinks and edge-bandwidth density increases. Various crosstalk cancellation (XTC) techniques have been proposed to suppress XT [2]–[5]. However, these techniques generally require either transition-information processing from adjacent channels or the insertion of compensating paths, which increase hardware overhead and design complexity. Second, large current transients generated by drivers on the transmitter side give rise to SSN. As I/O density increases, the current fluctuation per unit area also increases, further aggravating SSN. Correlation-based signaling schemes such as C-PHY and balanced coding have been introduced to mitigate SSN [6]. However, because they rely on multi-lane correlation for data recovery, they are vulnerable to clock and channel skew.

To address these challenges, this paper presents a noise-tolerant transceiver based on a crosstalk-equalized twisted-channel structure and paired pseudo-differential (PPD) signaling. The proposed approach improves tolerance to XT and SSN without explicit aggressor-data processing or dedicated XTC circuitry, enabling a compact and energy-efficient solution for high-density single-ended parallel I/O. Fabricated in a 28-nm CMOS process, the prototype achieves 16.5 Tb/s/mm edge-bandwidth density with an overall energy efficiency of 1.03 pJ/b.

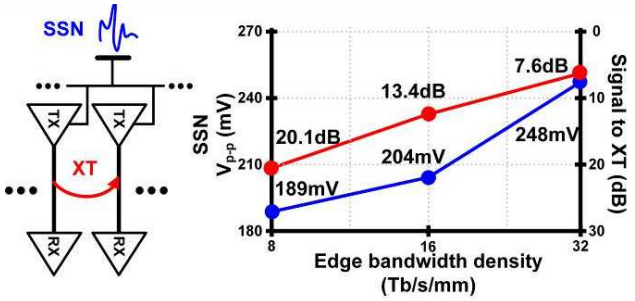


Fig. 1. SSN and signal-to-XT ratio versus edge-bandwidth density in dense parallel channel environment.

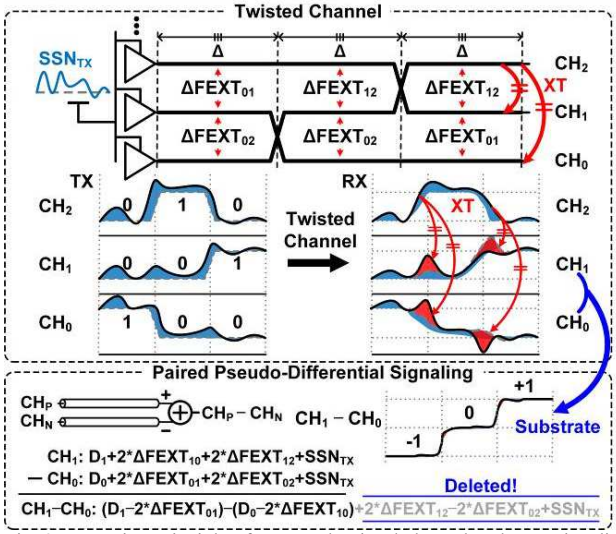


Fig. 2. Operating principle of proposed twisted channel and PPD signaling for XT and SSN suppression.

II. Proposed Noise Cancellation Technique

Fig. 2 illustrates the operating principle of the proposed twisted-channel structure with the proposed PPD for suppressing XT and SSN in high-density interfaces. In conventional channels, a victim channel is mainly affected by XT from its nearest aggressors. In contrast, the proposed twisted channel periodically permutes physical adjacency so that each channel has an equal adjacent length with all other channels, thereby equalizing the XT contribution from

Input Data			Encoded Data (Odd)		Encoded Data (Even)		Differential Level (Even)	Current Dissipations	
A	B	C	$CH_{P,O}$	$CH_{N,O}$	$CH_{P,E}$	$CH_{N,E}$	$CH_{P,E}$ - $CH_{N,E}$	$I_{P+N,O}$	$I_{P+N,E}$
Not assigned			1	1	1	1	overlap!! 0	$2I_0$	$2I_0$
1	1	1	1	0	0	0	0	I_0	0
1	1	0	1	0	0	1	-1	I_0	I_0
1	0	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	I_0
0	1	1	0	1	1	0	-1	I_0	I_0
0	1	0	0	1	0	0	1	I_0	0
0	0	1	0	0	1	0	0	0	I_0
0	0	0	0	1	0	1	-1	I_0	I_0
Encoder Logic			$CH_{P,O}$: A & B				$CH_{N,O}$: ~A & (B | ~C)		
			$CH_{P,E}$: ~A & C				$CH_{N,E}$: (A | ~B) & ~C		
Decoder Logic			A: L_O | ~H_E				B: (~L_O | L_E) & H_O		
			C: (L_O | L_E) & H_E						

Fig. 3. Paired pseudo-differential encoding map and logic.

neighboring aggressors. As a result, for the *CH0/CH1* pair, the far-end crosstalk (FEXT) induced by *CH2* appears as a common-mode noise (CMN) together with SSN. At the receiver input, pseudo-differential operation between *CH0* and *CH1* rejects this CMN. In this scheme, *CH0* and *CH1* form a differential pair, serving as the positive and negative channels, respectively. Moreover, since the residual XT within the pseudo-differential pair is incorporated into the data-recovery path, it is treated as data-dependent jitter rather than uncorrelated jitter. Therefore, by equalizing XT across channels and rejecting the resulting CMN through PPD operation, the proposed architecture improves noise tolerance without explicit aggressor-data processing or dedicated XTC circuitry.

Unlike conventional pseudo-differential signaling schemes that require multiple channels for data recovery, the proposed PPD signaling performs differential operation only within two-channel pairs, thereby fundamentally reducing sensitivity to clock and channel skew [6]. However, simply treating two single-ended channels as a differential pair leads to ambiguity, because the pairs (CH_P, CH_N) = (1,1) and (0,0) produce the same differential value, as illustrated in Fig. 3. To eliminate these overlapping states, the proposed PPD coding maps the input data such that ambiguous and current-intensive output combinations are excluded. This enables reliable pseudo-differential signaling using only two single-ended channels while preserving the simplicity of the encoding and decoding operations.

As summarized in Fig. 3, three full-rate data streams (*A*-*C*) are encoded into four driver control signals corresponding to the odd/even and positive/negative channel data, thereby generating the PPD output patterns. At the receiver, the original data are reconstructed by performing the reverse operation of the encoder. By avoiding overlapping symbols while maintaining 75% pin efficiency, the proposed coding enables pseudo-differential operation with relaxed skew sensitivity and low logic complexity. In addition, excluding current-intensive states reduces the average driver current by 37.5%, thereby improving energy efficiency.

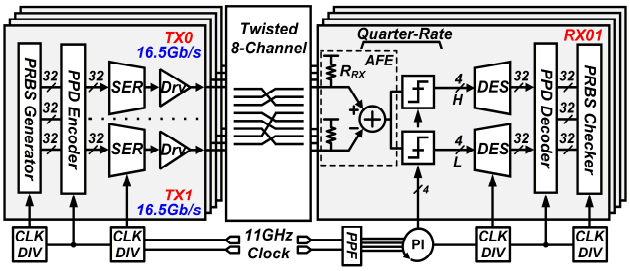


Fig. 4. Overall architecture of the proposed noise-tolerant transceiver.

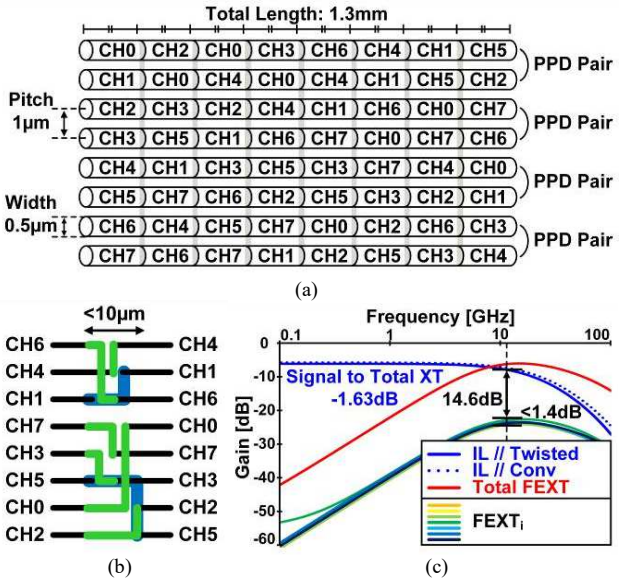


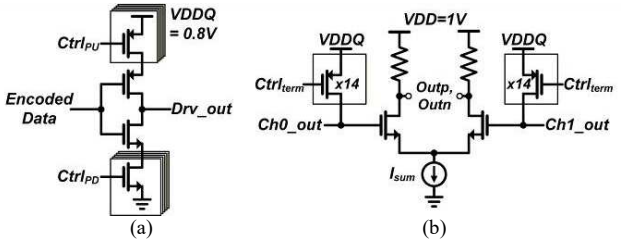
Fig. 5. (a) Proposed 8-channel twisting sequence for equalizing XT contribution, (b) twisted-structure detail, and (c) channel responses of twisted channel and conventional channel.

III. Circuit Implementations

Fig. 4 illustrates the overall architecture of the proposed 8-channel transceiver employing the twisted-channel structure and PPD signaling. The transceiver consists of eight transmitters and four receivers, where each receiver processes data from two transmitters as a PPD channel. At the transmitter side, PRBS generators and PPD encoders generate coded data streams. The signal is driven by voltage-mode drivers and transmitted through the twisted channels. At the receiver, paired channels perform pseudo-differential operation to suppress XT and SSN, and the outputs are sampled using high- and low-voltage reference levels. The sampled data is then decoded by the PPD decoder, and a PRBS checker is used to measure a bit error rate (BER).

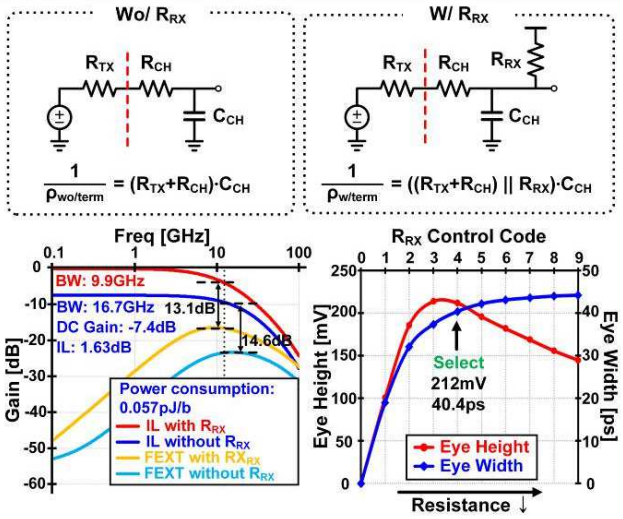
A. Crosstalk-Equalized Twisted 8-Channel Structure

Fig. 5 shows the implementation details and channel responses of the proposed twisted 8-channel structure. By permuting the channel order using vias, as shown in Fig. 5(a), the physical routing is periodically twisted, as illustrated in Fig. 5(b). The simulated channel responses in Fig. 5(c) show that the twisted-channel structure equalizes the crosstalk contributions from all aggressors. Specifically, at the Nyquist frequency, the signal is 14.6 dB larger than the largest individual XT, the signal-to-total-XT ratio is −1.63 dB, and the variation among the individual FEXT components is within 1.4 dB. Since the physically twisted segments are very short (<10 μm), the insertion loss of the twisted channel remains nearly unchanged compared to that of the



(a) (b)

Fig. 6. Circuit implementations of (a) P-over-N driver, (b) termination, and PPD summer.



(a) (b)

Fig. 7. (a) Simulated channel response with and without receiver input termination (R_{RX}), and (b) eye margins with respect to R_{RX}.

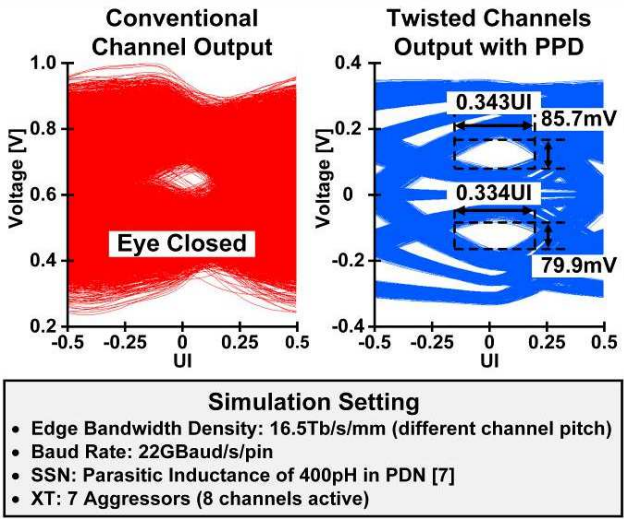
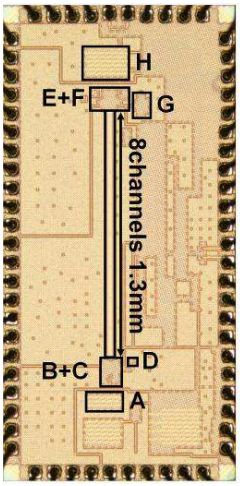


Fig. 8. Simulated eye diagrams of conventional straight channel output and twisted channel output with PPD under same edge-bandwidth density of 16.5 Tb/s/mm.

conventional straight channel. In the 8-channel structure, for each pseudo-differential pair, XT from the remaining six channels appears as a common-mode component and is rejected by PPD operation, while the residual XT within the pair is incorporated into the data-recovery path as data-dependent jitter. As a result, when combined with PPD signaling, the proposed twisted 8-channel structure mitigates XT by 75% and suppresses SSN.



Block (8ch)	Power(mW)	Area(μm²)
A. S2D Encoder	4.55	7,526
B. Serializer	39.89	7,525
C. Driver	9.91	729
D. TX CLK Path	8.11	1,452
E. Summer + Sampler	49.18	3,357
F. Deserializer	9.47	4,968
G. RX CLK Path	4.35	6,313
H. S2D Decoder + PRBS CHK.	11.34	20,984
Total TX	62.46	17,232
Total RX	73.34	35,622
@132Gb/s TX Energy Efficiency: 0.473pJ/b RX Energy Efficiency: 0.556pJ/b		

Fig. 9. Die micrograph with power and area breakdowns.

B. *Transceiver Architecture*

In the transmitter, the PPD-encoded data are serialized and transmitted through a 0.8-V P-over-N driver, as shown in Fig. 6(a). At the receiver, P-type terminations are introduced for bandwidth extension, and the two input signals are combined by the PPD summer shown in Fig. 6(b), followed by quarter-rate sampling and deserialization.

Fig. 7 shows the simulated channel responses and eye margins with and without the receiver input termination, R_{RX}. In the RC-dominant on-chip channel, adding R_{RX} makes the channel parasitic capacitance (C_{CH}) see $(R_{TX}+R_{CH}) \parallel R_{RX}$, shifting the dominant pole to a higher frequency and providing a 1.69× bandwidth extension [8]. The value of R_{RX} is optimized by considering both eye height and eye width. Although the termination introduces additional power consumption, the overhead is only 0.057 pJ/b according to the simulation results. This small penalty reduces the need for additional equalization, resulting in enhanced energy efficiency.

Fig. 8 compares the simulated eye diagrams of the conventional straight-channel output and the proposed twisted-channel output with PPD signaling at the same edge-bandwidth density of 16.5 Tb/s/mm. The simulations are performed at 22 Gbaud/s/pin under severe XT and SSN stress. SSN is modeled using a 400 pH parasitic inductance in the power distribution network (PDN), and XT is evaluated with seven aggressors, corresponding to simultaneous operation of all 8 channels. Under these conditions, the conventional straight channel exhibits a closed eye due to severe XT and SSN. In contrast, the proposed twisted channel with PPD signaling effectively rejects the equalized XT and SSN, achieving a clear eye opening of 0.334 UI and 79.9 mV.

IV. Measurement Results

Fig. 9 shows the die micrograph with the power and area breakdown. Operating at 16.5 Gb/s/pin over 8 channels, corresponding to an aggregate data rate of 132 Gb/s, the prototype transmitter and receiver achieve energy efficiencies of 0.473 pJ/b and 0.556 pJ/b, respectively. To evaluate tolerance to XT and SSN, the number of simultaneously active channels is increased from 2 to 8. As shown in Fig. 10, which presents the worst-case measured eye diagram between the H and L levels, the eye diagram remains open under 8-channel operation, providing a voltage margin of 63 mV and a timing

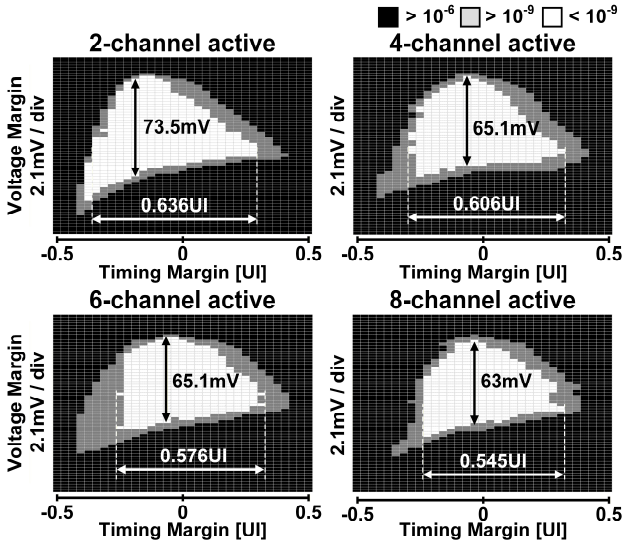


Fig. 10. Measured eye diagrams (worst case of H/L) of proposed transceiver at 16.5 Gb/s/pin under different SSN and XT stress (2/4/6/8-channel active).

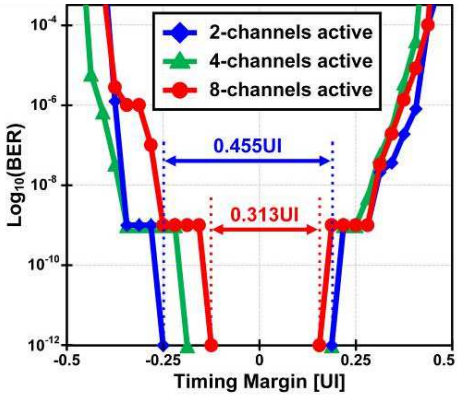


Fig. 11. Measured bathtub curves of proposed transceiver at 16.5 Gb/s/pin under different SSN and XT stress (2/4/8-channel active).

margin of 0.545 UI, compared to 73.5 mV and 0.636 UI in the 2-channel case. Fig. 11 shows that the measured timing margin at a BER of 10^{-12} decreases from 0.455 UI for 2-channel operation to 0.313 UI for 8-channel operation, while still maintaining a sufficient margin under increased XT and SSN stress.

Table I summarizes the measured performance and compares it with prior works. The proposed transceiver achieves the highest edge-bandwidth density of 16.5 Tb/s/mm among the compared works, even when the total XT exceeds the signal by 1.52 dB. It also obtains an overall energy efficiency of 1.03 pJ/b while providing robust tolerance to XT and SSN.

V. Conclusion

This work demonstrates that combining a crosstalk-equalized twisted-channel structure with paired pseudo-differential (PPD) signaling effectively improves noise tolerance in high-density chiplet interconnects. By equalizing aggressor-induced XT across channels and rejecting the resulting common-mode noise through PPD operation, the proposed architecture suppresses XT and SSN without explicit aggressor-data processing or dedicated XTC circuitry. In addition, the proposed PPD coding enables energy-efficient pseudo-differential signaling with reduced driver current, low logic complexity, and relaxed skew sensitivity. The measured eye and bathtub results verify sufficient voltage and timing margins even as the XT/SSN stress increases from 2-channel to 8-channel operation. The prototype achieves 16.5 Tb/s/mm edge-bandwidth density with an overall energy efficiency of 1.03 pJ/b.

Table I. Performance Comparison With Other Noise Cancellation Techniques

	ISSCC'20 [2]	ISSCC'25 [3]	SOVC'24 [4]	JSSC'23 [5]	This Work
Process [nm]	65	28	40	28	28
Signaling	NRZ	PAM-3	NRZ	Fibonacci	PPD
XTC Scheme	FS-XTC	FS-XTC	Coupling-Balanced	Coding	Twisted Channel & Coding
Pin-efficiency [%]	100	150	100	75	75
Data Rate [Gb/s/pin]	4	42	20	10	16.5
Type of Noise Tolerance	XT	XT, PN	XT	XT	XT, SSN
Channel Length [mm]	6	2	1	N/A	1.3
Channel Pitch [μm]	0.5	2.5	1.5	N/A	1.0
# of Aggressors	4	2	2	3	7
Signal to Total XT Ratio [dB]	-5.26*	6.7*	0.98*	-1.62*	-1.52
Energy Efficiency [pJ/b]	1.5	0.275	0.246	1.29	1.03**
TRX Area [mm^2/ch]	0.0083	0.0012	0.0021	0.004	0.0066**
Edge-Bandwidth Density [Tb/s/mm]	8	9.16	13.3	N/A	16.5

*Calculated from channel response ** Including PRBS Checker

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