An Interleaved 4-Fine-Level Buck-or-Boost Converter Utilizing Addition-Subtraction Modes Achieving 2.3µs Recovery Time and <5mV Output Ripple for OLED Displays

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***Abstract*—This paper proposes an interleaved 4-fine-level buck-or-boost (4FLBB) hybrid converter for mobile OLED displays. By proposing addition-subtraction modes, the design extended the maximum theoretical conversion ratio (CR) to 2 without extra flying capacitors. The architecture doubles the effective inductor current frequency without extra switching loss and achieves $0.5V_{IN}$ fine steps at the switching node, significantly reducing the output ripple, LC value, and transient recovery time. Fabricated in a 180nm CMOS process, the chip maintains an output ripple of ≤5mV at a compact $L \times C_O$ constant of 2.2 p(rad/s)$^{-2}$. The converter also exhibits a 2.3 µs recovery time and a 96.04% peak efficiency.**

Keywords—interleaved 4-fine-level buck-or-boost, hybrid converter, mobile OLED displays, addition-subtraction modes, ripple reduction, LC value reduction, fast transient response

I. Introduction

For flicker-free, compact-size mobile OLED displays, the power supply must exhibit low output ripple (ΔV_O), high efficiency, and incorporate small LC passives. Nevertheless, minimizing the output ripple and off-chip LC size involves an inherent trade-off. Modern OLEDs now operate from 2V to 6V to support advanced brightness levels and panel architectures. Accommodating this wide range from a lithium battery supply requires a buck-boost (BB) converter with a wide conversion ratio range of 0.5 to 2. Furthermore, a fast transient response is needed for precise, frequent brightness adjustment. Unfortunately, as illustrated in Fig. 1(a), conventional non-inverting buck-boost converters (CBBC) [1] suffer from a right-half-plane zero (RHPZ) that limits the transient speed, and a discontinuous output delivery current (I_D) that causes excessive output voltage (V_O) spikes.

To address these challenges, the dual-path hybrid BB [2,3] in Fig.1(b) can provide continuous I_D and reduced inductor current, but they suffer from C_F inrush current that induces output spikes. The inductor-last BB topologies [4,5] shown in Fig. 1(c) can eliminate the RHPZ and suppress output ripple by delivering continuous I_D. However, their switching node (V_X) toggles with a full V_{IN} step, which still necessitates bulky LC filters to achieve minimal voltage ripple. To further reduce the passive size, the recent 3-fine-level BB [6,7] in Fig. 1(d) reduces the V_X step to $0.5V_{IN}$. However, these topologies are theoretically limited to a maximum conversion ratio of 1.5. Specifically, to obtain $V_X = 2V_{IN}$, both flying capacitors are stacked with V_{IN}, resulting in a discharging state. When connecting V_X to $1.5V_{IN}$, one capacitor is discharging, while the other lacks a $0.5\ V_{IN}$ source to charge. Consequently, the required charge balance of two capacitors cannot be maintained to achieve conversion ratios from 1.5 to 2.

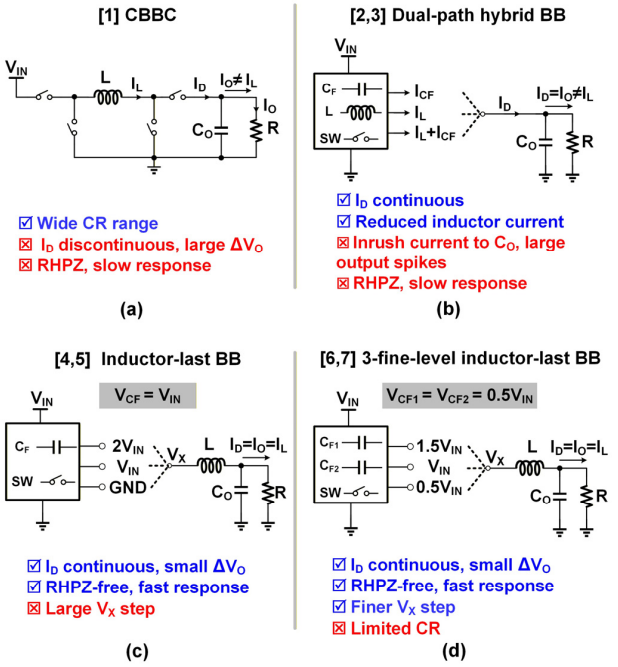

Fig. 1. Prior works of BB converter.

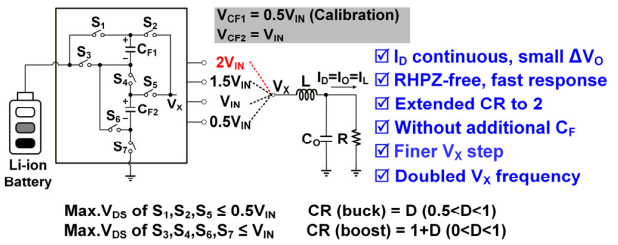

Fig. 2. Proposed 4FLBB hybrid converter.

II. Proposed 4FLBB Converter

A. Overall Structure of Proposed Converter

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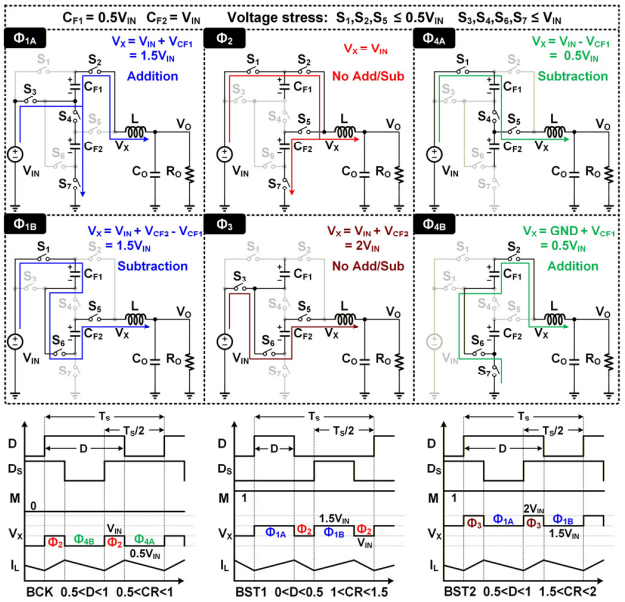


Fig. 3. Operating phase and key switching waveforms of the proposed converter in BCK, BST1 and BST2 modes.

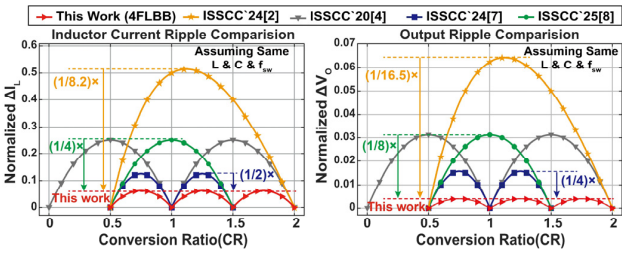


Fig. 4. Theoretical comparison of the normalized inductor current ripple and output voltage ripple.

As shown in Fig. 2, this paper proposes an interleaved 4-fine-level buck-or-boost (4FLBB) hybrid converter. It retains the inductor-last structure to eliminate the RHPZ and supply continuous I_D, ensuring small output ripple and fast transient response. By utilizing the proposed addition-subtraction control method, where V_{CF1} is maintained at $0.5V_{IN}$ and V_{CF2} is established at V_{IN}, the Vx node can produce four fine levels: $0.5V_{IN}$, V_{IN}, $1.5V_{IN}$, and $2V_{IN}$. This allows the converter to reach the theoretical CR range of 0.5 to 2 without extra C_F. Furthermore, by time interleaving, it can double the effective inductor current frequency without additional switching loss.

B. *Operation Principle of 4FLBB Converter*

The operation of the proposed 4FLBB converter is realized by the proposed addition-subtraction mode. This mode relies on the reconfigurable connection of C_{F1} to either add to or subtract from a specific voltage node. The two C_Fs are regulated differently: V_{CF2} is established at V_{IN} by its periodic parallel connection to V_{IN}, while V_{CF1} is maintained at $0.5V_{IN}$ by calibration. As illustrated in Fig. 3, the six operating phases (Φ_{1A}-Φ_{4B}) realize the four V_X levels through the following configurations:

For the $1.5V_{IN}$ level, Φ_{1A} operates in addition mode by stacking C_{F1} on top of V_{IN} to synthesize a V_X level of V_{IN} + V_{CF1}, while Φ_{1B} operates in subtraction mode by subtracting C_{F1} from the V_{IN} + V_{CF2} rail to generate a V_X of (V_{IN} + V_{CF2}) − V_{CF1}. Similarly, for the $0.5V_{IN}$ level, Φ_{4B} achieves addition mode by connecting C_{F1} to GND to synthesize a V_X level of GND + V_{CF1}, while Φ_{4A} achieves subtraction mode by

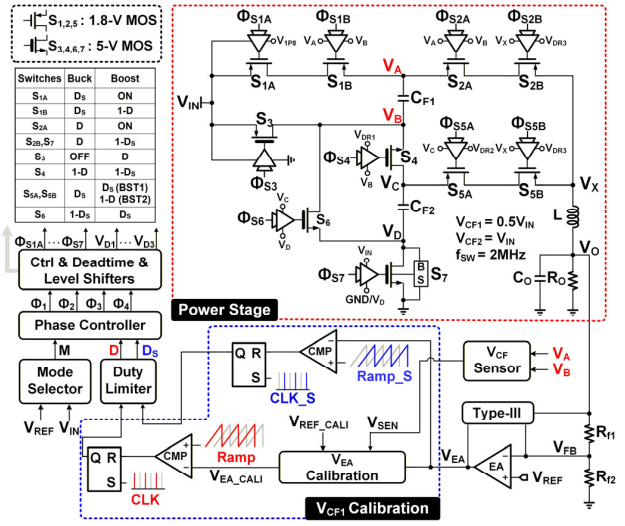


Fig. 5. Overall structure of the proposed 4FLBB converter.

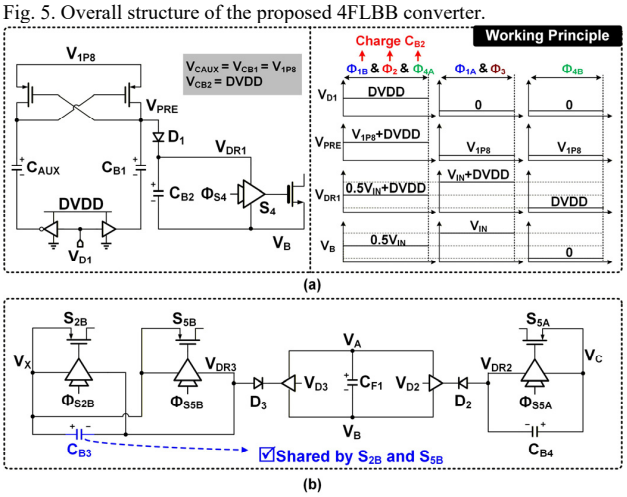


Fig. 6. Implementation of (a) 3-voltage-level bootstrap for S_4 and (b) $S_{2B,5A,5B}$ driver utilizing a shared C_{B3}.

subtracting C_{F1} from V_{IN} to generate a V_X of V_{IN} − V_{CF1}. Additionally, Φ_2 and Φ_3 are no addition/subtraction mode and C_{F1} is kept floating to provide V_X levels of V_{IN} and $2V_{IN}$, respectively. By interleaving these addition and subtraction paths within a single switching cycle, the system roughly ensures the C_{F1} charge balance and doubles the effective V_X node frequency.

The converter operates across different phases depending on the two interleaving duty cycles (D, D_S) and the mode-indicator (M). In the buck (BCK) mode (M=0, 0.5<CR<1), the operating sequence is $\Phi_2 \rightarrow \Phi_{4B} \rightarrow \Phi_2 \rightarrow \Phi_{4A}$. V_X toggles between $0.5V_{IN}$ and V_{IN}. The $0.5V_{IN}$ level is formed by either the addition mode Φ_{4B} or the subtraction mode Φ_{4A}. In the boost-1 (BST1) mode (M=1, 1<CR<1.5), the operating sequence is $\Phi_{1A} \rightarrow \Phi_2 \rightarrow \Phi_{1B} \rightarrow \Phi_2$. V_X alternates between V_{IN} and $1.5V_{IN}$. The $1.5V_{IN}$ level is generated by the addition mode Φ_{1A} and the subtraction mode Φ_{1B}. In the boost-2 (BST2) mode (M=1, 1.5<CR<2), the operating sequence is $\Phi_3 \rightarrow \Phi_{1A} \rightarrow \Phi_3 \rightarrow \Phi_{1B}$. V_X alternates between $1.5V_{IN}$ and $2V_{IN}$.

Comparing with prior arts, this work reduces the normalized inductor current ripple (ΔI_L) and output ripple ΔV_O by a maximum factor of 8.2× and 16.5×, respectively, as shown in Fig. 4. It can also reduce the inductor value to

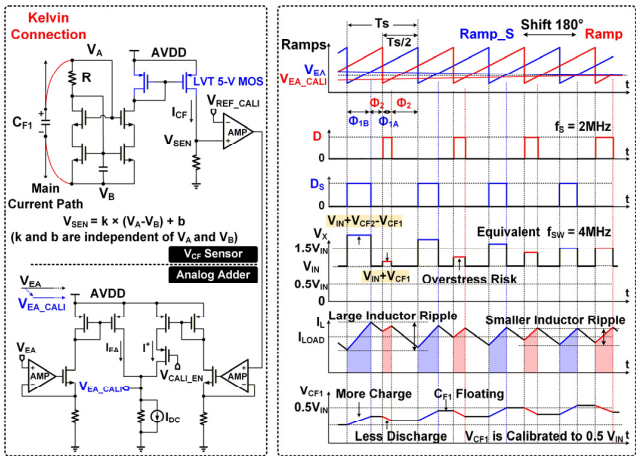
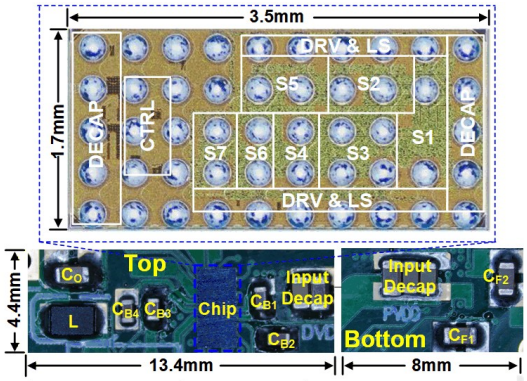


Fig. 7. (a) V_{CF} sensing and calibration schematic (b) Calibration process of 4FLBB in BST1 mode ($D<0.5$, $V_{CF}<0.5V_{IN}$).



Components	Description	Size
C_{B1},C_{B2},C_{B3},C_{B4}	10nF	0402 (1×0.5×0.5 mm³)
C_{F1},C_{F2}	10μF	0603 (1.6×0.8×0.8 mm³)
C_O	2.2μF	0603 (1.6×0.8×0.8 mm³)
L	1μH (60mΩ)	0805 (2×1.2×0.8 mm³)

Fig. 8. Die micrograph and PCB photo.

enhance the transient response. This significant improvement is due to the four fine voltage levels and the frequency-doubling effect of the addition-subtraction interleaving strategy. Moreover, it breaks the CR limit of 1.5 in prior work without adding extra capacitors.

C. *Implementation of Converter*

Fig. 5 exhibits the block diagram of the proposed 4FLBB system. $S_{1,2,5}$ utilize 1.8V devices and use the back-to-back structure to prevent leakage current across different modes. $S_{3,4,6,7}$ are implemented with 5V devices. To drive S_4, as shown in Fig. 6(a), a 3-voltage-level bootstrap circuit is employed to accommodate its source voltage variations. By charging C_{B2} in Φ_{1B}, Φ_2 and Φ_{4A}, the bootstrap circuit is enabled to operate in all three modes, as this ensures at least one charging phase is available in each mode. To reduce the number of capacitors, as shown in Fig 6(b), S_{2B} and S_{5B} share the same bootstrap path (C_{B3}, D_3) charged by C_{F1}. S_{5A} is driven by C_{B4}, which is also established from C_{F1}. Other switches are driven by flying capacitors or regular voltage supplies directly.

The converter switches at 2MHz and the voltage loop employs type-III compensation without the RHPZ. In the calibration loop, the sensing signal of V_{CF1} - V_{SEN} is

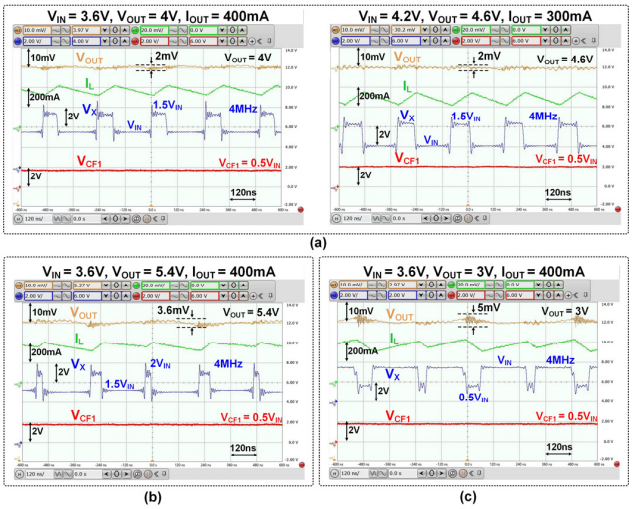


Fig. 9. Measured steady-state waveforms of (a) BST1 mode (b) BST2 mode (c) BCK mode.

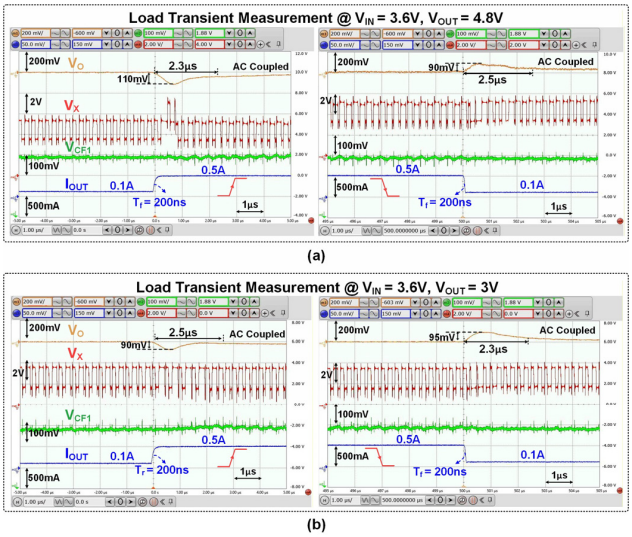


Fig. 10. Measured load transient responses of (a) BST mode (b) BCK mode

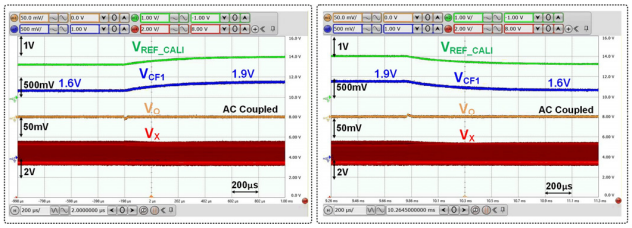


Fig. 11. Measured waveforms of the dynamic calibration tracking process.

compared to V_{REF_CALI}, and the resultant offset is added to V_{EA} to generate the V_{EA_CALI} signal. These two EA signals modulate the interleaved duty D_S and D, respectively, thereby maintaining V_{CF1} at $0.5V_{IN}$. The driving signals of the switches are generated according to the logic mapping table. For V_{CF} sensing, a V_{CF} sensor in Fig. 7(a) generates the V_{SEN} signal linear to V_{CF1} via a Kelvin-connected differential sensor [9]. In particular, as shown in Fig 7(b), the calibration process in BST1 shows that when $V_{CF1}<V_{REF\_CALI}$, the system changes the duty cycles of specific phases (e.g., Φ_{1B} and Φ_{1A}). The charging time will be larger than the discharging time until V_{CF1} reaches the target. This method eliminates

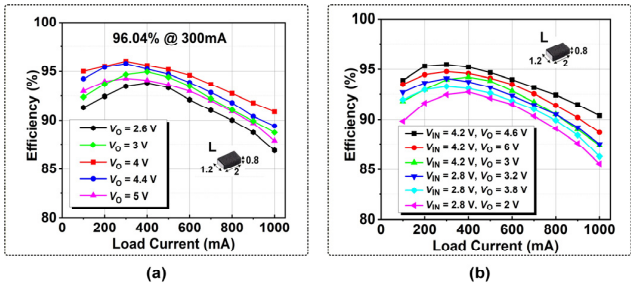


Fig. 12. Measured power efficiencies at different V_O for (a) V_{IN} = 3.6V and (b) V_{IN} = 2.8V and 4.2V.

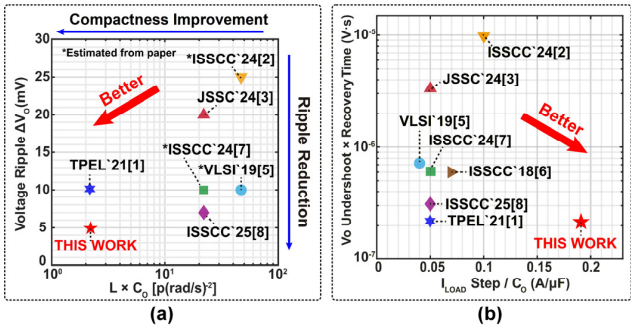


Fig. 13. Benchmarks: (a) ripple performance (b) transient performance.

overstress risks on power switches and ensures the ripple reduction performance.

III. Measurement Results

The proposed 4FLBB was fabricated in a 180nm CMOS process, employing a 1μH inductor (DCR = 60mΩ) and 2.2μF output capacitor. Fig. 8 shows the chip and PCB test board micrograph. Fig. 9 presents steady-state waveforms under different modes, demonstrating the four fine levels and doubled switching frequency of V_X. The output voltage ripple is smaller than 5mV. Fig. 10 shows the measured load transient responses with a load step of 0.4A and an edge within 200ns. For V_{OUT}=4.8V, the system exhibits a recovery time of 2.3μs/2.5μs with 110mV undershoot and 90mV overshoot. Similarly, at V_{OUT}=3V, the recovery time is 2.5μs/2.3μs. The dynamic calibration tracking is verified in Fig. 11. As V_{REF_CALI} varies, V_{CF1} follows linearly while V_O remains undisturbed. The measured efficiency curve is plotted in Fig. 12, showing a peak efficiency of 96.04% at I_O=0.3A, noting that a compact inductor with relatively high DCR is adopted. As illustrated in Fig. 13(a), the benchmark of ripple exhibits that this work achieves the smallest ripple with the minimal LC_O product. Fig. 13(b) shows the transient performance benchmark comparing recent works, comprehensively evaluating four critical parameters: I_{LOAD} step, C_O, undershoot of V_{OUT} and recovery time. As illustrated, the proposed work achieves the best overall transient performance. Table I compares this work against the state-of-the-art buck-or-boost converters. The work achieves a 4MHz equivalent frequency, supports a wide 2-6V output range at 100mA-1A. It realizes the smallest volume of inductor and achieves an ultra-low $L \times C_O$ product of 2.2 $p(rad/s)^{-2}$, which is 10-20× smaller than prior works. The converter maintains a $\Delta V_O \leqslant$ 5mV. The approximate 2.3μs recovery time in both buck and boost modes exhibits the fastest load transient response.

IV. Conclusion

This paper presents an interleaved 4FLBB hybrid converter featuring fast transient response, small output ripple and reduction in LC value for mobile OLED displays. By adopting the addition-subtraction control modes, the proposed converter provides four fine V_X levels to significantly suppress ripples, while extending the CR up to 2.0 without additional flying capacitors. This strategy also realizes a doubling of the inductor current frequency. The inductor-last structure eliminates the RHP zero, ensuring continuous output current and enabling rapid transient recovery. Measured results show an output ripple of less than 5mV with a 1μH inductor and a peak efficiency of 96.04%. The converter demonstrates a transient recovery time of only 2.3μs, providing an integrated power management solution that meets the stringent ripple and volume requirements of portable electronics.

TABLE I. Performance summary and comparison

Work		TPEL`21[1]	ISSCC`20[4]	VLSI`19[5]	ISSCC`24[7]	ISSCC`25[8]	**This Work**
Process(nm)		130	90	250	180	180	**180**
Switch Vds		V_{IN} × 2 V_O × 2	V_{IN} × 5	V_{IN} × 2 $2V_{IN}$ × 2	1/2V_{IN} × 7	1/2V_{IN} × 7	**1/2V_{IN} × 3 V_{IN} × 4**
Equivalent Frequency (MHz)		6	0.8-3	1.45	2	1	**2×2 = 4 (f_{SW} = 2)**
Input voltage (V)		2.3-5	2.5-5	2.9-6.3	2.8-4.2	2.8-4.2	**2.8-4.2**
Output voltage (V)		1.5-3.6	0.4-9	4.6	3.3	3.3	**2-6**
C_O/C_F (μF/μF)		10 / -	4.7 / 10	10 / 0.47	10 / 2×10	10 / 2×4.7	**2.2 / 2×10**
Inductor	Inductance/DCR (μH/mΩ)	0.22 / -	2.2 / -	4.7 / -	2.2 / 110	2.2 / 12	**1 / 60**
Inductor	Volume (mm^3)	N/A	N/A	N/A	4.5 (2.3×)	234 (121.9×)	**1.92 (1×)**
$L \times C_O$ [$p(rad/s)^{-2}$]		2.2 (1×)	10.34 (4.7×)	47 (21×)	22 (10×)	22 (10×)	**2.2 (1×)**
Output Current (A)		0-1	0-1	0.05-0.6	0.05-1	0.1-1	**0.1-1**
V_X		0 / V_{IN} / V_O	0 / V_{IN} / $2V_{IN}$	0 / V_{IN} / $2V_{IN}$	0.5V_{IN} / V_{IN} / 1.5V_{IN}	0.5V_{IN} / 1.5V_{IN}	**0.5V_{IN} / V_{IN} / 1.5V_{IN} / 2V_{IN}**
Peak Efficiency (%)		91.7	96.8	97.46	97.2	98.3	**96.04**
ΔV_O		<10mV	N/A	<10mV	<10mV	<7mV	**<5mV**
Recovery time (μs)		10 / 9	N/A	9 / -	25 / 27.5	9.5 / 9	**2.3 / 2.5**
Under / Overshoot (mV/mV)		70 / 65	N/A	80 / -	21.6 / 18.3	31 / 25	**110 / 90**
CR_Theoretical		0-∞	0-2	0-2	0.5-1.5	0.5-1.5	**0.5-2**

References

[1] M. Singh and A. A. Fayed, "A 1-A 6-MHz digitally assisted Buck–Boost converter with seamless mode transitions and fast dynamic performance for mobile devices," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4338-4351, Apr. 2021.

[2] D. -H. Kim and H. -S. Kim, "8.2 A 96.9%-peak-efficiency bilaterally-symmetrical hybrid Buck-Boost converter featuring seamless single-mode operation, always-reduced inductor current, and the use of all CMOS switches," *ISSCC*, pp. 146-148, Feb. 2024.

[3] J. Jin, Y. Zhou, C. Chen, X. Han, W. Xu and L. Cheng, "A battery-to-3.4 V hybrid Buck-Boost converter with always reduced conduction loss," *IEEE Journal of Solid-State Circuits*, vol. 60, no. 6, pp. 2194-2205, Jun. 2025.

[4] J. Baek et al., "11.7 A voltage-tolerant three-level Buck-Boost DC-DC converter with continuous transfer current and flying capacitor soft charger achieving 96.8% power efficiency and 0.87μs/V DVS rate," *ISSCC*, pp. 202-204, Feb. 2020.

[5] Y. -A. Lin et al., "A right-half-plane zero-free Buck-Boost DC-DC converter with 97.46% high efficiency and low output voltage ripple," *VLSI*, pp. C174-C175, Jun. 2019.

[6] M. -W. Ko et al., "A 97% high-efficiency 6μs fast-recovery-time buck-based step-up/down converter with embedded 1/2 and 3/2 charge-pumps for li-lon battery management," *ISSCC*, pp. 428-430, Feb. 2018.

[7] S. Zhao, C. Zhan and Y. Lu, "8.4 A fast-transient 3-fine-level Buck-Boost hybrid DC-DC converter with half-voltage-stress on all switches and 98.2% peak efficiency," *ISSCC*, pp. 150-152, Feb. 2024.

[8] J. Jin, R. Yang, W. Xu and L. Cheng, "9.11 A 98.3%-peak-efficiency single-mode hybrid buck-boost converter with 7mV maximum output ripple for Li-Ion battery management," *ISSCC*, pp. 198-200, Feb. 2025.

[9] J. Tang, J. Jiang, L. Zhao, X. Zhang, K. Wei and C. Huang, "A monolithic 3-level single-inductor multiple-output Buck converter with state-based non-linear control capable of handling 1A/1.5ns transient with on-die LC," *CICC*, pp. 1-2, Apr. 2024.