A 12b 25GS/s Time-Interleaved SAR ADC with 4x Oversampling and TDC-Assisted Conversion in 7nm FinFET

Jiazhen Ni*, Minqing Cai†, Chen Chen†, Zhanpeng Yang†, Xinrong Hu†, Gaofeng Jin†, Bao Luo†, Biao Wang†, Yufeng Yao†, Xiang Gao* and Seung-Chul Lee†
Email: xiang.gao@zju.edu.cn
*College of Integrated Circuits, Zhejiang University, Hangzhou 310027, China
†Shanghai Formula Microelectronics Co., Ltd., Shanghai 201203, China.

***Abstract*—A 12-bit, 25GS/s 128-way time-interleaved SAR ADC is implemented in a 7-nm FinFET process. The ADC employs 4x oversampling, enabled by a 100-GS/s internal sampling rate, to deliver a 25-GS/s effective output rate while mitigating jitter-induced noise—a key performance bottleneck at multi-GHz input frequencies. The design incorporates a linearity-enhanced source follower, a locally buffered bootstrapped switch, and a hybrid SAR–TDC architecture that leverages redundancy-assisted calibration. The prototype achieves 53.3-dB SNDR at 0.39 GHz and 47.5-dB SNDR at an 11.95-GHz input, corresponding to Schreier figures of merit (FoMs) of 157.3 dB and 151.5 dB, respectively.**

***Index Terms*—Time-interleaved ADC, hybrid SAR-TDC, oversampling, redundancy calibration, FinFET**

I. Introduction

Time-interleaved (TI) architectures have enabled sampling rates exceeding 100 GS/s [1]; however, their overall dynamic performance is constrained by practical non-idealities, particularly channel mismatches, front-end sampling nonlinearity, and clock jitter. This work addresses these challenges through five key techniques: (1) a 4× oversampling mode (from 100 GS/s to 25 GS/s) to reduce jitter-induced noise; (2) a comprehensive on-chip foreground calibration engine for channel mismatches; (3) a linearity-enhanced front-end source follower paired with a locally buffered bootstrapped switch; (4) a power-efficient sub-ADC design employing a hybrid SAR-TDC topology with built-in redundancy, in which the comparator seamlessly operates as a voltage-to-time converter (VTC) during the LSB cycles; and (5) an amplitude- and time-domain redundancy scheme that ensures robust TDC calibration across wide process, voltage, and temperature (PVT) variations.

II. Architecture

The ADC employs a two-level hierarchical sampling structure (2×16×4), interleaving 128 sub-ADCs, as depicted in the upper part of Fig. 1. The first-stage sampler clocks (Q_{S1}–Q_{S32}) are generated from a 12.5 GHz external differential clock using a delay-locked loop and a divider chain [1].

The overall operation follows the timing scheme illustrated in the lower part of Fig. 1. Specifically, each first-stage sampler

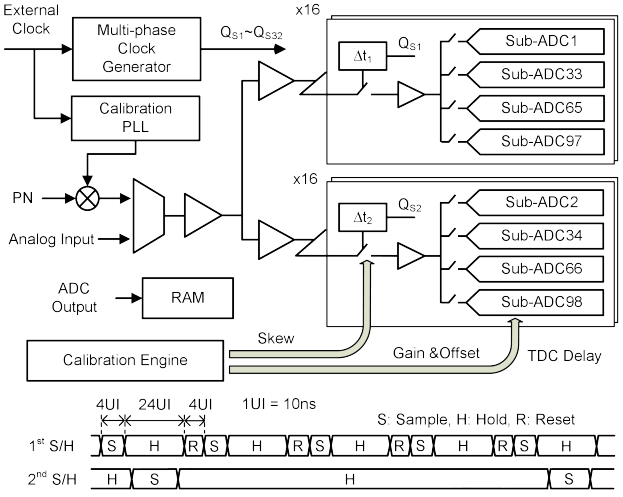

Fig. 1. 128-way time-interleaved ADC architecture, incorporating a two-stage hierarchical sampling network and an on-chip calibration.

is allocated 32 clock cycles: 4 for input sampling, 16 for data transfer to the second stage, 4 for reset, and 8 cycles reserved as skew margin. To mitigate inter-channel mismatches, an on-chip calibration engine corrects channel offset, gain, skew, and TDC delay variation in the analog domain. A dedicated PLL provides the reference clock for generating a pseudo-random (PN) training signal whose frequency is chosen to be relatively prime to the 32 samplers. Offset and gain errors are extracted from the flat regions of the PN waveform to avoid the interaction between amplitude- and time-domain calibration.

III. Frontend Circuit

To overcome the linearity limitations of cascaded source followers (SFs), a linearity-enhanced SF is introduced as the first-stage buffer (Fig. 2, top). Unlike [2], which enhances large-signal gain, the proposed design reduces small-signal gain by subtracting the output of a source-degenerated common-source (SD-CS) auxiliary path from the main SF path. This technique yields a slightly reduced yet stable output gain across the input voltage range. Consequently, the total

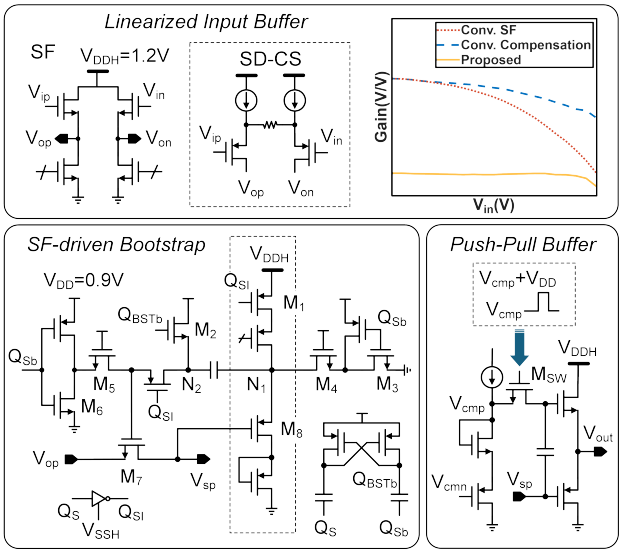

Fig. 2. Detailed schematics of the front-end circuits: Linearized input buffer; SF-driven bootstrapped sampler; Push-pull output buffer.

harmonic distortion (THD) is improved by more than 20 dB across PVT corners, achieving -70 dB THD at low frequencies with only a ∼0.2-dB gain loss and ∼8% power overhead.

Following the initial buffer stage, the signal is sampled by a bootstrapped switch (Fig. 2, bottom-left). Building upon the architecture in [3], this design relocates the bootstrap reference node to the output to decouple fan-out and bandwidth constraints. A local SF isolates the bootstrap capacitor. During the hold phase, M_3 discharges node N_1, M_2 ties N_2 to V_{DD}, and M_5 and M_6 ground the gate of the sampling switch (M_7). M_1 operates in weak inversion to ensure rapid SF turn-on. During the tracking phase, the SF boosts the gate of M_7 to $V_{DD} + V_{sp} + V_{GS(M8)}$, while M_4 and M_5 remain off. Device reliability is maintained by biasing M_1 at V_{SSH} (∼0.4 V).

After the sampling network, the final-stage SF (Fig. 2, bottom-right) is employed to drive the subsequent circuits efficiently. It adopts a push-pull structure to improve drivability and linearity at low power. The gate of the switch M_{SW} is boosted from V_{cmp}, a PVT-tracking bias, while V_{cmn} is set to the input common-mode voltage of the buffer.

IV. Proposed Sub-ADC Architecture

A. Hybrid Operation and Built-In Redundancy

To achieve high-resolution and power-efficient conversion, each sub-ADC channel (Fig. 3) integrates a reference buffer, a dual-mode comparator, a SAR logic, an 8-bit CDAC with redundancy, and an 8-bit DAC array for fine offset and gain calibration. A multiplexer (MUX) and a 2.5-bit Vernier TDC are embedded to realize the SAR–TDC hybrid architecture. During the final three LSB cycles, the MUX routes the comparator clock (CK_c) to the TDC by leveraging the comparator's VTC operation [4].

As shown in Fig. 4 (left), the architecture exploits the quasi-logarithmic relationship between the decision time and input voltage, which becomes pronounced when the input amplitude falls below a characteristic voltage V_0 of approximately 15 mV. In this region, the comparator behaves as a log-linear VTC, whose gain and linearity are both enhanced by operating the circuit in a low-speed but low-noise mode during these final cycles. Because each SAR cycle halves the comparator's input range, the same set of delay cells (T_{L1}–T_{L3}) can resolve the remaining time residue (Fig. 4, right), while T_{M1}–T_{M3} cells introduce time shifts corresponding to the previous cycle's LSB. The TDC delay step is set to one-quarter of each cycle's LSB, providing two extra bits and overflow/underflow detection. Consequently, the proposed hybrid architecture achieves an effective 11-bit resolution

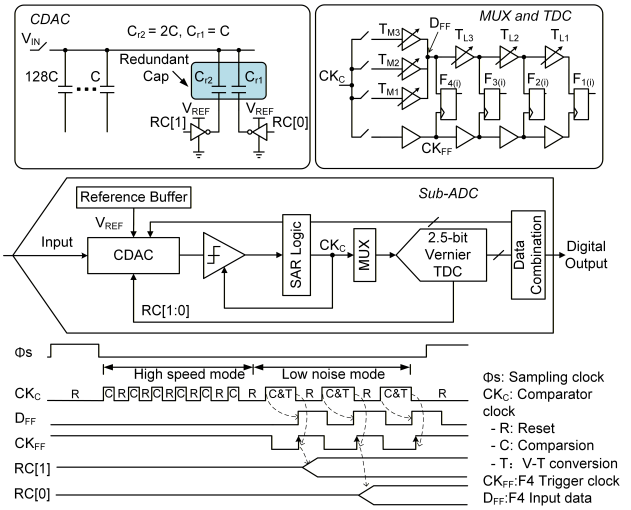

Fig. 3. Proposed single-channel sub-ADC: hybrid SAR-TDC architecture and its corresponding operation timing diagram.

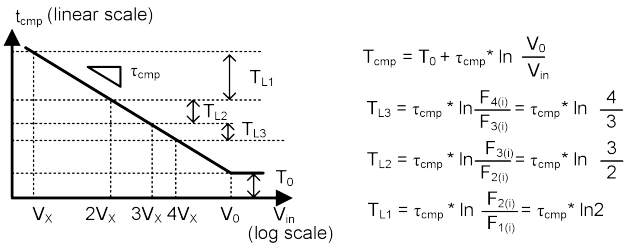

Fig. 4. Comparator-based VTC characteristics (left) and time residue resolution utilizing shared delay cells T_{L1}–T_{L3} (right).

SAR and TDC output weight

Cycle (i)	SAR	TDC			
		$F_{4(i)}$	$F_{3(i)}$	$F_{2(i)}$	$F_{1(i)}$
7	B_7:16	16	12	8	4
8	B_8:8	8	6	4	2
9	B_9:4	4	3	2	1

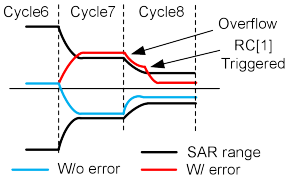

Fig. 5. Proposed redundancy scheme: (left) SAR and TDC output weight assignments; (right) operational mechanism demonstrating error recovery.

within only 9 conversion cycles, relaxing the critical timing constraints. The resulting weight assignments for the SAR and TDC outputs are illustrated in Fig. 5 (left).

Furthermore, a built-in redundancy scheme is employed to enhance the system's robustness. As shown in the timing sequence, during the 7^{th} and 8^{th} cycles, the TDC outputs ($\text{F}_{4(7)}$, $\text{F}_{4(8)}$) detect potential overflow or underflow events and generate control signals (RC[1:0]) to toggle the redundant capacitors (C_{r1}, C_{r2}). An operational example is provided in Fig. 5 (right): if an earlier comparison error causes a residue deviation, it is captured by $\text{F}_{4(7)}$, which triggers RC[1] to recover the signal. This mechanism corrects non-idealities such as incomplete settling, drift, and noise with minimal hardware cost. To maximize the effectiveness of this error recovery, an adaptive offset calibration is implemented via a current-injection technique. By proportionally scaling the calibration current to track the larger tail current in the high-speed mode, it actively suppresses the mode-dependent offset mismatch between the high-speed and low-noise operations. Consequently, the built-in redundancy range is effectively maintained.

B. Redundancy-Assisted TDC Calibration

Time-domain conversion is sensitive to PVT variations and requires calibration. Unlike prior TDCs relying on PVT tracking or matching circuits [5], [6], the proposed calibration algorithm leverages the inherent redundancy between the SAR and TDC bits (Fig. 5, left). The procedure (Fig. 6) is performed with redundant capacitors C_{r1} and C_{r2} disabled. Initially, T_{M3} is tuned until $\text{F}_{4(7)}$ is aligned with B_8 (half of the normal weight). Next, T_{L3} is adjusted until $\text{F}_{2(7)}$ matches B_9, followed by a readjustment of T_{M3} to equate $\text{F}_{2(7)}$ with B_8 (returning T_{M3} to the normal delay). This alignment allows $\text{F}_{4(7)}$ to correspond to B_7; combined with the comparator output, this enables overflow or underflow detection. With this reference established, TDC delays T_{L1}–T_{L3} are then identified by comparing B_8 and B_9 against the TDC outputs. For example, the TDC output at the 7^{th} SAR cycle, $\text{F}_{3(7)}$, should equal $\text{B}_8 + \text{B}_9$, which identifies T_{L3}. Likewise, T_{L2} is determined by comparing $\text{F}_{2(7)}$ with B_8, and T_{L1} by comparing $\text{F}_{1(7)}$ with B_9. Finally, T_{M2} and T_{M1} are updated by comparing B_9 with $\text{F}_{2(8)}$, and $\text{F}_{1(8)}$ with $\text{F}_{2(9)}$, respectively.

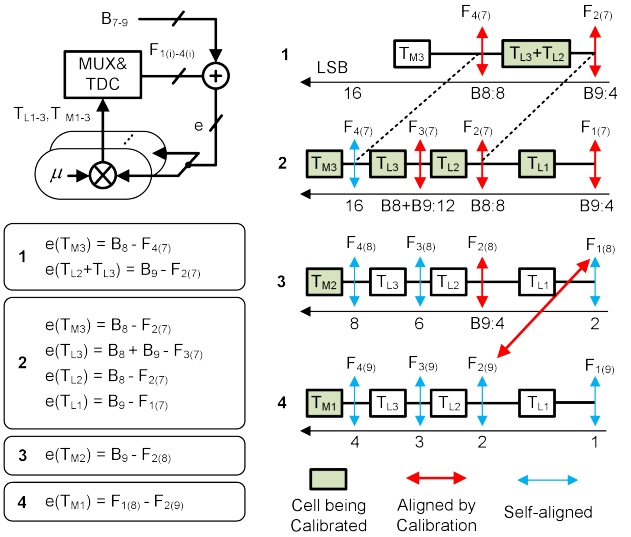

Fig. 6. Flowchart and principle of the redundancy-assisted TDC delay calibration.

V. Measurement Results

Fabricated in a 7-nm FinFET process, the ADC occupies 0.36 mm^2 and consumes 495 mW from 0.8/1.2-V supplies (Fig. 7). Fig. 8 demonstrates the efficiency of the on-chip calibration in correcting offset, gain, skew, and TDC delay. To address residual bandwidth mismatch at high frequencies, a 7-tap off-chip digital FIR filter (three linear and four nonlinear) is applied. As shown in the 11.95-GHz spectra, this filter further improves SNDR and SFDR by 2.9 dB and 8.5 dB, respectively.

Although front-end circuitry dominates the noise budget (>50%) in such a high-speed design, the TDC still yields a 3-dB SNDR improvement at low frequencies. Under these same input conditions, compared to a 70-GS/s baseline where the comparator operates entirely in low-speed mode, the nominal 100-GS/s operation (utilizing both high- and low-speed modes) degrades the measured SNDR by less than 0.2 dB. This negligible difference validates that the proposed TDC-based redundancy scheme effectively absorbs dynamic non-idealities such as incomplete settling, drift, and noise.

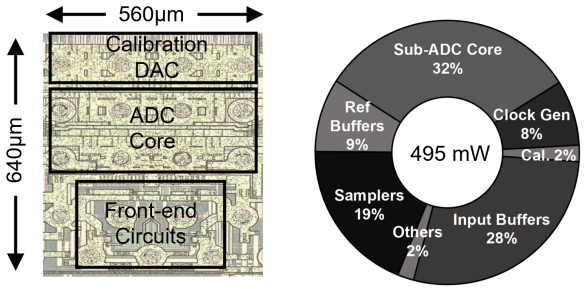

Fig. 7. Die micrograph and power breakdown.

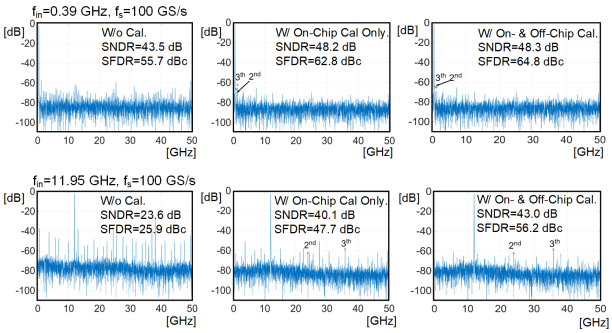

Fig. 8. Measured ADC output spectra, comparing performance before calibration, after on-chip calibration, and after on-chip & off-chip calibration.

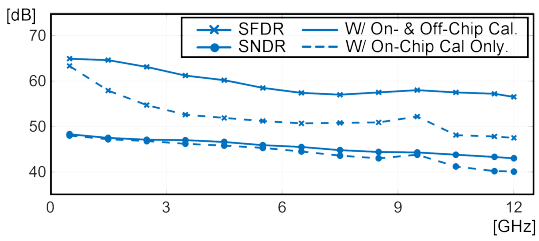

Fig. 9. Measured ADC output SNDR/SFDR versus input frequencies at 100 GS/s (comparing on-chip vs. on-chip & off-chip calibration).

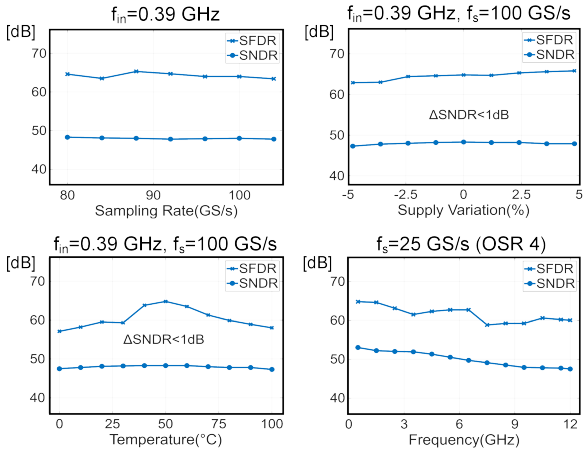

Fig. 10. Measured SNDR/SFDR versus sampling rate, voltage, temperature, and input frequencies at 25 GS/s (one-time calibration).

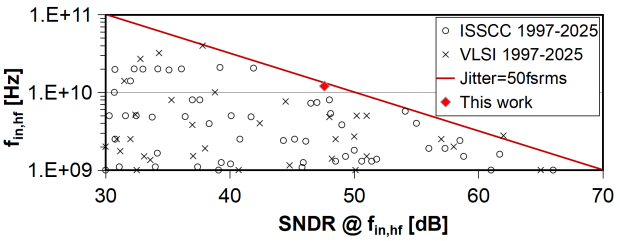

Fig. 11. Performance comparison with state-of-the-art ADCs ($f_{in} > 1$ GHz).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	This work		C. -E. Hsieh ISSCC'25 [7]	J. Liu VLSI'2024 [8]	S. S. Kumar ISSCC'23 [9]	J. Shen ISSCC'25 [10]
Architecture	TI-SAR-TDC		TI-Pipe-SAR	TI-TD	TI-SAR	TI-SAR
Process (nm)	7		4	4	7	16
Area (mm^2)	0.36		0.43	0.008	0.9	0.25
f_s (GS/s)	100	25	16	16	24	12
Number of Channels	128		16	4	80	16
Supply (V)	1.2/0.8		1.35/0.85	0.9/0.75	1.8/0.9	1.8/0.8
Resolution (bits)	11	12	12	10	12	9
Power (mW)	495		570	94.2	750	175
f_{in} (GHz)	**11.95**		7.4	7.6	7.2	5.3
SFDR @ f_{low} (dB)	65	65	67	57	/	60[a]
SNDR @ f_{low} (dB)	48.3	53.3	54	45.3	/	49[a]
SFDR @ f_{in} (dB)	56	60	58	56	76	61
SNDR @ f_{in} (dB)	43	47.5	47	44.5	46.5	48.1
NSD (dBFS/Hz)	**-150**	**-148.5**	-146.1	-143.5	-147.3	-145.9
FoM$_S$ @ f_{low} (dB)	**158**	**157.3**	155.5	154.8	/	154.5
FoM$_S$ @ f_{in} (dB)	153	151.5	148.5	153.8	148.5	153.5

[a]Value estimated from figure.

The overall measured SNDR and SFDR versus input frequency are plotted in Fig. 9. Performance remains stable across voltage and temperature variations (Fig. 10). With 4× oversampling (25-GS/s output), the final SNDR at 11.95 GHz improves to 47.5 dB, corresponding to an effective clock jitter of <56 fs, a Schreier FoM$_s$ of 151.5 dB, and a Noise Spectral Density (NSD) of -148.5 dBFS/Hz. At low frequency, the peak FoM$_s$ reaches 157.3 dB. As shown in Fig. 11 and Table I, the ADC achieves state-of-the-art performance [7]–[11].

VI. CONCLUSION

This paper presented a 25-GS/s TI ADC fabricated in a 7-nm FinFET process. By leveraging the comparator as VTC, a 2.5-bit TDC is seamlessly embedded to extend the 9-bit SAR to an effective 11-bit resolution. Furthermore, a built-in redundancy scheme tolerates incomplete settling and decision errors with minimal hardware overhead. Aided by an off-chip FIR filter for high-frequency bandwidth mismatch calibration and oversampling for clock jitter suppression, the prototype achieves a peak Schreier FoM$_s$ of 157.3 dB and maintains 151.5 dB at an 11.95-GHz input. The measured results objectively demonstrate the proposed architecture's viability in achieving state-of-the-art power efficiency and dynamic performance for ultra-high-speed applications.

REFERENCES

[1] H. Park *et al.*, "A 4.63pJ/b 112Gb/s DSP-based PAM-4 transceiver for a large-scale switch in 5nm FinFET," in *IEEE International Solid-State Circuits Conference (ISSCC)*, 2023, pp. 5–7.

[2] Y. Cao, M. Zhang, Y. Zhu, R. P. Martins, and C.-H. Chan, "A 12GS/s 12b 4× time-interleaved pipelined ADC with comprehensive calibration of TI errors and linearized input buffer," in *IEEE International Solid-State Circuits Conference (ISSCC)*, 2024, pp. 388–390.

[3] A. S. Yonar *et al.*, "An 8-bit 56GS/s 64× time-interleaved ADC with bootstrapped sampler and class-AB buffer in 4nm CMOS," in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2022, pp. 168–169.

[4] B. Xu, Y. Zhou, and Y. Chiu, "A 23-mW 24-GS/s 6-bit voltage-time hybrid time-interleaved ADC in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1091–1100, April 2017.

[5] Y. Cao, M. Zhang, Y. Zhu, C.-H. Chan, and R. P. Martins, "A single-channel 12b 2GS/s PVT-robust pipelined ADC with critically damped ring amplifier and time-domain quantizer," in *IEEE International Solid-State Circuits Conference (ISSCC)*, 2023, pp. 9–11.

[6] J. Hao *et al.*, "A single-channel 2.6GS/s 10b dynamic pipelined ADC with time-assisted residue generation scheme achieving intrinsic PVT robustness," in *IEEE International Solid-State Circuits Conference (ISSCC)*, 2023, pp. 168–170.

[7] C.-E. Hsieh *et al.*, "A power- and area-efficient 4nm self-calibrated 12b/16GS/s hierarchical time-interleaving ADC," in *IEEE International Solid-State Circuits Conference (ISSCC)*, 2025, pp. 438–440.

[8] J. Liu, A. Shabra, S. Ho, G. Manganaro, and M. S.-W. Chen, "A 16GS/s 10b time-domain ADC using pipelined-SAR TDC with delay variability compensation and background calibration achieving 153.8dB FoM in 4nm CMOS," in *IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2024, pp. 1–2.

[9] S. S. Kumar *et al.*, "A 750mW 24GS/s 12b time-interleaved ADC for direct RF sampling in modern wireless systems," in *IEEE International Solid-State Circuits Conference (ISSCC)*, 2023, pp. 1–3.

[10] J. Shen *et al.*, "A 12GS/s 9b 16× time-interleaved SAR ADC in 16nm FinFET," in *IEEE International Solid-State Circuits Conference (ISSCC)*, 2025, pp. 442–444.

[11] B. Murmann, "ADC performance survey 1997-2024," [Online]. Available: https://github.com/bmurmann/ADC-survey.