An FR2 Transmitter for Configurable Asymmetric Phased Arrays

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***Abstract*—Phased array transmitters for mmW frequencies typically rely on symmetric feed networks. Such corporate-fed arrays are practical for fixed sub-array based antenna configurations through one or many RF-to-baseband paths with limited array scalability. This paper proposes a transmitter IC that enables re-configurable antenna panel usage, providing flexibility to combine multiple antenna elements or sub-arrays using mmW chip-to-chip interconnects routed asymmetrically across a large antenna panel. The proposed FR2 sliding-IF transmitter tested at 26 GHz range connects multiple chips together through two two-way mmW busses and one two-way IF bus across the panel. A dual-polarized 64-element phased array, using 16 ICs and four I/Q baseband inputs, has been demonstrated in a chip-on-board setup with an EIRP of 47.0 dBm using a 1.57 V power amplifier supply. Also, modulated measurements using 5G NR signal are performed.**

***Index Terms*—Asymmetrical routing, chip-on-board, irregular antenna array, mmW interconnect, phase shifters, power amplifiers, transmitter, phased array, RFIC.**

I. Introduction

Phased arrays are extensively adopted in broadband mmW communications e.g. 5G to enable long-range radio links. A typical mmW base station radio has 64 antennas or more. To avoid excessive power consumption in digital processing and conversion, analog sub-arrays with steerable beams are deployed. Such phased arrays typically have a symmetric (corporate) feed network to half-wavelength–spaced antennas, like in [1], [2]. For optimized use of silicon and to minimize routing from RF front end chips to antennas, mmW chips are typically fed symmetrically forming sub-arrays from a limited number of digital data streams to enable hybrid multi-beam processing [3].

Corporate-fed arrays offer several advantages due to symmetric routing, including a lower sensitivity to beam squint which helps to maintain beamforming performance over a wide bandwidth. However, maintaining a symmetric structure limits the flexibility for element sharing and panel reconfiguration. Various approaches have been proposed to improve flexibility in antenna configuration, enabling the synthesis of various beam patterns with and without dedicated amplitude and phase control per antenna by exploiting sub-array irregularities [4], [5]. Until now, different RF and hybrid multi-beam architectures have not allowed for highly flexible selection of antenna elements in large-scale arrays [6], [7]. Nevertheless, recent works, e.g., in satellite communications, continue to rely on classical corporate-fed architectures [8], [9].

Despite the drawbacks of irregular feeding networks, they can achieve decent broadband performance over wide steering angles when the sub-arrays are properly dimensioned [10]. Furthermore, asymmetry can be exploited to provide flexibility in antenna configurations across multiple chips using chip-to-chip (C2C) interconnects at the carrier frequency or any intermediate frequency supported by the architecture.

This paper describes an FR2 transmitter (TX) that can be configured on an antenna-by-antenna basis to operate in different sub-array shapes of the phased array, using dedicated mmW and IF interfaces between the chips. The transceiver (TRx) IC, which includes a time division duplex (TDD) switch, also provides receiver (RX) functionality as discussed in the companion article [11]. To the best of authors knowledge the work demonstrates, for the first time, the concept of irregular feeding networks with C2C interfaces as part of a 64-element phased array using 16 TRx IC's.

Section II describes the transmitter and array architecture, and Section III the transmitter circuits. Section IV presents the experimental results, and Section V concludes the work.

II. Transceiver IC and Array Architecture

The TRx IC, shown in Fig. 1(a) provides eight RF front ends (FE) with TDD antenna switch and phase shifters that are connected to two signal splitting/combining networks to support dual-polarized antennas. The details of the chip architecture are discussed in [4] without TX circuits or antenna array implementation. In the TX, baseband (BB) I/Q signals are converted using sliding-IF architecture to carrier frequency with double-balanced mixers. The signal can be simultaneously routed to other ICs using dedicated C2C interconnects at carrier frequency (mmW bus) or at intermediate frequency (IF bus). Each four-antenna RF sub-array can be fed from either the same chip or from adjacent chips vertically using an IF bus, or horizontally using a bi-directional mmW bus to form an asymmetric feeding network as shown in Fig. 1(b).

The phased array to evaluate the concept has been constructed from 16 RFICs feeding a 64-antenna dual-polarized antenna array. Two mmW busses are routed, as in Fig. 1(b), for each row of the panel. For practical PCB routing reasons, only a single one-directional IF bus has been routed between chips, either from top-to-bottom or vise versa, depending on the column. Therefore, signal routing can combine all chips together as a single antenna panel, but the IF bus limits the

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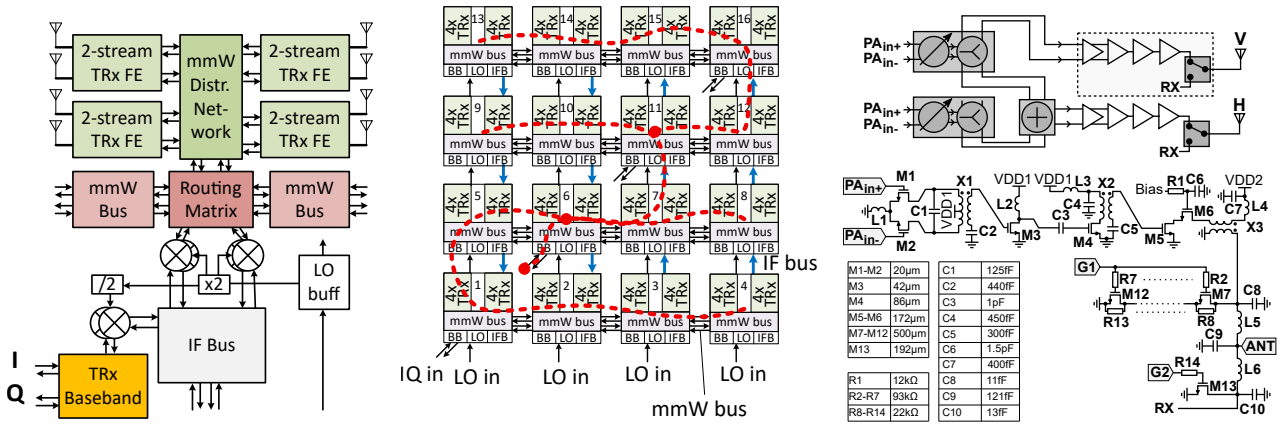


(a) (b) (c)

Fig. 1: (a) Transceiver IC, (b) 16-chip reconfigurable transceiver array; each chip is connected to four dual-polarized antennas; the dashed red lines illustrate the panel test setup for the complete array, showing the baseband starting point, row-wise signal propagation across ICs, and the transition to the next column, and (c) TX front end with power amplifier and TDD switch.

connectivity on the test platform. Similarly, for PCB routing reasons, only one BB I/Q input per row has been connected to the test platform diagonally from the bottom left corner. The differential LO signal is daisy-chained bottom-to-top over the chips from a commercial synthesizer. Only a selected number of possible signal path and antenna array configurations, out of tens or hundreds of options, have been shown in this article demonstrating the operational principles related to broadband signals. Compared with early proposals of on-chip, fully RF connected hybrid beamforming [6], this work shows reconfigurable connectivity between antenna elements in large antenna arrays.

III. Transmitter Circuits

A. mmW Front End

The TX front end consists of two vector modulator type phase shifters with 5-bit control per constellation dimension, antenna selector, four stage power amplifier, and TDD switch as shown in Fig. 1(c). Each TX FE branch can feed one dual-polarized patch antenna element (4.5 dBi antenna gain per polarization) that are connected through the PCB on the other side of the test board.

The first stage of the power amplifier (PA) converts the differential input to single-ended. Two single-ended pre-drivers with 1 V supply (VDD1) are driving the transformer matched output stage with dedicated supply (VDD2). The output stage consists of a series of two transistors that can be configured to operate as a cascode (with 1 V supply) or a two-stack topology by increasing the supply up to 1.5-2 V. In the measurements, intermediate setting of 1.57 V is used. In TX mode, the TDD switch is configured by setting G1 at 0 V and G2 at 1 V. The antenna switch is a single-pole-double-throw switch implemented with lumped element quarter-wave transmission lines having simulated loss of 1.3 dB. Transistor stacking was used in the PA side shunt switch to increase the switch power handling capability.

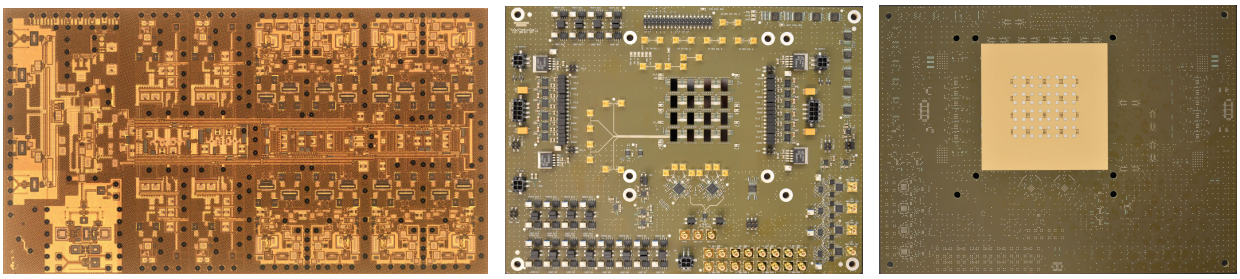
B. Chip-to-chip and on-chip interfaces

The asymmetric signal routing between the chips at carrier frequency is implemented with two differential bi-directional mmW busses that can bypass the front-ends or connect antennas to them as in Figs. 1(a) and (b) [4]. They can also loop-back the signal at the interface for testing purposes. Each bus has differential amplifiers for buffering and similar phase shifters as in the front-ends for the possibility to tune the phase of the whole sub-array before feeding the next chip. The bus has gain control such that it can provide unity gain between chips taking into account on-chip and off-chip routing, interface, and switching losses. The IF bus operates similarly without the option for phase control. Each chip has input and output buffering for the LO daisy-chaining using a differential common-source stage with inductor load and capacitive neutralization. The LO signal, in div/3 ratio to the carrier, is first doubled on the chip for the mmW mixer and then divided-by-two to provide LO to the I/Q mixers.

In the IF and mmW bus as well as in the mmW routing and distribution networks, differential active splitters and combiners are used for signal distribution. In active splitters and combiners, g_m stages are used to convert the input voltage to current, and the current signals are routed via differential co-planar lines to distant locations inside the chip. In active splitters, the voltage signal is inserted to the gates of up to four closely spaced g_m stages. Inductive load is used to resonate the transmission line capacitance and is tuned with additional tuning capacitors to provide gain at the desired frequency to compensate the transmission line loss. A folded cascode type stage is used to terminate and buffer the signal to the next stage in the signal chain. In active combiners, signals are combined in the current domain, close to the common inductive load.

C. I/Q Inputs and Sliding IF Upconversion

Double balanced passive up-conversion mixers are used at the BB inputs to up-convert the signals to the IF. The IF mixers



(a) (b) (c)

Fig. 2: Photographs of (a) designed RFIC, (b) PCB from the component side with 16 RFICs, and (c) PCB from the antenna array side.

have transformer loads and their frequency response can be fine-tuned by three switchable capacitors on both sides of the transformer. Ladder resistor DC level shifting is implemented for the LO inputs to mitigate LO feedthrough. The IF signals can be either combined with IF signals from other ICs or routed directly to mmW mixers. Double balanced Gilbert cell mixers are used to up-convert the IF signal to mmW frequency.

A push-push injection-locked doubler is used to multiply the LO signal for the IF to mmW mixers. A current-mode logic divider provides the LO for the BB to IF mixers.

IV. Experimental Results

The IC has been implemented using 45 nm PD-SOI CMOS by GlobalFoundries. The chip area is 35.2 mm^2 and the micrograph is shown in Fig. 2(a). The IC is tested in a 16-chip configuration with 64 dual-polarized antennas [12]. The ICs are flip-chipped directly on a 16-layer PCB (Megtron7 by Panasonic) using SnAg bumps. Each row of the panel has one I/Q BB input to feed the array to support several beams generation. In this paper, only one input at a time is used, and all measurements have been performed in over-the-air (OTA).

PCB is shown from both sides in Figs. 2(b) and (c), respectively. ICs, other components and connectors in 16-metal layer board are on the other side of the antenna elements. Differential LO and IF signals are routed vertically in the mid-layer of the PCB and differential mmW signals are routed horizontally on the top layer. PCB includes two frequency synthesizers (LMX2594) with two differential outputs. Each synthesizer is driving LO for two daisy chained columns of the array, and the two synthesizers can be phase synchronized.

Each TX path was tested with a moderate 1.57 V PA supply in two-stack mode. The saturated output power of 2x64 PAs with switch is on average 9.1 dBm with σ of 1.3 dB at 26.5 GHz. The external LO of the sliding IF TX was 1/3rd of the carrier. Phase calibration of the array elements was performed for the irregular feeding network first for all rows and then between the rows. The saturated EIRPs of the single-polarized array are shown in Fig. 3(a) with three power control settings (maximum, 9 dBm, and 5 dBm Psat of each PA). The test uses irregular routing with IQ input from the chip 6 as shown in Fig. 1(b) with dashed red line. The EIRP of the array using irregular feeding network is close to what is expected from individual PA measurements. Beam patterns were measured at -30°, 0°, and +30° steering angles in Fig. 3(b). The results of two simultaneous beams towards (-15° and +30°) using the same feed are obtained by using two IC rows for one direction and two for the other in Fig. 3(c) validating that irregular feed networks can support multiple simultaneous beams.

Finally, a 400-MHz 5G NR OFDM waveform using 4×100-MHz component carriers (CCs) was transmitted with a low side LO injection to demonstrate the impact of irregular feeding on signal quality. An exemplary EVM constellation is presented in Fig. 4(a) by measuring through four chips in the same row and feeding the signal from chip 1. The EVM vs. EIRP for all CCs in three steering angles is shown in Fig. 4(b). The EVM results for all CCs are in close proximity for the lowest steering angles. However, the highest (+45°) steering angle (the red curves) showed a slight deterioration with a minor indication of beam squint.

The TX consumes in 64-antenna single-polarized configuration 260 mW per antenna and the performance is compared with the state-of-the-art in Fig. 4(c). It should be noted that this is to the authors' knowledge the first experimental demonstration of this scale on irregularly fed arrays for 5G.

V. Conclusion

A reconfigurable transmitter capable of constructing irregularly shaped phased arrays has been demonstrated. The chip adopts mmW and IF C2C interfaces to enable flexible routing in asymmetric manner for multiple ICs. The proposed architecture enables various kinds of hybrid beamforming schemes, but demonstrates that the routing area needed for a very large number of C2C interconnections is not feasible for fully connected hybrid beamforming at RF for large arrays as proposed in the theoretical literature [13].

The concept is demonstrated using a 16-chip platform that supports 64 dual-polarized antennas. As predicted by theory, the measured results show a reasonable bandwidth reduction due to asymmetric routing even in large steering angles in setups up to 8×8 two-dimensional panel. The test setup provides 47.0 dBm EIRP and consumes 260 mW per antenna. The experimental results prove the operational principle of the reconfigurable irregular array with minor degradation due to beam squint in EVM for the large steering angles.

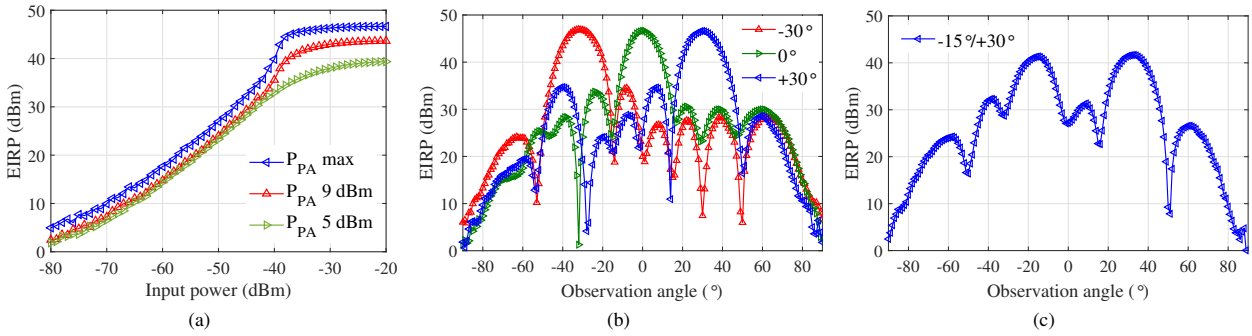
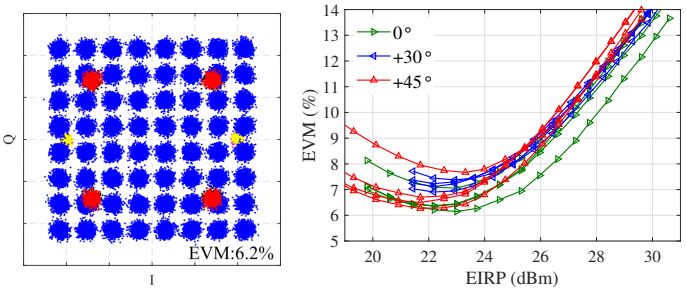


Fig. 3: OTA measurement results of (a) Single-polarized full array compression for three different power control settings with different Psat, (b) Full array radiation pattern in different steering angles and (c) Radiation pattern with lower half of the array pointing to -15° and upper half to +30° angle.



	This work	[1]	[7]	[8]	[9]
Technology	45 CMOS SOI	180 BiCMOS	65 CMOS	65 CMOS	65 CMOS
Frequency (GHz)	25.5-27.5	16.0-52.0	39.0	27.5-31.5	18.0-20.0
EIRP (dBm)	47.0	50.0	53.0	54.0	64.6
Feed-achitecure	Irregular	Corporate	Corporate	Corporate	Corporate
Pdc per path (mW)	260^	250	375	n/a	68
PA Psat (dBm)	9.1	15.0	15.5	19.2	12.0
# of antennas per polarization	64	64	64	64	256
Polarization	dual-pol, linear	single-pol, linear	single-pol, linear	dual-pol, circular	dual-pol, circular
Beam steering (°)	45	60/30	40	45/60	66
Number of beams	4	1	1	4	1

^including all IF and mmW chip-to-chip routings

(c)

Fig. 4: OTA measurement results of one IC row i.e. 16 antennas with 4CC 5G NR signal: (a) 64-QAM constellation diagram for CC0 @0°, (b) The average EVM measured for all CCs and different steering directions using one IC row as a function of combined component carriers' EIRP from 16 PAs, and (c) comparison to state-of-the-art.

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