A 240Gb/s D-Band Modulator-Last Transmitter with Quadrature Correction in 28nm CMOS

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***Abstract*—This paper presents a D-band transmitter optimized for high-capacity short-range communication and die-to-die interconnects. A low-loss high-linearity passive IQ modulator is designed to realize direct conversion with adequate output power. By shifting the power amplification to the LO path, this transmitter design employs a modulator-last architecture to achieve an optimal balance between gain, efficiency, and bandwidth performances. An injection-locking-based quadrature correction scheme is implemented to mitigate IQ phase imbalances. Fabricated in 28-nm CMOS, the transmitter achieves a record 240Gb/s data rate under 16QAM modulation with an energy efficiency of 0.52pJ/bit. These results demonstrate a scalable, highly efficient solution for next-generation short-range wireless communication and die-to-die interconnects.**

Keywords—D-band, transmitter, modulator-last.

I. Introduction

The rapid evolution of high-performance computing and 6G systems has catalyzed a global research shift toward the D-band (110–170GHz). This spectrum can provide vast contiguous bandwidth necessary for throughput exceeding 100Gb/s, serving as a transformative solution for short-range communication and die-to-die (D2D) interconnects. Such applications facilitate next-generation integrated systems by providing a scalable, high-capacity path for data transfer.

However, realizing D-band transmitters in standard CMOS technology remains a formidable challenge due to the rigid trade-offs between output power, bandwidth, and linearity. While state-of-the-art designs have surpassed 100Gb/s [1-5], achieving high energy efficiency while maintaining low EVM required for high-order modulation remains a major hurdle. At sub-THz frequencies, the limited power gain and linearity performances of silicon-based PAs severely restrict the maximum achievable data rate and degrade overall power efficiency.

This paper presents a D-band transmitter specifically optimized for short-range and D2D applications where output power requirements are inherently relaxed. Under these conditions, a modulator-last architecture is proposed to bypass traditional RF PA bottlenecks to achieve superior bandwidth and efficiency while realizing adequate output power. To ensure signal integrity, an injection-locking-based quadrature correction scheme mitigates quadrature phase imbalances. Fabricated in 28nm CMOS, the transmitter achieves a record 240Gb/s data rate with an energy efficiency of 0.52pJ/bit, which is the highest among all mm-wave or D-band transmitters reported to our best knowledge.

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II. The Modulator-Last Transmitter Architecture

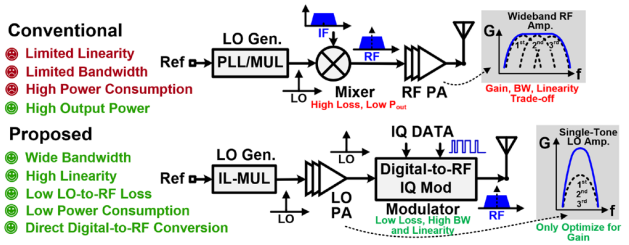

Fig. 1. Comparison between the conventional and proposed TX architecture.

As illustrated in Fig. 1, conventional D-band transmitters are typically based on mixers, which presents significant conversion loss and limits the output power to <-10dBm. Consequently, multi-stage power amplifiers (PAs) are required to achieve the ~0dBm level of transmitted power necessary for practical applications. Moreover, to meet the ultrawide bandwidth requirements, these PAs have to employ the staggered-tuning scheme to achieve a flat frequency response by intentionally offsetting the resonant frequencies of successive amplifier stages. Consequently, these PA-heavy designs suffer from severe trade-offs between gain, bandwidth, as well as linearity and power consumption. Especially at D-band frequencies, the limited power gain of the silicon transistors makes maintaining simultaneous amplitude flatness, constant group delay and high linear output power extremely difficult, ultimately restricting the achievable data rate and energy efficiency.

To address these limitations, this work proposes the modulator-last architecture shown in Fig. 1. Central to this architecture is a high-linearity direct-conversion modulator with low modulation loss, enabling ultrahigh data rates with adequate output power and superior EVM, which are critical for reliable communication links. In this architecture, power amplifications are then shifted to the LO signal path preceding the modulator, which allows the amplifiers to operate on a single-tone signal. This significantly relaxes the bandwidth and linearity requirements of these amplifiers, allowing them to be optimized primarily for maximum gain and power efficiency.

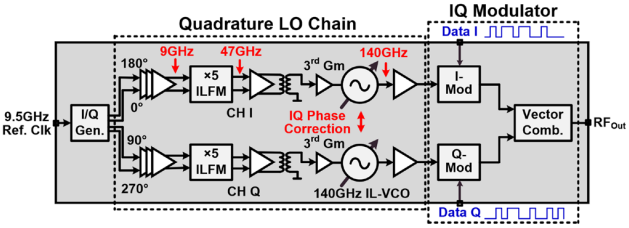

Fig. 2. Details of the proposed D-band modulator-last transmitter.

The proposed transmitter in Fig. 2 comprises a quadrature LO chain and a passive IQ modulator. The LO chain

generates initial quadrature phases at 9.5GHz, followed by 15x frequency multiplication via a 5th-order ILFM and a 140GHz IL-VCO. To maintain quadrature accuracy, an injection-locking based phase tuning scheme is implemented at the 140GHz stages to compensate for the phase imbalances. Finally, the passive IQ modulator employs a direct-conversion architecture, where a vector combiner sums I/Q components in the electric field domain to enable high-speed quadrature modulation, which achieves low modulation loss and high linearity.

III. Detailed Circuit Implementation

A. The Low-Loss High-Linearity Passive IQ Modulator

The modulation circuit is a critical component in high-performance transmitters, directly dictating the attainable bandwidth and constellation accuracy. This work proposes a low-loss, high-linearity passive IQ modulator.

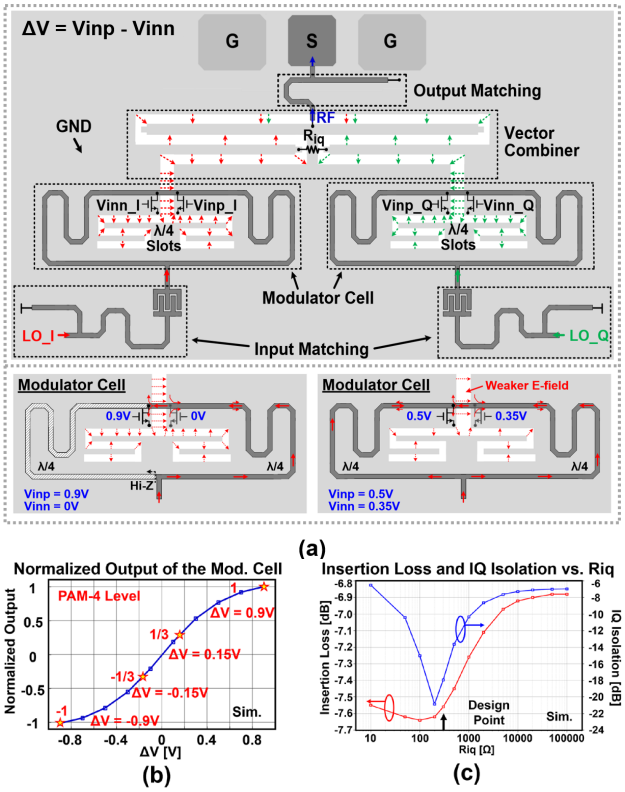

Fig. 3. (a) The proposed passive IQ modulator structure, (b) the simulated normalized output, (c) insertion loss and isolation behaviors.

As illustrated in Fig. 3(a), each modulator employs a transmission-line (TL) to slot-line conversion structure [6]. Differential I/Q data is applied directly to the gates of the NMOS switches, forming a direct-conversion topology. By adjusting the differential input levels (V_{inp}/V_{inn}=0.45V±ΔV/2), the electric fields within the slot structure are precisely controlled to achieve high-quality PAM-4 modulation within each cell, as shown in Fig. 3(b). Subsequently, a slot-to-TL mode vector combiner sums the I and Q components in the electric field domain to generate a 16QAM signal at the RF output. Compared to Wilkinson power combiners, the proposed vector combiner theoretically avoids the 3dB combining loss, but at the expense of degraded IQ isolation. To balance this isolation against modulation loss, a resistor (R_{iq}) is inserted across the I and Q slots. As shown in Fig. 3(c), the optimal value for R_{iq} is 300Ω, allowing the modulator to achieve an IQ isolation of -18dB with an insertion loss of -7.5dB.

Linearity of the passive IQ modulator was characterized through simulation. Fig 4(a) depicts the output power versus LO input at the selected differential input levels, revealing an excellent P_{sat} of 2.7dBm.

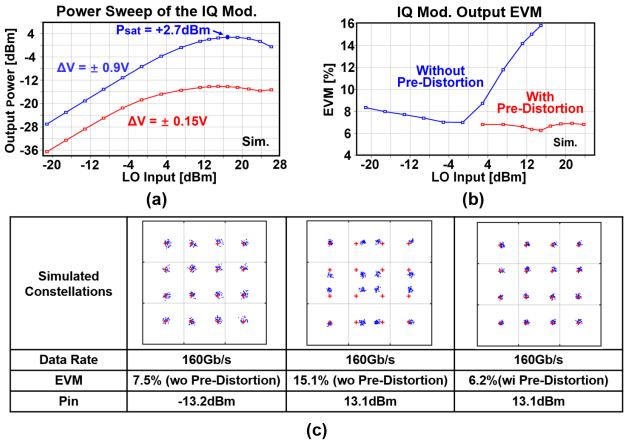

Fig. 4. The simulated linearity of the passive IQ modulator: (a) output power sweep, (b) 16QAM output EVM and (c) constellations wo/wi pre-distortion.

Due to different saturation trends for different points in the 16QAM constellation, the simulated EVM degrades when LO input power exceeds 0dBm. The application of appropriate input pre-distortion maintains superior EVM performance up to P_{sat}. The effectiveness of this approach is validated in Fig. 4(b) and (c), which illustrate the simulated constellations and EVM both with and without pre-distortion at a data rate of 160Gb/s. These simulations confirm its capability for high-speed and high-quality modulation with high output power.

B. Quadrature LO Multiplier Chain

High-speed wireless coherent systems demand a high-quality LO signal characterized by low phase noise and robust harmonic rejection. Compared to sub-sampling PLL based LO chain scheme in D-band [7-8], injection-locking multiplier chains offer significantly reduced in-band spurs. This design implements a quadrature 15x multiplier chain.

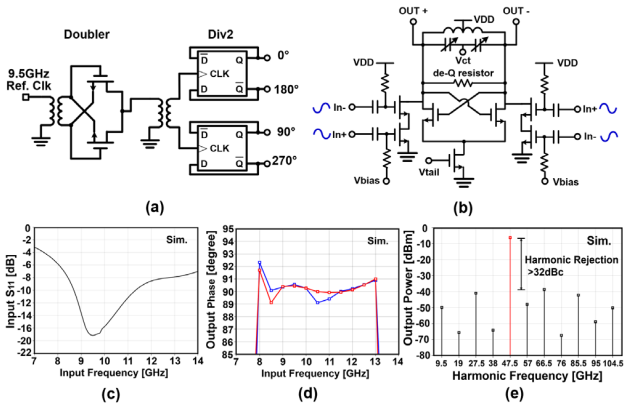

Fig. 5. Schematic of (a) IQ generation block and (b) 5x ILFM circuitry. Simulated (c) input matching and (d) operation frequency of the IQ generation block. (e) Harmonic rejection performance of the 5x ILFM .

Quadrature phase generation is performed at 9.5 GHz using a frequency doubler followed by two CML DFF-based

dividers. A 3-stage buffer then distributes and shapes the 9.5GHz LO for richer harmonic components. The subsequent 5th-order ILFM utilizes a current-chopper-based LC VCO structure [9], incorporating a de-Q resistor within the LC tank to extend the locking range. By optimizing the chopper bias, the ILFM generates the desired 5th harmonic while suppressing unwanted harmonics. Simulations show that the harmonic rejection ratio exceeds 32dBc, ensuring the high spectral purity necessary for the LO signal.

C. *The 140GHz IL-VCO with Phase Calibration Scheme*

As shown in Fig. 6, the 140GHz IL-VCO utilizes a Return-Path-Gap-Coupler (RPGC) structure to maximize output power and efficiency [10]. An NMOS transistor biased in the sub-threshold region serves as a 3rd harmonic Gm cell, achieving the 3rd-harmonic injection-locking.

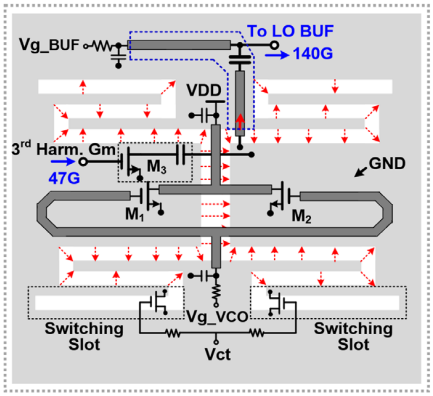

Fig. 6. The 140G IL-VCO schematic.

To mitigate IQ phase imbalances arising from PVT variations or layout parasitic, an injection-locking-based quadrature correction scheme is employed. In the injection-locked state, the relative LO phase can be shifted by varying the free-running frequencies of the I and Q IL-VCOs, which can be utilized for quadrature phase correction [11].

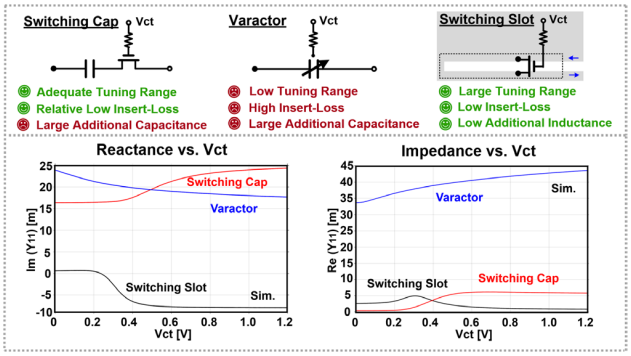

Fig. 7. Frequency Tuning Components comparison.

While various tuning elements, such as switching-cap or varactors, can be integrated into the RPGC structure, this design adopts a switching-slot architecture. Compared to alternative tuning methods, the switching-slot provides a sufficient tuning range with minimal insertion loss and parasitic reactance, as shown in Fig. 7.

IV. Measurement Results

The transmitter prototype is fabricated using a 28-nm CMOS process. As depicted in Fig. 8, the transmitter occupies a die area of 1.13mm², and a core area of 0.55mm².

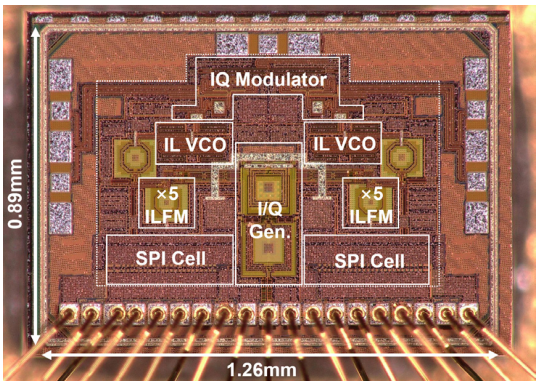

Fig. 8. Photograph of the D-band transmitter chip.

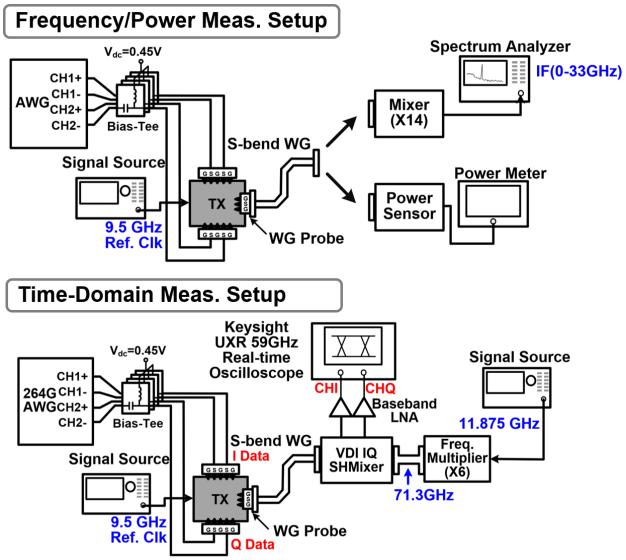

Fig. 9. The Frequency, power and time-domain measurement setups.

The measurement setups are shown in Fig. 9. The external 9.5GHz reference is provided by a signal source. IQ input data is generated by a 2-channel AWG via Bias-Tees. The RF signal is captured through a D-band waveguide (WG) probe with an S-bend WG.

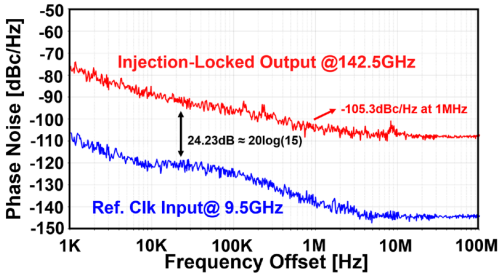

Fig. 10. The phase noise measurements.

In the frequency measurement, a spectrum analyzer with a frequency extender is utilized to analyze the output signal. The phase noise measurement results are plotted in Fig. 10. At the 9.5GHz reference input, an LO signal at 142.5GHz with ~24dB worse phase noise is obtained, which matches with the injection locking theory well, demonstrating that the harmonic injection-locking LO chain works properly. In the power measurement, a power meter with a D-band sensor head is utilized to capture the RF output power. The transmitter demonstrates an output power of -5.2dBm with a

total DC power consumption of 135.4mW. Table I summarizes the block-level power consumption.

TABLE I. POWER CONSUMPTION BREAKDOWN

Block Circuit	I/Q Gen.	I/Q LO Chain	IQ Modulator	SPI and Bias	Total
Pdc (mW)	6.3	122.5	0	6.6	135.4

Measured at Pout = -5.2dBm

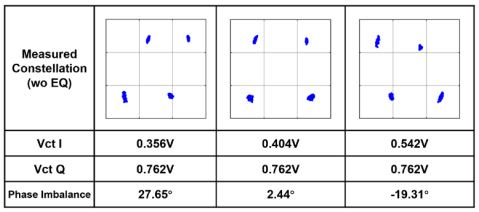

Fig. 11. Quadrature phase correction mechanism validation.

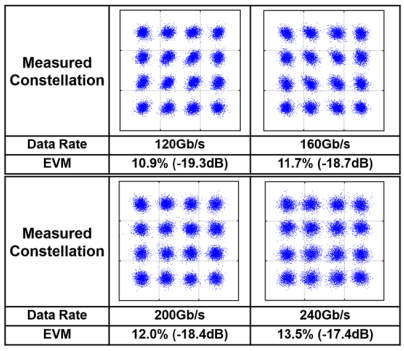

Fig. 12. Measured high-speed data EVM and constellations.

TABLE II. PERFORMANCE COMPARISON TABLE

Reference	This Work				ISSCC' 18 [1]	ISSCC' 22[2]	VLSI' 23[3]	JSSC' 23[4]	VLSI' 24[5]
Technology	28-nm CMOS				65-nm CMOS	22-nm CMOS	65-nm CMOS	130-nm SiGe	65-nm CMOS
RF Freq. (GHz)	142				87.5	140	112	140	142
TX Pout (dBm)	-5.2				-1.9	-3.8	-	-8	13
TX Pdc (mW)	135.4				120	161	200	2500	1150
Mod.	16QAM				16QAM	16QAM	16QAM	32QAM	16QAM/ 32QAM
Data Rate (Gb/s)	120	160	200	240	120	160	112	200	160/200
Link EVM (%)	10.9	11.7	12.0	13.5	14.3	12.7	14.8	8.3	13.4/10.4
Efficiency (pJ/bit)	1.1	0.85	0.68	0.52	1.0	1.0	1.79	12.5	7.19/5.75
Area	1.13/0.55*				6 (TRX)	0.75*	5.7 (TRX)	27.2 (TRX)	6.17

*Core Area.

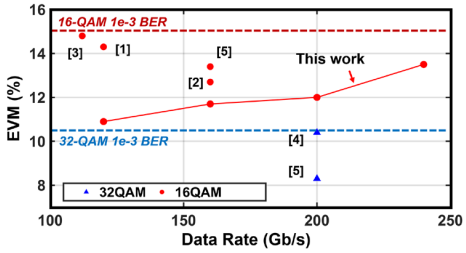

Fig. 13. EVM and data rate comparisons.

In the time-domain measurement, a VDI D-band IQ SHMixer serves as an external receiver to down-convert the 140GHz modulated signal. A Keysight UXR real-time oscilloscope is utilized to sample the receiving IQ signal. Two baseband LNAs are cascaded to suppress the noise from oscilloscope. To verify the IQ phase correction scheme, the control voltage (Vct) of the 140GHz IL-VCOs was tuned, and the corresponding measured 10M QPSK constellation rotations are presented in Fig. 11.

For high-speed measurement, an off-line complex EQ is employed to alleviate ISI from the dispersion of the WG fading channel [2]. As shown in Fig. 12, the transmitter achieves a record 240Gb/s data rate in 16QAM, resulting in an energy efficiency of 0.52pJ/bit. The measured EVM at 240Gb/s is 13.5%. Results at other data rates are also included in Fig. 12. Table II and Fig. 13 compare this work with other state-of-the-art transmitters supporting data rates exceeding 100Gb/s. To the best of our knowledge, this design achieves the highest data rate and energy efficiency among all reported mm-wave and D-band transmitters.

V. CONCLUSION

This work presents a 240Gb/s 0.52pJ/b D-band modulator-last transmitter with quadrature correction scheme in 28nm CMOS. The proposed architecture and circuit innovations achieve an optimal balance among bandwidth, linearity and output power. It achieves the highest data rate and energy efficiency, demonstrating its potential in high-capacity short-range communication and D2D interconnects.

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