A 7.4-9.6 GHz Harmonic-Shaping VCO with Implicit Second and Third Harmonics Expansion Achieving 195 dBc/Hz FoM and 206.4 dBc/Hz FoM_A

Bihong Zhang, Kaitian Yang, Xiaolong Liu
School of Microelectronics, Southern University of Science and Technology, Shenzhen, China
Email: liuxl@sustech.edu.cn

***Abstract*—This paper presents a compact, low-power, wideband harmonic-shaping complementary voltage-controlled oscillator (VCO) that improves phase noise (PN) and figure-of-merit (FoM) performance without the need for manual harmonic tuning. By leveraging a four-coil transformer, implicit common-mode (CM) and differential-mode (DM) impedance expansion at the second- and third-harmonic frequencies is achieved without incurring an area penalty. Furthermore, eliminating single-ended switch-capacitor arrays (SCAs) for second-harmonic tuning preserves the high CM tank quality factor (*Q*), thereby reducing PN and FoM variations across a wide frequency tuning range (FTR). Fabricated in a 65-nm CMOS process, the proposed VCO achieves an FTR of 26% from 7.4 to 9.6 GHz, consumes 1.2 mW of power, and occupies a core area of 0.073 mm². It achieves a peak FoM of 195 dBc/Hz and a peak FoM_A of 206.4 dBc/Hz at a 10 MHz offset.**

Keywords—CMOS, harmonic shaping, transformer, voltage-controlled oscillator (VCO), differential-mode, common-mode, low power, harmonic expansion.

I. Introduction

Harmonic-shaping VCOs that exploit second-harmonic CM or third-harmonic DM resonances have been extensively investigated to improve PN performance and FoM [1]–[5]. As shown at the top of Fig. 1, a single-coil resonant tank can generate an implicit CM resonance at twice the oscillation frequency (f_0) with minimal area overhead [1]. However, single-ended SCAs are required to manually align the first- to second-harmonic resonances over a wide FTR, which degrades the tank Q and, consequently, deteriorates PN and FoM performance. Similarly, [2] combines an implicit CM resonance with a class-F topology but still relies on low-Q single-ended SCAs for harmonic tuning. Moreover, these conventional implicit CM resonance approaches inherently exhibit a low Q_{CM} due to unavoidable CM magnetic-flux cancellation, resulting in a severe trade-off between the Q_{CM} and the mutual coupling coefficient (k_{CM}) of the resonant coil ($Q_{CM} \propto 1 - k_{CM}$). Alternatively, an explicit CM resonance extension with high impedance can be realized using a head or tail resonator [3], [4]. However, this method consumes extra area. In [5], a transformer-based resonator is employed to generate dual CM resonances. Nonetheless, the necessary single-ended SCAs continue to degrade the tank Q.

To overcome these limitations, this work proposes a compact harmonic-shaping complementary VCO that requires no manual harmonic tuning. As shown at the bottom of Fig. 1, implicit second- and third-harmonic resonance extensions are realized using a four-coil transformer. Additionally, a fourth-harmonic resonance is introduced to further suppress noise upconversion. By removing low-Q single-ended SCAs for second-harmonic tuning, the tank Q is enhanced, and variations in PN and FoM are reduced. Furthermore, the transformer feedback scheme increases the output swing, improving power efficiency.

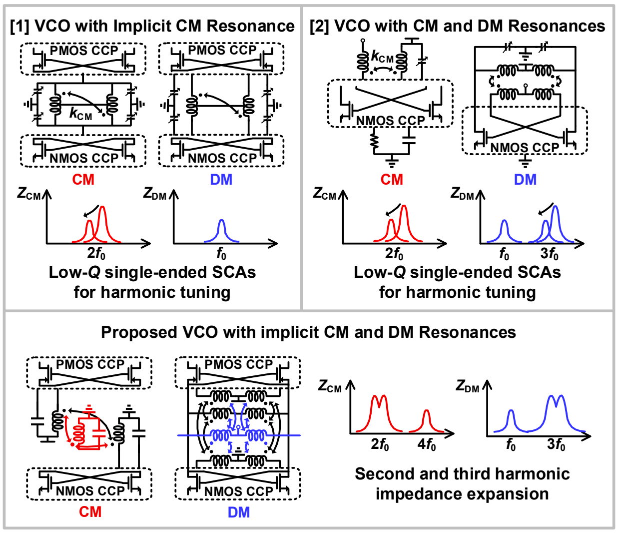

Fig. 1. CM and DM operations of the prior harmonic-shaping *LC* oscillators and the proposed VCO.

II. Proposed Transformer-Based Complementary VCO with Both CM and DM Impedance Expansion

Figs. 2(a)–(b) show the current direction and equivalent resonator of the proposed four-coil transformer under CM excitation. In the CM, the resonant coil L_1 is effectively disabled due to induced-flux self-cancellation. This scheme allows the remaining three coupled resonators ($L_{2,CM}C_{2,CM}$, $L_{3,CM}C_{3,CM}$, and $L_{4,CM}C_{4,CM}$) to generate three resonance peaks. By appropriately designing the high-Q fixed CM capacitors at different nodes of the coupled resonators, two of these peaks can be positioned around $2f_0$, thus extending the CM resonance bandwidth, as shown in Fig. 2(c). The simulated impedance exceeds 90 Ω over a fractional bandwidth of more than 26% at the center frequency of $2f_0$. A third peak is designed near $4f_{0,max}$ to mitigate PN deterioration at higher operating frequencies. Due to the complementary topology, the coupling coefficient k_{CM} in the CM tank is highly flexible, enabling a high Q_{CM}. More importantly, the realization of CM impedance expansion eliminates the need for single-ended SCAs for harmonic tuning, as illustrated in Fig. 3(a). Compared to previous implicit CM implementations [1], [2], [5], the simulated CM tank Q improves from 3.3 to 10, with a significant reduction in Q variation, as shown in Fig. 3(b). As a result, the proposed topology achieves a 0.9 dB improvement in PN and a 0.8 dB reduction in PN variation.

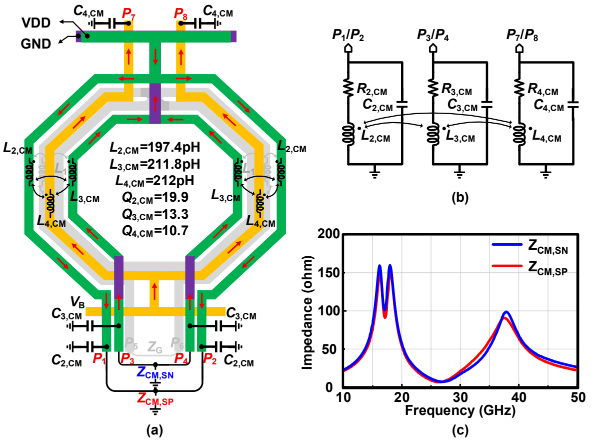

Fig. 2. (a) Proposed transformer in CM excitation, (b) equivalent circuit, and (c) simulated impedance seen from the source nodes.

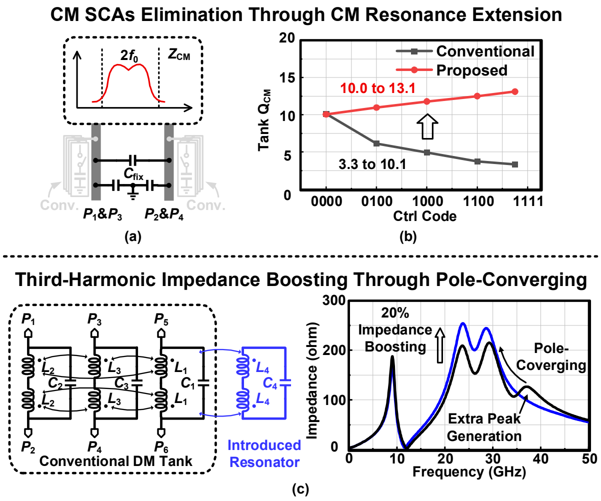

Fig. 3. (a) Elimination of the CM SCAs with CM resonance extension, (b) simulated tank Q improvement in CM, and (c) the proposed DM resonance extension with impedance boosting.

In the DM, the four-coil transformer facilitates third-harmonic resonance extension, as shown in Figs. 4(a)–(b). Based on the dual-peak bandwidth extension with coupled resonators ($L_{2,DM}C_{2,DM}$ and $L_{3,DM}C_{3,DM}$), the additional resonator ($L_{4,DM}C_{4,DM}$) introduces an extra impedance peak at a higher frequency. As plotted in Fig. 3(c), by pole-tuning, the highest peak is aligned near $3f_0$ and converges with the two lower peaks, resulting in an impedance boost of approximately 20%. As depicted in Fig. 4(c), the simulated 3-dB fractional bandwidth of the third-harmonic resonance is 41%, providing robust protection against process, voltage, and temperature (PVT) variations.

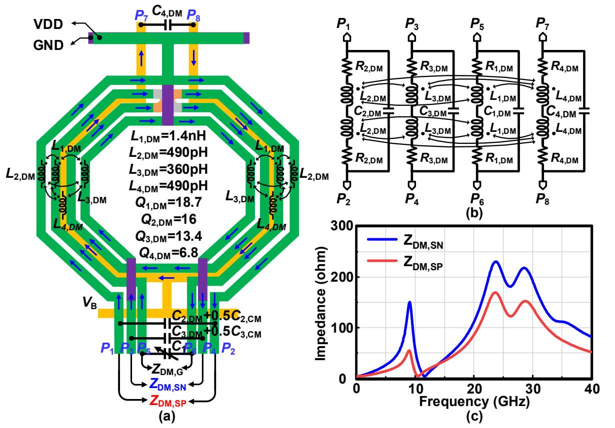

Fig. 4. (a) Proposed transformer in DM excitation, (b) equivalent circuit, and (c) simulated impedance seen from the source nodes.

III. Circuit Implementation

Fig. 5 shows the detailed schematic of the proposed transformer-based complementary VCO. A 4-bit differential SCA and a pair of varactors are used at the drain terminal for frequency tuning. By employing the proposed CM and DM impedance extension technique, the active device is significantly simplified. The interconnect line between the source and drain terminals is reduced by 65%, and the active device area is reduced by 25% due to the elimination of the harmonic-tuning SCA. This effectively reduces parasitics and preserves a high tank Q.

The proposed four-coil transformer is implemented using ultra-thick metal for L_1 (L = 1.4 nH, Q = 18.7), L_2 (L = 490 pH, Q = 16), L_3 (L = 360 pH, Q = 13.4), and thick metal for L_4 (L = 490 pH, Q = 6.8), achieving low loss. The electromagnetic (EM) simulated parameters of the transformer are presented in Fig. 5. Symmetric coupling coefficients between L_2 and L_3 are adopted to ensure matched source impedances for the PMOS and NMOS cross-coupled pairs.

Thanks to transformer feedback between L_1 and L_2/L_3, the gate-source voltage (V_{GS}) amplitude is boosted by 40%, as shown in Figs. 6(a)–(b), enhancing PN and power efficiency. As plotted in Figs. 6(c)–(d), the zero region of the impulse sensitivity function (ISF) corresponds to the flat region of the drain-source voltage (V_{DS}), and the effective ISF (ISF_{eff}) exhibits good symmetry. This results in a low DC value, suppressing the upconversion of flicker noise to the LC tank.

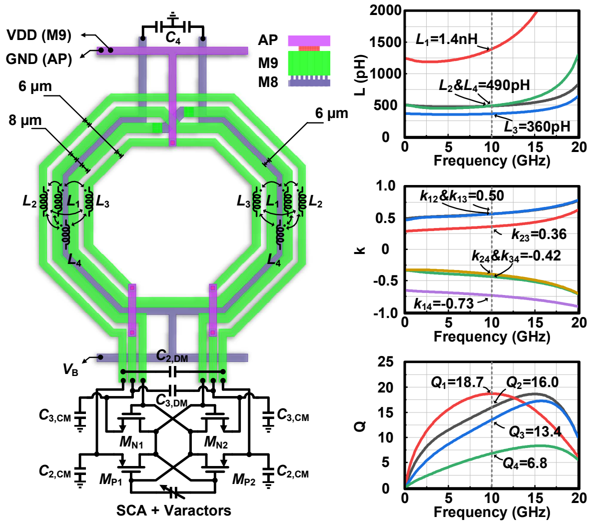

Fig. 5. Detailed schematic of the proposed VCO with layout and EM simulation results of the four-coil transformer.

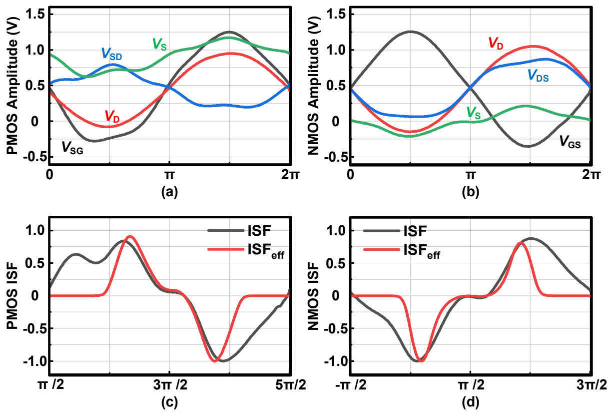

Fig. 6. Simulated voltage waveforms of the (a) PMOS and (b) NMOS tanks, and simulated ISFs and ISF_{eff}s of the (c) PMOS and (d) NMOS transistors.

IV. Measurement Results

The proposed prototype was fabricated in a 65-nm CMOS process, with the chip micrograph shown in Fig. 7. It achieves a compact core area of 0.073 mm^2 and low power consumption of 1.2 mW.

Fig. 8 presents the measured PN at the lowest and highest carrier frequencies. At 7.4 GHz and 9.6 GHz, the PN is −115.7 and −112.4 dBc/Hz at a 1 MHz offset, and −138.4 and −134 dBc/Hz at a 10 MHz offset, respectively. The measured FTR spans from 7.4 to 9.6 GHz. Figs. 9(a)–(b) and 10(a) summarize the measured PN, FoM, and flicker noise corner across the entire FTR. The corresponding FoM ranges from 192.7 to 195 dBc/Hz at a 10 MHz offset, and a peak FoM_A of 206.4 dBc/Hz. The measured flicker noise corner remains below 400 kHz across the full FTR.

Table I and Fig. 10(b) compare the performance of the proposed VCO with the state-of-the-art works. The proposed prototype demonstrates superior FoM, FoM_T, and FoM_A.

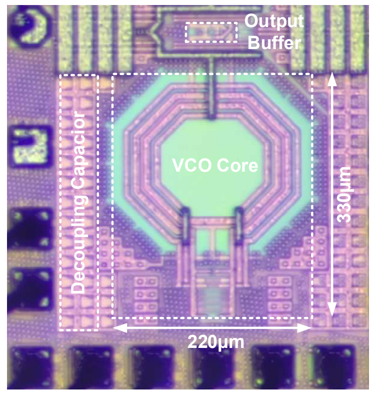

Fig. 7. Chip micrograph.

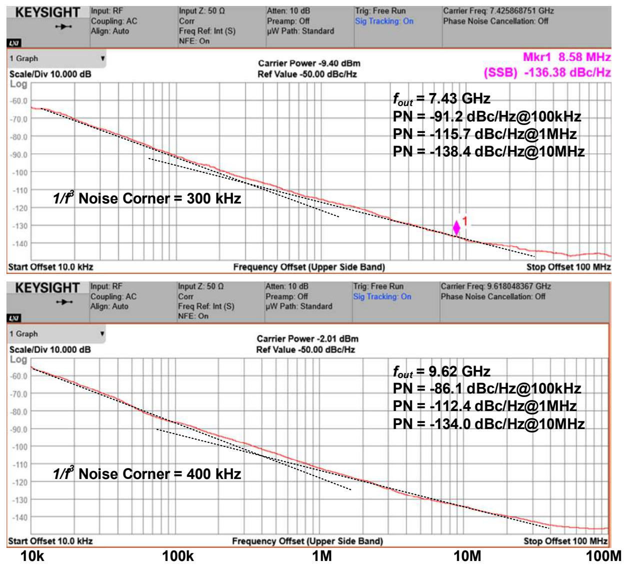

Fig. 8. Measured phase noise at 7.4 GHz and 9.6 GHz.

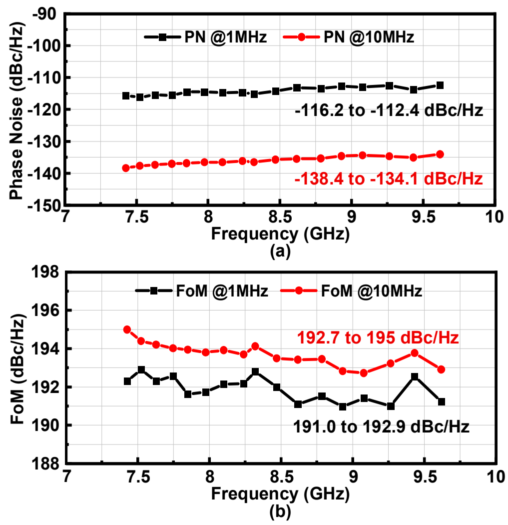

Fig. 9. Measured (a) phase noise and (b) FoM across the whole FTR.

TABLE I. PERFORMANCE COMPARISON WITH STATE-OF-THE-ART *LC* OSCILLATORS

Reference		ESSERC'25 [5]	VLSI'23 [6]	JSSC'24 [7]	TCASI'25 [8]	ISSCC'25 [9]	This work
Technology		65-nm CMOS	28-nm CMOS	65-nm CMOS	65-nm CMOS	28-nm CMOS	65-nm CMOS
Frequency (GHz)		7.7 to 10.1	7.8 to 9.4	12.3 to 15.2	10.7 to 13.2	8.1 to 9.9	7.4 to 9.6
Tuning Range		27%	18.1%	21.1%	20.9%	20%	26%
Supply (V)		0.9	0.58	0.6	0.6	0.9	0.9
Power (mW)		1.2	0.66	8.4	7.8	33.5	1.2
PN (dBc/Hz)	1M	-115.1 to -110.5	-103.8 to -98.6	-118 to -113.6	-117.4 to -114.5	-128.7 to -124	-116.2 to -112.4
	10M	-137 to -132	-127.1 to -112.7	-141.4 to -138.8	-139.4 to -138.2	-146.3 to -144.1[(a)]	-138.4 to -134.1
FoM[(b)] (dBc/Hz)	1M	189.3 to 192	179.8 to 183.6	188.1 to 190.4	187.6 to 188.7	189.7 to 191.4	191 to **192.9**
	10M	191.3 to 194.7	183.9 to 186.9	193.1 to 193.7	189.8 to 191.7	189.9 to 193.8[(a)]	192.7 to **195**
FoM_T[(c)] (dBc/Hz)	1M	197.9 to 200.6	184.9 to 189	194.6 to 196.9	194 to 195.1	193.7 to 197.4	199.2 to **201.2**
	10M	199.9 to 203.3	188.7 to 192	199.6 to 200.2	196.2 to 198.1	195.9 to 199.8[(a)]	201.1 to **203.4**
FoM_A[(d)] (dBc/Hz)	1M	200.6 to 203.3	193.5 to 197.3	200.3 to 202.6	200.3 to 201.4	195.6 to 198.4	202.3 to **204.3**
	10M	202.6 to 206	197.6 to 200.5	205.3 to 205.9	202.4 to 204.3	197.8 to 201.7[(a)]	204.1 to **206.4**
$1/f^3$ Corner (kHz)		180 to 250	500 to 600	450 to 700	310 to 450	320 to 380	200 to 400
Core Area (mm^2)		0.074	0.043	0.06	0.054	0.16	0.073

(a) Estimated from plots
(b) $FoM = -PN + 20\log_{10}(f_{LO}/\Delta f) - 10\log_{10}(P_{DC}/1mW)$
(c) $FoM_T = FoM + 20\log_{10}(TR/10\%)$
(d) $FoM_A = FoM + 10\log_{10}(1mm^2/Area)$

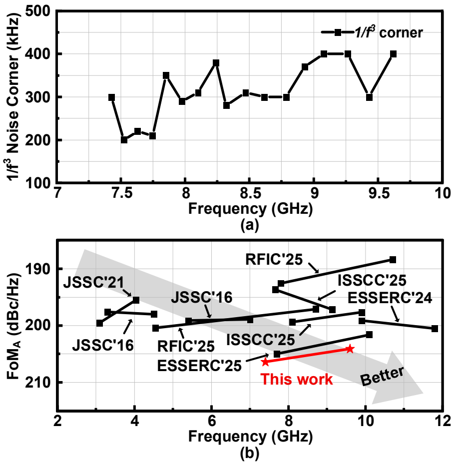

Fig. 10. (a) Measured flicker noise corners across the entire FTR and (b) comparison FoM_A@10 MHz with the prior state-of-the-art VCOs.

V. CONCLUSION

This paper presented a harmonic-shaping complementary VCO with implicit second- and third-harmonic impedance expansion. The proposed topology eliminates single-ended SCAs for harmonic tuning, preserving high tank *Q* and minimizing performance variations across the FTR. Fabricated in 65-nm CMOS, the proposed prototype achieves an FTR of 26% from 7.4 to 9.6 GHz, consumes 1.2 mW, and occupies a 0.073 mm² core area, yielding a peak FoM of 195 dBc/Hz and a peak FoM_A of 206.4 dBc/Hz.

ACKNOWLEDGMENT

This work was supported in part by the National Natural Science Foundation of China under Grant 62304098, in part by the Natural Science Foundation of Guangdong Province under Grant 2024A1515013269, and in part by the Guangdong Provincial Quantum Science Strategic Initiative GDZX2406005.

REFERENCES

[1] D. Murphy, H. Darabi and H. Wu, "Implicit common-mode resonance in *LC* oscillators," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 812–821, Mar. 2017.

[2] M. Shahmohammadi, M. Babaie and R. B. Staszewski, "A 1/f noise upconversion reduction technique for voltage-biased RF CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2610–2624, Nov. 2016.

[3] H. Guo, Y. Chen, P. -I. Mak and R. P. Martins, "A 5.0-to-6.36GHz wide-band-harmonic-shaping VCO achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz $1/f^3$ PN corner without harmonic tuning," *in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 294–295, Feb. 2021.

[4] S. Tian and X. Liu, "A class-F_{23} CMOS oscillator with second and third harmonic resonances expansion," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 73, no. 1, pp. 87–99, Jan. 2026.

[5] K. Yang and X. Liu, "A 7.7-to-10.1GHz transformer-based VCO achieving 194.7dBc/Hz FoM and 206dBc/Hz FoM_A with third-harmonic impedance expansion and dual common-mode resonances in 65nm CMOS," *in Proc. IEEE European Solid-State Electronics Research Conference (ESSERC)*, pp. 505–508, Sep. 2025.

[6] K. Xu, B. Yu, J. Hu, Y. Li, R. B. Staszewski and H. Xu, "A 50μW ring-type complementary inverse-class-D oscillator with 191.4dBc/Hz FoM and 205.6dBc/Hz FoM_A," *in IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, pp. 1–2, June 2023.

[7] Z. Lin, H. Jia, R. Ma, W. Deng, Z. Wang and B. Chi, "A low-phase-noise VCO with common-mode resonance expansion and intrinsic differential 2nd-harmonic output based on a single three-coil transformer," *IEEE J. Solid-State Circuits*, vol. 59, no. 1, pp. 253–267, Jan. 2024.

[8] Y. Gao et al., "A low-noise class-F_{23} VCO with harmonic resonance expansion and 2nd/3rd-harmonic outputs for multiband mm-wave applications," *IEEE Trans. Circuits and Syst. I, Reg. Papers*, vol. 72, no. 11, pp. 6679–6690, Nov. 2025.

[9] J. Chen, K. Xu, T. Siriburanon and R. B. Staszewski, "An 8.1-to-9.9GHz single-core pseudo-series-resonance oscillator achieving -128.7dBc/Hz PN at 1MHz," *in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 1–3, Feb. 2025.