A 256-316-GHz Frequency Quadrupler with Polyphase Continuous Harmonic Tuning and Power Combining Network in 65-nm CMOS

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***Abstract*—This paper presents an *H*-band frequency quadrupler in CMOS technology for terahertz communication and sensing applications. A continuous harmonic tuning analysis approach is proposed to investigate the optimum load impedance at the 1st, 2nd, 3rd and 4th harmonic frequencies, thus improving the conversion gain, output power, and efficiency of the quadrupler. Moreover, a polyphase continuous harmonic tuning and power combining (PCHTPC) network is proposed to further enhance the output power while simultaneously achieving suitable load impedances across continuous harmonic frequencies. Implemented in 65-nm CMOS technology, the prototype quadrupler integrates quadrature Lange couplers, buffer stages, quadrupling cores, and the proposed PCHTPC network within a chip area of 3.09 mm^2. Measurement results demonstrate that the quadrupler delivers an output power of 3.6 dBm with a 3-dB bandwidth spanning from 256 GHz to 316 GHz. Besides, it achieves a peak conversion gain of 6.1 dB and a DC-to-RF efficiency of 0.26%, respectively.**

***Index Terms*—frequency quadrupler, *H*-band, CMOS, power combiner.**

I. Introduction

In recent years, the terahertz (THz) band has attracted considerable research interest for next-generation wireless backhaul, data center interconnects, high-resolution imaging, and spectroscopy. In 2017, IEEE Std. 802.15.3d was released for ultra-high-speed wireless links in the frequency band from 252 GHz to 325 GHz (referred to as the "300-GHz band"). In these applications, the THz source is an essential building block to provide a frequency reference and a local oscillator (LO) signal. However, it remains challenging to generate a THz signal in the "300-GHz band" due to the limited device performance in the frequency band beyond the maximum oscillation frequency (f_{max}) of the CMOS technology.

Frequency doublers are commonly used to generate wideband THz signals in the 300-GHz band thanks to their favorable conversion gain and output power. Nevertheless, frequency doublers require a *D*-band THz input signal, which is also challenging to realize in CMOS technology [1]. A frequency quadrupler (FQ) is an alternative solution that relaxes the input frequency requirement to the *E*-band. However, FQs typically suffer from limited conversion gain, output power, and efficiency [2].

Weiping Wu and Xun Bao contributed equally to this work.

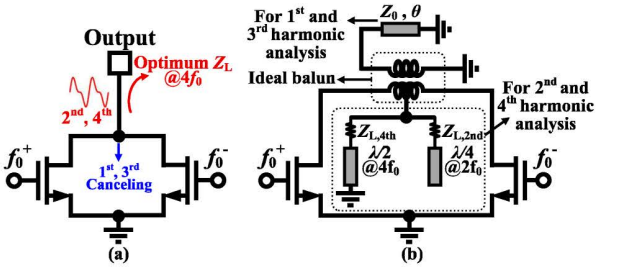

Fig. 1. (a) Conventional push-push frequency quadrupler. (b) Continuous harmonic tuning concept.

To address these challenges, this paper proposes an analysis methodology for continuous harmonic tuning at the 1st, 2nd, 3rd, and 4th harmonics, thus improving the conversion gain, output power, and efficiency of the FQ. Moreover, a polyphase continuous harmonic tuning and power combining (PCHTPC) network is proposed to simultaneously achieve continuous harmonic tuning and power combining, thereby further boosting the output power. Finally, an FQ based on the proposed PCHTPC technique is demonstrated in a 65-nm CMOS technology with an f_{max} of 250 GHz. The proposed FQ achieves a peak output power of 3.61 dBm with a 3-dB bandwidth from 256 GHz to 316 GHz.

II. Continuous Harmonic Tuning Concept and Polyphase Power Combining Network

A. Continuous Harmonic Tuning Concept

Fig. 1(a) shows the schematic of the conventional push-push frequency quarupler. In this configuration, odd-harmonics are cancelled out with each other at the drain of transistors, and the load impedance is optimized at the $4f_0$. However, the conventional quadrupler encounters two main limitations: first, odd-harmonic currents are dissipated, and the underutilization of odd-harmonic currents restricts the performance in THz bands, particularly beyond f_{max}; second, the load impedance at $2f_0$ is generally neglected, which also degrades the performance of the quadrupler.

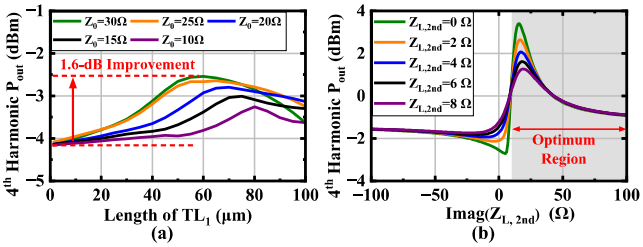

Fig. 2. Simulated 4th harmonic P_{out} at optimum $Z_{L,4th}$ with (a) $Z_{L,2nd}$=0 and sweeping TL_1, (b) TL_1(Z_0=30Ω, Length=60μm) and sweeping $Z_{L,2nd}$.

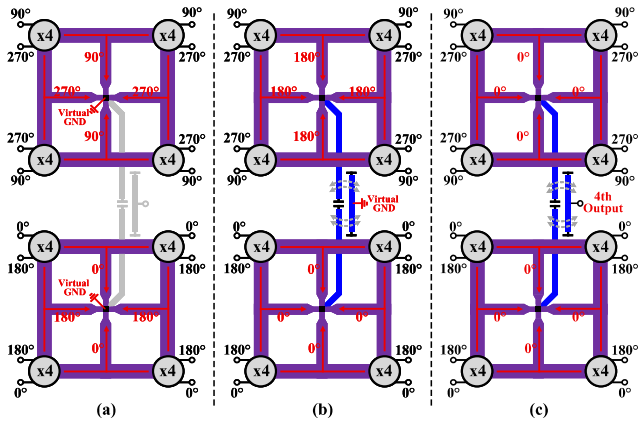

Fig. 3. Operation principle of the proposed polyphase continuous harmonic tuning and power combining network at (a) odd-mode harmonics, (b) the 2nd harmonic, and (c) the 4th harmonic.

As shown in Fig. 1(b), this paper proposes a continuous harmonic tuning analysis approach to investigate the optimum load impedance at the 1st, 2nd, 3rd, and 4th harmonic frequencies. The approach consists of three main steps. First, an ideal balun is utilized to decouple odd- and even-harmonic paths. Second, a transmission line TL_1 is utilized as an odd-mode load to enhance the 1st and 3rd harmonics at the drain of the transistor. These harmonics are then fed back to the input of the quadrupler, thereby boosting the output power at the 4th harmonic. Third, the network formed by $Z_{L,4th}$ and TL_2 is employed to present the desired load at $4f_0$ while presenting an open circuit at $2f_0$, whereas $Z_{L,2th}$ and TL_3 together provide the appropriate load at $2f_0$ and an open circuit at $4f_0$.

Fig. 2 presents simulation results based on the proposed continuous harmonic tuning concept, with a transistor size of 48 μm/60 nm and an input power of 10 dBm. Fig. 2(a) shows the 4th output power with $Z_{L,2nd}$=0 and sweeping parameters of TL_1. The quadrupler with an odd-mode load of TL_1 (Z_0=30Ω, Length=60μm) exhibits a 1.6 dB higher output power compared to the conventional quadrupler. Moreover, as shown in Fig. 2(b), the load impedance at $2f_0$ ($Z_{L,2nd}$) also significantly impacts the output power, and the optimum $Z_{L,2nd}$ locates in an inductive region.

B. Polyphase Power Combining Network

To further enhance the output power and to achieve appropriate load impedance simultaneously at the 1st, 2nd, 3rd, and

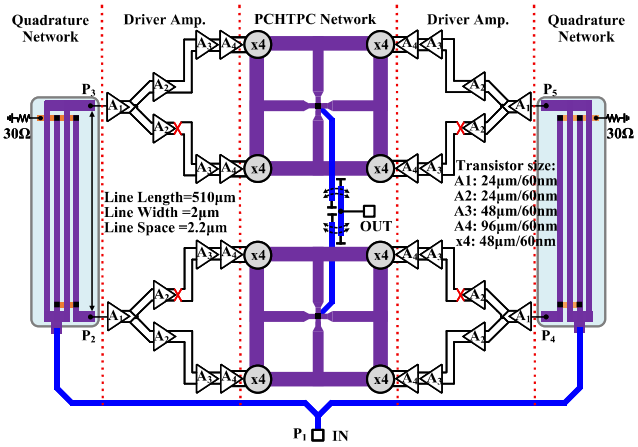

Fig. 4. Schematic of the proposed quadupler based on the PCHTPC network.

4th harmonic frequencies, this paper proposes a PCHTPC network, as illustrated in Fig. 3. The PCHTPC network consists of eight frequency-quadrupling cores, two grid-shaped power combiners, and a coupled-line-based matching network. By carefully distributing the phases of input signals as 0°, 90°, 180°, and 270°, the load impedances at the 1st, 2nd, 3rd, and 4th harmonics can be partially decoupled. First, as shown in Fig. 3(a), odd-mode currents cancel with each other at the center of the grid-shaped combiner, which acts as a virtual ground for odd-mode signals, effectively preventing the odd-mode signals from propagating to the output node. Consequently, the physical parameters of grid-shaped combiners can be determined by the optimal TL_1. Second, the 2nd harmonic maintains a consistent phase across all branches within each individual grid-shaped combiner, while exhibiting an anti-phase relationship between the two combiners. Therefore, the 2nd harmonic is canceled out at the output node, which serves as a virtual ground at $2f_0$. The 2nd-harmonic virtual ground at the output node also facilitates the realization of an inductive $Z_{L,2nd}$ at the load of the quadrupling core, which is beneficial to further enhancing the 4th-harmonic output power. Thirdly, the 4th harmonic exhibits an identical phase across all branches within both grid-shaped combiners, thus effectively combining the 4th-harmonic powers. The coupled-line-based coupler is utilized to achieve the optimum $Z_{L,4th}$.

III. Prototype Implementation

A frequency quadrupler with the proposed PCHTPC network is implemented in a 65-nm bulk CMOS technology, whose schematic is shown in Fig. 4. Two Lange couplers are utilized to generate the quadrature signals for frequency-quadrupling paths. Each path consists of four buffers and one quadrupling core. The quadrupled signals are combined with the proposed polyphase combining network.

Lange couplers feature multiple advantages. Firstly, it supports large bandwidth with a small area overhead. Secondly, the large range of achievable coupling coefficient enables a good amplitude-phase consistency. Fig. 5 shows that for

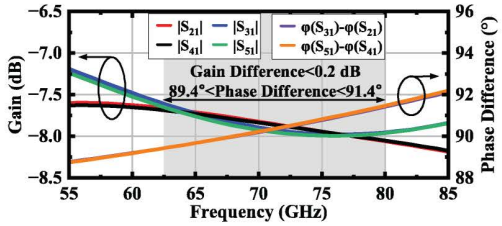

Fig. 5. Simulated amplitude and phase performance of the quadrature input matching network.

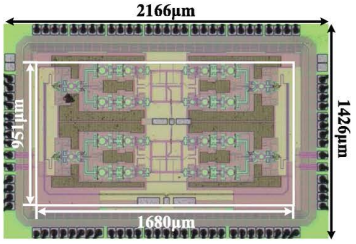

Fig. 6. Chip micrograph.

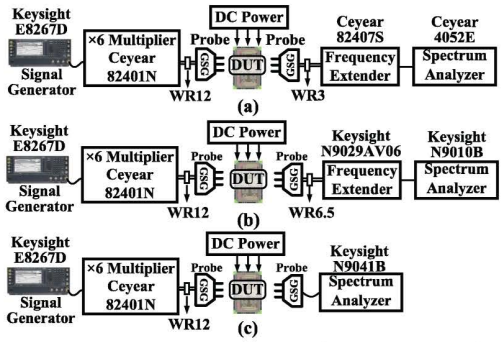

Fig. 7. Measurement setups of (a) 4th and 3rd harmonic; (b) 2nd harmonic; (c) 1st harmonic.

frequencies between 64 and 79 GHz, the gain difference of the quadrature input matching network is below 0.2 dB, with a phase difference between 89.4° and 91.4°. In buffer stages, three-coupled-lines (TCLs) are utilized at the first stage for wideband matching, whose theories and analyses have been discussed in [3]. Cross-coupled neutralized differential structures are used in the following three stages, where transistor sizes are scaled up by stage for optimizing linearity and output power. To provide consistent phase of quadrupled signals for the polyphase combining network, the swap of signal phase is realized at the output of second buffer stage. The proposed PCHTPC network is employed to simultaneously combining the 4th-harmonic powers and achieving suitable load impedances across continuous harmonic frequencies, thereby improving the output power, efficiency, and CG of the quadrupler.

IV. Measurement Results

The proposed frequency quadrupler is implemented in a 65-nm bulk CMOS process. The chip micrograph is shown in Fig. 6, with an area of 2.17×1.43 mm^2. Fig. 7 shows the

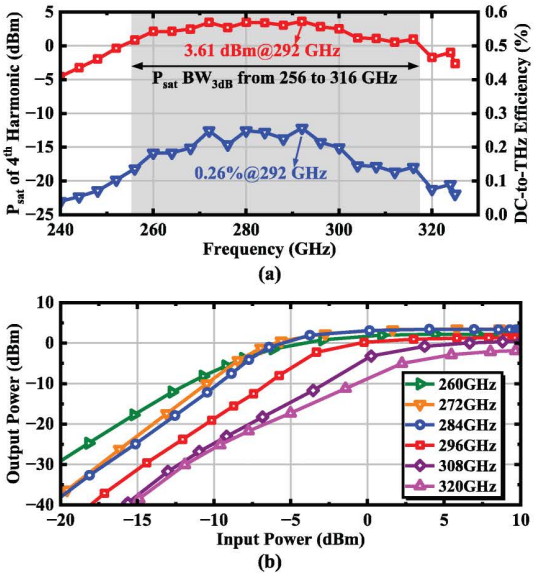

Fig. 8. (a) Measured saturated output power and DC-to-THz efficiency versus frequency, and (b) output power versus input power of the proposed quadrupler.

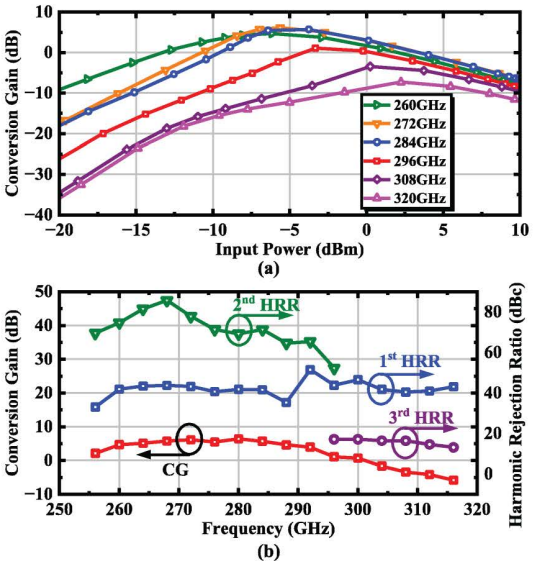

Fig. 9. Measurement results of (a) conversion gain versus input power; (b) conversion gain and harmonic rejection ratios at saturation versus frequency.

measurement setups. A signal generator, Keysight E8267D, is utilized to provide the input power, which is multiplied by a ×6 multiplier, Ceyear 82401N, to be injected into the DUT. For the output power characterization at the 4th and the 3rd harmonic, a spectrum analyzer, Ceyear 4052E, works with a frequency extender, Ceyear 82407S, to characterize the output power. For the 2nd and the 1st harmonic measurement, a spectrum analyzer, Keysight N9010B, is used to measure the harmonic powers, where a D-band frequency extender N9029AV06 is inserted to characterize the 2nd harmonics.

Fig. 8 (a) shows the measured saturated out power (P_{sat})

Table I Performance comparison with the state-of-the-art CMOS THz frequency multipliers.

	This work	ISSCC '23 [4]	ISSCC '21 [5]	TMTT '16[6]	TTST '23 [7]	IMS '24[8]	IMS '23[9]
Process	65nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS	40nm CMOS	40nm CMOS	40nm CMOS
f_{max} of Process (GHz)	250	NA	250	250	NA	260	NA
Topology	DA, ×4	PLL, ×2	DA, ×2, ×3	DA, ×4	DA, ×3, DA, ×2	DA, ×3	DA, ×2, DA, ×2, DA, ×2
Supply (V)	1.2	NA	NA	1.4	249-266	1.5/0.9	1.1/1.8
f_c (GHz)	286	275.5	380	390	257.5	234	231.5
$f_c > f_{max}$	Yes	NA	Yes	Yes	NA	No	NA
BW (GHz)	60 (256-316)	23 (264-287)	40 (360-400)	40 (370-410)	17 (249-266)	34 (218-252)	41 (211-252)
Fractional BW (%)	29.5	8.4	10.5	10.3	6.6	10.2	17.7
Peak CG (dB)	6.1	NA	NA	-20	NA	-5.7	NA
P_{sat} (dBm)	3.6	-2.5	-10.9	-7	3	-2.7	-4
HRR (dBc)	13	NA	NA	NA	NA	11	NA
DC-to-RF efficiency (%)	0.255	0.216	0.059	0.013	0.22#	0.56	0.145
DC Power (mW)	896	262	138	1500	890	96	275
Chip area (mm^2)	3.09	1.16	3	10.5	7.3	0.43	1.17

Calculated by provided data.

and DC-to-THz efficiency (η) versus output frequency. Fig. 8 (b) exhibits the output power versus input power at multiple frequencies. A P_{sat} of 3.61 dBm is achieved at 292 GHz, with a -3dB-bandwidth of 60 GHz from 256 to 316 GHz. A peak η of 0.26% is achieved at 292 GHz. Fig. 9 (a) and (b) illustrate the measured conversion gain (CG) versus input power and harmonic rejection ratio (HRR) under saturation versus frequency, respectively. The maximum CG of the quadrupler is 6.1 dB at 280 GHz. Over the whole band, the 1st, 2nd, 3rd HRR exceeds 33 dBc, 52dBc, and 13 dBc, respectively.

Table I summarizes and compares the frequency quadrupler's performances with the state-of-the-art CMOS THz frequency multipliers. With the proposed technique, the prototype quadrupler features wide bandwidth, high CG, large output power, and competitive efficiency, with the widest fractional bandwidth (FBW) of 29.5%.

V. Conclusion

This paper demonstrates a CMOS *H*-band frequency quadrupler. A continuous harmonic tuning concept is proposed to obtain the optimum load impedance across continuous harmonic frequencies, thereby improving the performance of the quadrupler. Moreover, a PCHTPC network is proposed to further enhance the output power while simultaneously achieving a suitable load impedance across the continuous harmonic frequencies. The prototype quadrupler is fabricated in 65-nm CMOS technology and achieves superior output power, bandwidth, and conversion gain compared to state-of-the-art CMOS counterpart.

Acknowledgment

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