A Sub-mW and Sub-100fs$_{rms}$ Jitter 6.4GHz Fractional-N Hybrid PLL with -260.9dB FoM and a 100MHz reference in 28nm CMOS

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***Abstract*—A 0.88mW and 96fs$_{rms}$ jitter 6.4GHz fractional-N hybrid phase-locked loop (PLL) with a 100MHz reference and a 0.11mm^2 core area is presented. Gated-LMS-based voltage-controlled-oscillator (VCO) duty-cycle (DC) calibration (DCC) is used to allow digital-to-time converter (DTC) delay range reduction with 1st-order delta-sigma modulator (DSM-1). A capacitive digital-to-analog converter (CDAC) is used in a merged DTC and sampling phase detector (SPD) to cancel residual quantization error. The merged DTC-SPD also extracts phase error polarity for digital integral path without extra PD to avoid phase offset mismatch between PDs. A dual-edge retimer employs two tri-state TSPC D-flip-flops (DFFs) to reduce power consumption and remove the output multiplexer (MUX).**

Keywords—Fractional-N, PLL, gated LMS, low power, low jitter

I. Introduction

A fractional-N PLL is an essential building block in modern electronic systems. Its chip area, jitter and power consumption greatly impact overall system cost and energy efficiency. Achieving both low integrated jitter and low power consumption results in a high figure-of-merit (FoM). Although prior art achieved a FoM up to -261dB, it requires a reference frequency above 2.2GHz to reduce the delta-sigma modulator's (DSM) quantization noise and an advanced technology node down to 7nm to reduce power consumption [1]. A hybrid PLL can achieve a small chip area with low jitter. However, existing hybrid PLLs utilize two separate PDs for proportional and integral paths and requires additional delay to compensate for offset mismatch between these two PDs [5], which degrades jitter performance. In addition, offset mismatch still exists under process, voltage and temperature (PVT) variations and may drive the PD with a high detection gain into saturation. This work presents a 100MHz reference-driven fractional-N hybrid PLL with 0.11mm^2 core area and a -260.9dB FoM by using power reduction and DTC delay reduction techniques. It also resolves PD output saturation issue by using shared PD for both proportional and integral paths.

II. Proposed Fractional-N Hybrid PLL

A. Overall Architecture

Fig.1 illustrates the block diagram of the proposed fractional-N PLL with a DTC-based sampling PLL architecture for high FoM [2-6] and a hybrid loop for a compact chip area [5]. The DTC consists of a 4-bit tree-like coarse DTC (C-DTC) for short minimum delay [2] and a 10-bit fine DTC which is merged into the DTC-SPD [6,7] for

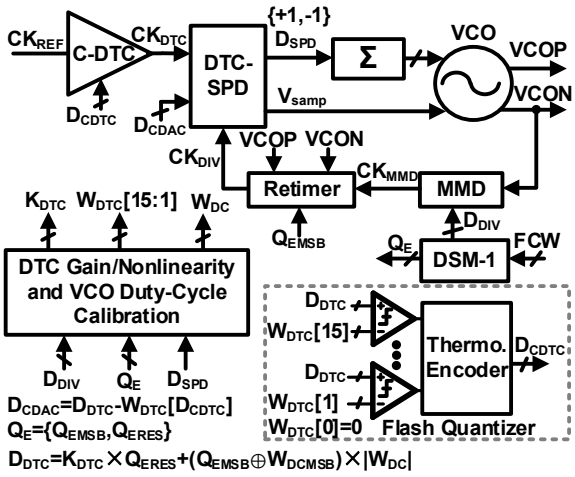

Fig. 1. Block diagram of the proposed fractional-N hybrid PLL

low jitter and low power consumption. Since both the integral and proportional paths share the same PD rather than use separate PDs [5], the proportional path attains a well-defined control voltage without requiring phase-offset mismatch correction. The LC VCO uses an NMOS-only cross-coupled pair with 2nd-harmonic common-mode resonance [4]. The multi-modulus divider (MMD) is dithered by a DSM-1 instead of DSM-2 to reduce the DTC delay range [2,3]. The DTC delay range is further reduced by retiming the MMD output with a dual-edge retimer [4]. To suppress fractional spurs caused by DTC's coarse-fine mismatch-induced nonlinearity (NL) and gain error and VCO DC error, a calibration engine obtains the C-DTC delay weights W_{DTC}[15:1], DTC gain K_{DTC}, and the VCO DC coefficient W_{DC}. The linear DTC control (D_{DTC}) is quantized by a flash quantizer with W_{DTC}[15:1] as a reference to generate C-DTC control (D_{CDTC}). Its residue code (D_{CDAC}) drives the CDAC in the DTC-SPD to compensate for the flash-quantizer's quantization error and linearize DTC [2,3] without using an additional fine DTC [6].

B. Calibration Engine

Fig.2 shows the DTC gain and NL calibration and VCO DCC techniques. To allow the use of DSM-1 at near-integer settings, the gated-LMS calibration technique [2,3] is utilized for both DTC gain and NL calibration. Since V_{samp} produces narrow pulses of opposite polarity at both rising and falling edges of Q_{EMSB} with near-integer settings and VCO DC error. This property allows gated-LMS to be applied to VCO DCC, thereby halving the DTC delay range requirement. The

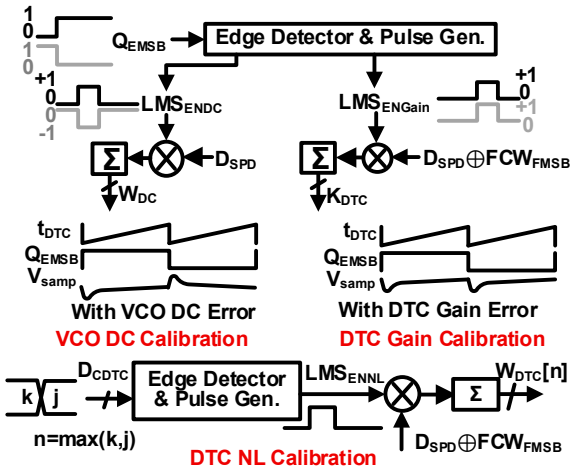

Fig. 2. Block diagram of the gated-LMS-based VCO DCC, DTC gain nonlinearity calibration

gated-LMS VCO DCC uses an edge detector to detect the transitions of Q_{EMSB} and a pulse generator to generate a signed LMS enable signal (LMS_{ENDC}). This signal is correlated with D_{SPD} and accumulated to tune W_{DC}. Similarly, with DTC gain error and the dual edge retimer, the V_{samp} also generates narrow pulses with the same polarity at both Q_{EMSB} transition edges rather than only after the division ratio pulse [2,3]. The DTC gain error and NL-induced narrow pulses polarities change with different FCW_{FMSB}, where FCW_{FMSB} is the MSB of the fractional frequency control word (FCW). Two unsigned LMS enable signals LMS_{ENGain} and LMS_{ENNL} are thus generated, correlated with $D_{SPD}\oplus FCW_{FMSB}$ and then accumulated to update K_{DTC} and $W_{DTC}[15:1]$ for gain and NL calibration respectively. At the medium-integer and far-integer settings, the SPD output pulse may overlap with subsequent pulses and affect the stability of gated-LMS calibration. Fortunately, since the error signals at SPD output are not filtered out by the PLL loop, conventional LMS calibration can be applied to DTC gain and nonlinearity and VCO duty-cycle calibration.

C. Circuit Implementation

The merged DTC-SPD performs quantization error cancellation in SPD without DTC by using either a resistive DAC (RDAC) [6,7], CDAC [11,12] or a switched capacitor (SC) approach [10]. The RDAC consumes static power and slows down settling time, while existing CDAC-based DTC-SPD designs require a transmission gate (TG) as sampling switch between the sampling capacitor and the switched current source. The TG exhibits large ON-resistance when the sampled voltage is close to half of the supply voltage, which limits the rise time of the voltage across the sampling capacitor and thus limits available detection gain. The SC-based DTC-SPD have strong NL caused by switch resistance [10], which becomes worse with a higher detection gain. Although NL can be compensated by using charge injection [10], the compensation accuracy is vulnerable to PVT variations, which is similar to digital predistortion without calibration. Therefore, a merged DTC-SPD with CDAC without a TG-based sampling switch is used as shown in Fig.3. The charging current is turned on when both CK_{BUF} and CK_{DIV} are low. As part of the charging capacitance, the CDAC adds only minimal extra dynamic power consumption. After compensation, a comparator is triggered to convert the

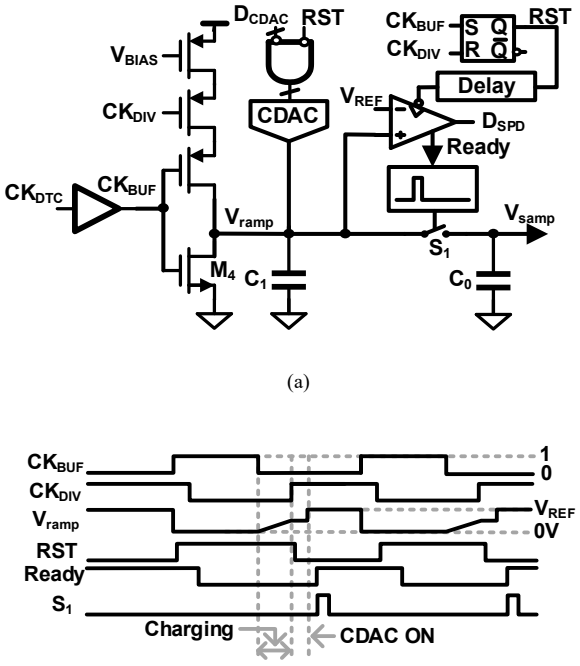

Fig. 3. (a) Schematic of the merged DTC-SPD with CDAC (b) timing diagram of DTC-SPD

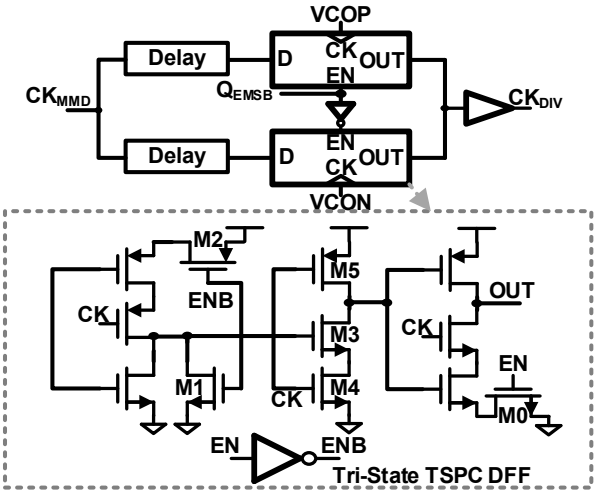

Fig. 4. Schematic of the dual-edge retimer with tri-state TSPC DFFs

phase error polarity into a 1-bit output (D_{SPD}) for calibration and the integral path. The compensated sampled voltage is transferred to the output holding capacitor (C_0) to control the proportional-path varactor after comparison to avoid pulse amplitude reduction [3]. The simulated input-referred integral NL is within 44fs with a detection gain of 15.8GV/s.

Fig.4 shows the dual-edge retimer employing tri-state TSPC DFFs. Conventionally, a dual-edge retimer is realized using two cascaded DFFs with an output MUX [4,7], which requires two high-speed DFFs operating simultaneously, thereby doubling power consumption. Therefore, the proposed design utilizes two tri-state TSPC DFFs operating complementarily with a shared output, reducing power

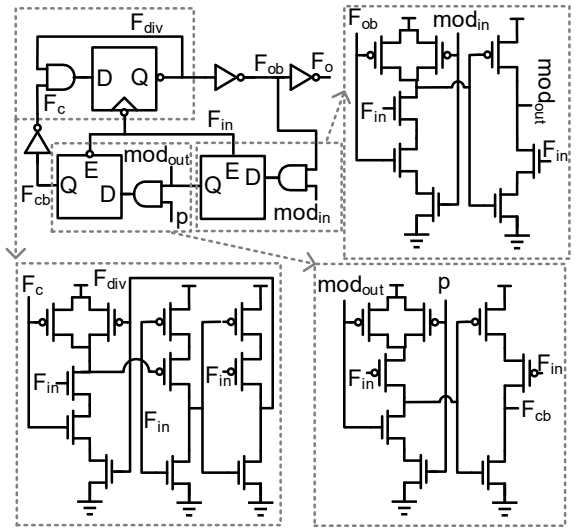

Fig. 5. Schematic of divided-by 2/3 frequency prescaler

consumption. In the off state of TSPC DFF, M3 is disabled to prevent high-speed dynamic current through M4 and M5, while M0 is turned off to leave the output stage in a high-impedance state, allowing it to be shared with the other DFF. To meet setup and hold-time requirements, two different delay lines are inserted between CLK_{MMD} and the DFF inputs.

The MMD is implemented by cascading divided-by 2/3 cells [8]. Since the MMD output is retimed to remove output jitter, it uses a transistor width of 90nm for the first two stages to save power. To maintain high speed operation with small size, the first two stages use TSPC-based DFF and latches with merged AND gate as shown in Fig.5 and the first stage uses ultra-low-threshold-voltage transistors.

III. Measurement Results

The presented fractional-N PLL occupies a core area of 0.11mm^2, as shown in Fig.9 and TABLE I. It consumes only 0.88mW (TABLE I) with a 100MHz reference input and FCW=64+2^{-14}. Fig.6 and Fig.7 show the measured output phase noise spectrum in integer-N and fractional-N mode. Fig.8 shows the measured output jitter and fractional spur levels with different fractional FCW (FCW_F). When approaching far-integer settings, the V_{samp} output pulses overlap with subsequent pulses, destabilizing the gated-LMS calibration. For $FCW_F < 2^{-6}$, gated-LMS calibration is applied to DTC gain, NL, and VCO DC. For $FCW_F \geq 2^{-6}$, the DTC NL calibration is then switched to conventional LMS calibration algorithm, and for $FCW_F \geq 2^{-4}$, both the DTC gain and VCO DC calibrations are changed to LMS mode for stable calibration. The worst-case integrated jitter with fractional spurs is 96fs_{rms}, while the fractional spurs remain below -61.2dBc. The measured performance of this work is summarized and compared with the prior arts (TABLE II). It achieves a FoM of -260.9dB with a 100MHz reference and smaller chip area.

IV. Conclusion

This work pushes fractional-N PLL's FoM down to -260.9dB with only a 100MHz reference by using power reduction and DTC delay reduction techniques and occupies only 0.11mm^2 core chip area by using a shared-PD-based

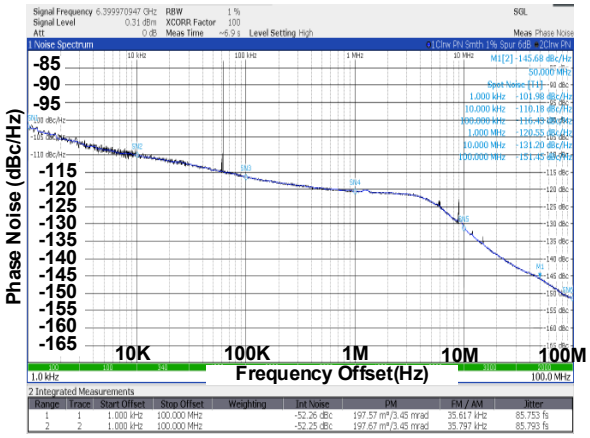

Fig. 6. Measured PLL's output phase noise spectrum in integer-N mode with FCW=64

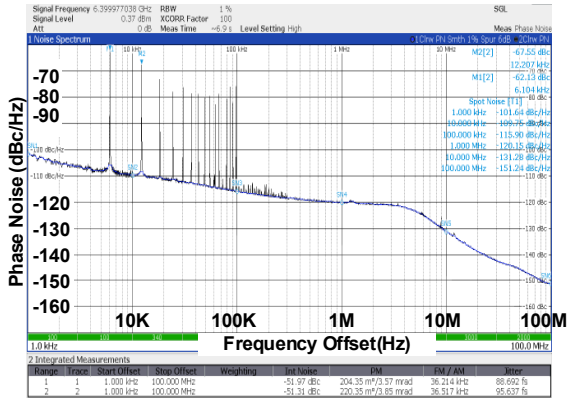

Fig. 7. Measured PLL's output phase noise spectrum in fractional-N mode with FCW=64+2^{-14}.

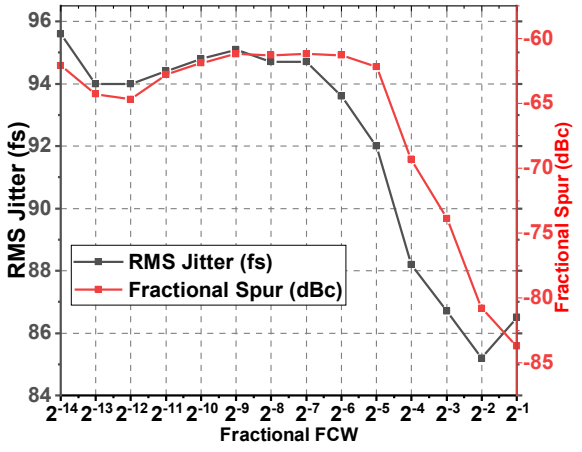

Fig. 8. Measured PLL's output rms jitter and fractional spur versus different fractional FCW with integer FCW=64.

hybrid loop without offset compensation. The gated-LMS calibration is extended to VCO DCC with DSM-1 to reduce DTC delay range to half of VCO period. CDAC-based DTC-SPD is used to avoid power and jitter contributed by fine DTC and also provide detection outputs for both analog proportional path and digital integral path.

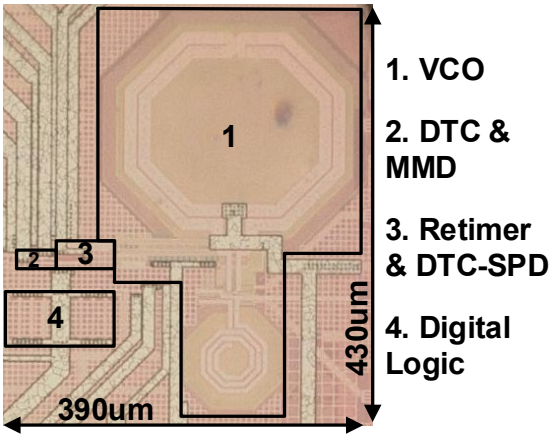

Fig. 9. Die photo of the presented fractional-N hybrid PLL

TABLE I. POWER CONSUMPTION AND CHIP AREA BREAKDOWN

Building Block	Power Consumption (mW)	Chip Area (mm^2)
VCO	0.53	0.0964
Retimer and DTC-SPD	0.15	0.0029
C-DTC	0.03	0.0016
MMD	0.07	
Digital Logic	0.1	0.0095
Total	0.88	0.1104

TABLE II. PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR FRACTIONAL-N PLLS.

	This Work	JSS25 [1]	VLSI25 [3]	ISSCC25 [9]	ISSCC26 [10]
PLL Arch.	Hybrid	Analog	Analog	Analog	Analog
Ref. Freq. (MHz)	100	2285	100	80×2	250
Out. Freq. (GHz)	6.4 (6.2-8)	4.85 (4.8-5)	6.4 (6.1-7.9)	9.5 (7.3-9.5)	13.75 (13.1-14.5)
RMS Jitter(fs)	96	91	96.6	37.7	29.7
In-Band Frac. Spur (dBc)	-61.2	-64	-65	-64.8	-67.4
Reference Spur (dBc)	-72.6	-70	-71.7	-101	-73.2
Power (mW)	0.88	0.96	1.94	24.4	18.1
FoM*	-260.9	-261	-257.4	-254.6	-258
Area (mm^2)	0.11	0.18	0.23	0.39	0.34
Technology	28nm	7nm	40nm	22nm	28nm

* $FoM=10\times\log_{10}[(Power/1mW)\times(RMS\ Jitter/1s)^2]$

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