A Single-Ended 2-to-32 Gb/s Multi-Lane-Shared EOM with 92% De-embedding Fidelity for Multi-Standard Chiplet and Memory Interfaces

Xianting Su[1], Xiaoteng Zhao[1*], Jie Liu[1], Chenxi Han[1], Zhicheng Dong[2],
Zekai Yang[1], Hongyu Su[1], Lin Wang[1], Hongzhi Liang[1], Shubin Liu[2], Zhangming Zhu[2]
[1]Key Laboratory of Analog Integrated Circuits, School of Integrated Circuits, Xidian University, Xi'an 710071, China.
[2]Zhejiang Key Laboratory of Analog Integrated Circuits, Hangzhou Institute of Technology, and also with School of Integrated Circuits, Xidian University, Hangzhou 311231, China
[*]Email: xtzhao@xidian.edu.cn

***Abstract*—This paper presents a reconfigurable single-ended eye-opening monitor (EOM) operating from 2 to 32 Gb/s for chiplet and memory interfaces. The design features a multi-lane-shared architecture enabled by the proposed single-bit-response (SBR) measurement and de-embedding methods. Moreover, it incorporates an 8-bit, quarter-rate phase interpolator (PI) employing balanced load cells and digital calibration to ensure high linearity across a wide operating range. Fabricated in 28-nm CMOS, the prototype occupies an area of 0.011 mm^2 and consumes 20.42 mW. The PI exhibits a peak-to-peak integral nonlinearity (INL_{pp}) of less than 2.5 LSB over a relative bandwidth of 16. Overall, the proposed EOM achieves a coefficient of determination (R^2) of >0.99 compared with the golden reference and a 92% intersection-over-union (IoU), demonstrating high de-embedding fidelity.**

***Keywords*—built-in self-test (BIST), eye-opening monitor (EOM), phase interpolator (PI), de-embedding**

I. Introduction

The explosive growth of global data traffic imposes stringent demands on the I/O capabilities for high-performance computing (HPC) systems and drives the development of numerous interface standards, as shown in Fig. 1(a) [1]. While eye diagrams serve as a critical metric for assessing signal integrity and bit error rate (BER), oscilloscope-based characterization becomes impractical for multi-channel, high-density transmission scenarios, such as the chiplet and memory interfaces depicted in Fig. 1(b). Consequently, on-chip or co-packaged eye-opening monitors (EOMs) for built-in self-test (BIST) offer a more viable and representative alternative. However, most existing EOMs target differential signaling, overlooking the dominance of single-ended interfaces in chiplet and memory applications.

A second challenge arises from the massive lane counts in these systems, where conventional EOMs support only single-lane testing, leading to prohibitive area overhead. This work introduces a multiplexer-based (MUX-based) EOM reuse architecture to mitigate this cost. Nevertheless, varying channel losses across lanes caused by distance discrepancies can degrade measurement accuracy. To address this, we implement a calibration scheme leveraging an 8-bit quarter-rate phase interpolator (PI) and a proposed de-embedding algorithm, enabling precise multi-lane-shared EOM operation, as shown in Fig. 1(b).

Thirdly, to ensure compatibility with multiple standards, timing scanning linearity is enhanced by employing balanced load cells with digital calibration. This optimization reduces the PI's integral nonlinearity (INL) across the operating range. Fabricated in 28-nm CMOS, the proposed EOM supports a data rate from 2 to 32 Gb/s while achieving high measurement fidelity, with a coefficient of determination (R^2) exceeding 0.99 in all conventional acquisition modes and an intersection-over-union (IoU) of 92% for channels with different lengths.

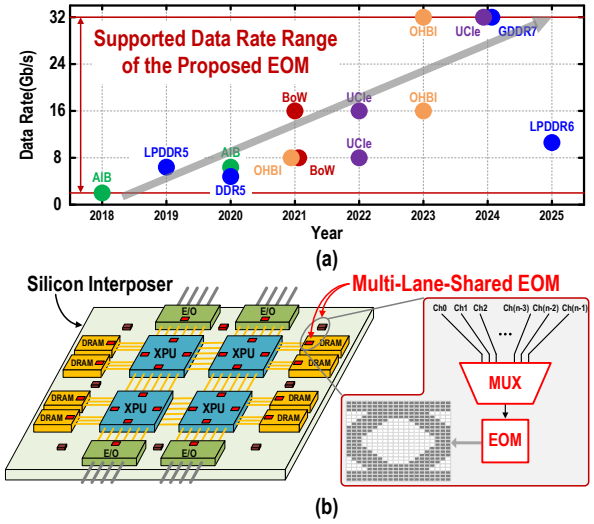

Fig. 1. (a) Trends in chiplet and memory interface standards. (b) Application of EOM in HPC scenario.

II. Circuit Implementation and Algorithmic Principles

Fig. 2 illustrates the overall architecture of the proposed EOM, where a 6-bit digital-to-analog converter (DAC) and an 8-bit PI collaborate to reconstruct the eye diagram in the voltage and time domains, respectively. Within the probability density function (PDF) solver, the single-ended input is routed through a MUX and converted to a differential signal by a single-ended-to-differential (S2D) stage. This differential signal drives two comparators with reference voltages separated by one DAC LSB [2]. Clocked by the PI, these comparators jointly determine signal presence within each sampling pixel. In the clock path, the quarter-rate PI provides 6-bit time resolution over one unit interval (UI), enabling a horizontal reconstruction resolution of 128 points for eye diagrams or 256 points for de-embedding. Moreover, the proposed EOM supports three conventional acquisition modes: multi-sampling mode (MSM), fast-multi-sampling mode (FMSM), and non-uniform-scanning mode (NSM) [3]. In MSM, the EOM captures a color-graded 2-D eye diagram, offering the most measurement information. In contrast, FMSM omits the time-consuming accumulation process required for color grading, thereby enabling faster reconstruction. Finally,

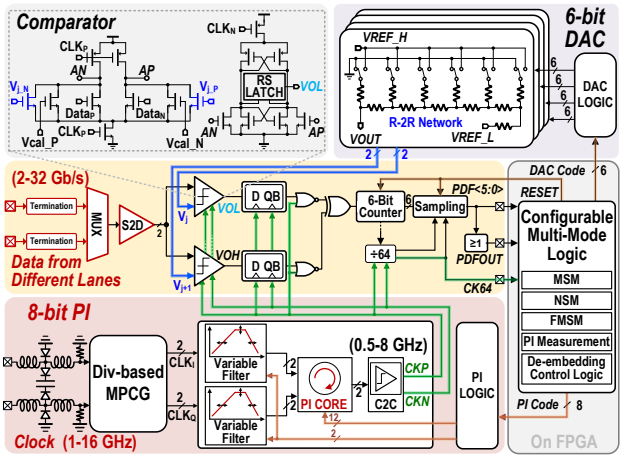

Fig. 2. Overall architecture of the proposed EOM.

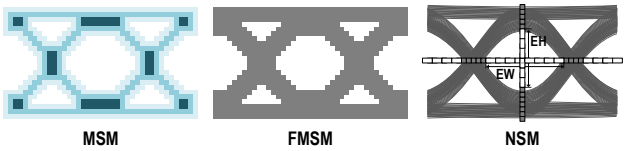

Fig. 3. Acquired eye-diagrams under three conventional acquisition modes.

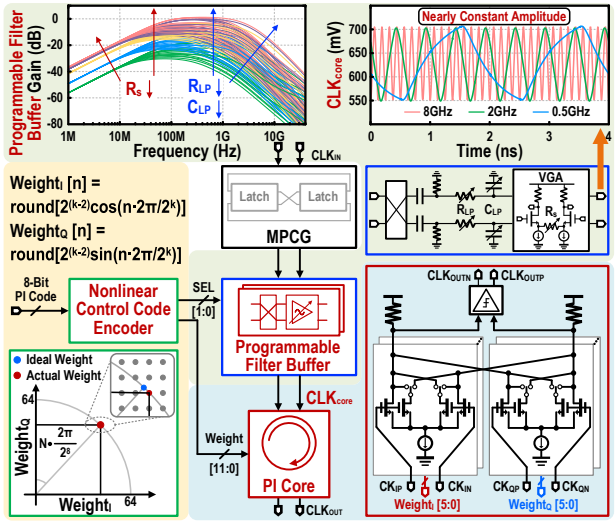

Fig. 4. Block diagram of the proposed PI with linearity enhancement techniques.

NSM directly extracts eye height (EH) and eye width (EW) information using variable search step sizes, achieving the fastest measurement speed, as illustrated in Fig. 3. Beyond these standard modes, the system also features the capability to measure the input single-bit response (SBR) for de-embedding. Additionally, the control logic governing all operational modes, including the PI measurement control program, is centrally implemented on an FPGA.

As PI is the primary factor limiting the overall operating range of the EOM, we propose a PI that operates from 0.5 to 8 GHz with a peak-to-peak INL (INL_{pp}) of less than 2.5 LSB. Fig. 4 details the architecture and its linearity enhancement techniques. The proposed design integrates balanced load interpolation cells and digital calibration to effectively suppress nonlinearity arising from circuit imperfections and systematic errors. To further extend the operating range, a programmable filter, comprising a digitally controlled filter and a variable gain amplifier (VGA), is placed before the

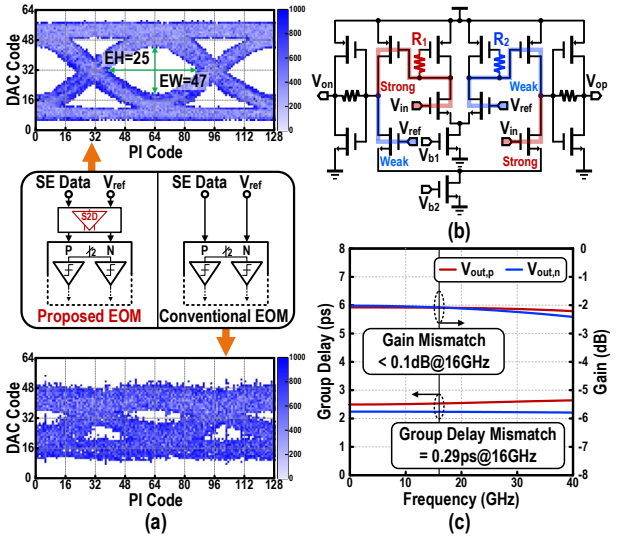

Fig. 5. (a) Comparison of the proposed single-ended EOM vs. the conventional differential EOM. (b) The schematic and (c) the simulation results of the S2D converter.

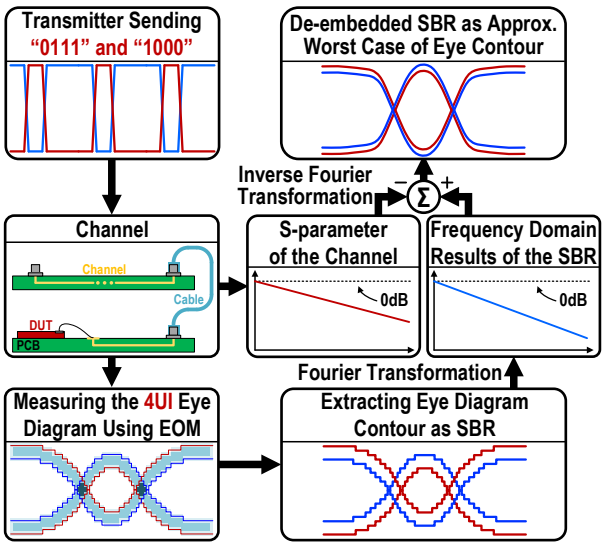

Fig. 6. Principle of de-embedding in the proposed EOM.

interpolation core. By adjusting its bandwidth and gain across different frequencies, this filter delivers signals with optimized amplitude and waveform shape to the interpolation core, thereby mitigating the impact of harmonics on interpolation accuracy, as shown in Fig. 4, top.

While a conventional differential-input EOM may directly be used to measure single-ended signals, its accuracy is significantly lower than that of the proposed approach due to the gain imbalance between the differential outputs, as shown in Fig. 5(a). In the employed S2D converter, the gain and group delay of the differential outputs are precisely tuned by adjusting R_1 and R_2, as depicted in Fig. 5(b) [4]. Simulation results demonstrate that this design exhibits a gain mismatch of less than 0.1 dB and a group delay mismatch of only 0.29 ps at 16 GHz, resulting in a significantly improved eye diagram compared with the differential EOM.

The proposed EOM employs a quarter-rate architecture. When transmitting repetitive "0111" or "1000" patterns, the

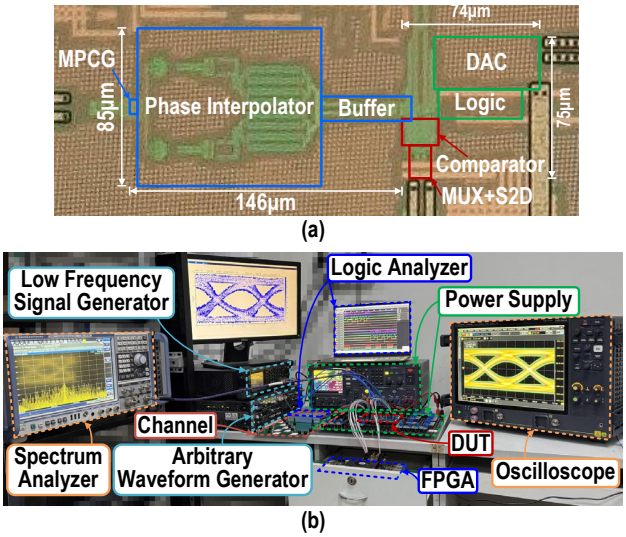

Fig. 7. (a) Die-micrograph and (b) measurement setup.

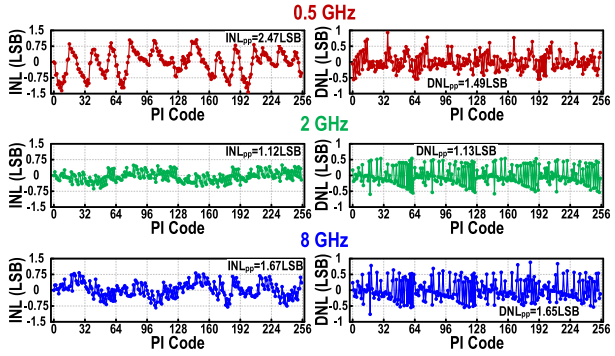

Fig. 8. Measured INL and DNL at 0.5 GHz, 2 GHz, and 8 GHz.

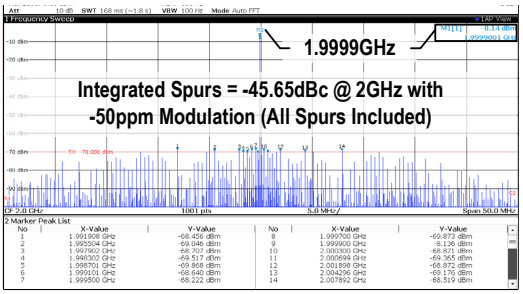

Fig. 9. Measured PI output spectrum under modulation.

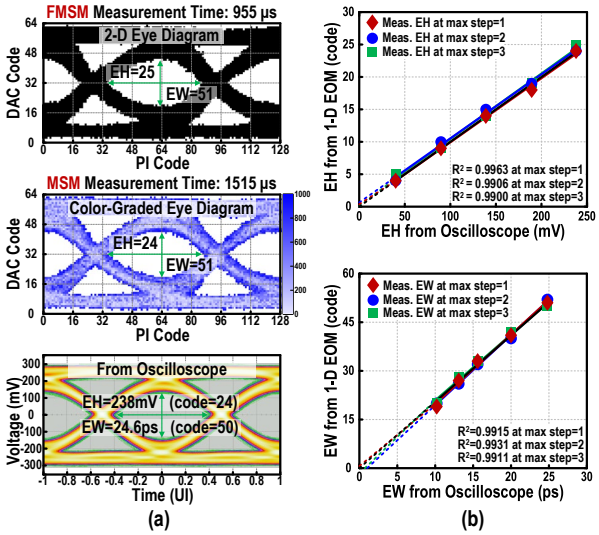

Fig. 10. (a) Reconstructed eye-diagram in FMSM and MSM versus oscilloscope at 32 Gb/s. (b) Measured EH and EW by NSM versus by the oscilloscope at 32 Gb/s with the non-uniform step size of 1, 2 and 3.

EOM captures the complete signal information over 4 UIs to approximate the SBR. This approach is justified since the channel loss in chiplet and memory interfaces is limited, enabling the 4-UI pulse response to adequately represent SBR. Furthermore, since the SBR corresponds to the eye diagram contour, we propose a de-embedding method illustrated in Fig. 6. Guided by the control logic, the EOM acquires the post-channel "0111" and "1000" patterns and extracts their contours as the SBR. This time-domain SBR is then transformed into the frequency domain via the Fourier transformation, and the channel response is removed using the measured S-parameters for de-embedding. Finally, an inverse Fourier transformation converts this result back to the time domain, yielding the de-embedded eye contour. The EOM provides 64 sampling points per UI, producing an equivalent sampling rate that is 64 times the data rate. This ensures sufficient resolution of the SBR, thereby enabling accurate frequency-domain de-embedding.

III. Measurement Results

Fig. 7(a) shows the die-micrograph of the prototype, which was fabricated in a 28-nm CMOS process and occupies a core area of 0.011 mm^2. During measurements, single-ended data and a synchronous clock were generated by an arbitrary waveform generator, as shown in Fig. 7(b).

Fig. 8 illustrates the measured INL and differential nonlinearity (DNL) of the employed PI over its entire operating range. The INL_{pp} is maintained below 2.5 LSB, and the peak-to-peak DNL (DNL_{pp}) is kept under 1.7 LSB. The best linearity is observed at 2 GHz, with an INL_{pp} of 1.12 LSB and DNL_{pp} of 1.13 LSB. Furthermore, during a linear PI code sweep that produces a −50 ppm frequency modulation at 2 GHz, the PI achieves an integrated spur of −45.65 dBc, as shown in Fig. 9. The spur performance further confirms its superior linearity, forming the foundation for EOM timing scanning.

To demonstrate the measurement accuracy in the conventional eye diagram acquisition modes, Fig. 10(a) compares the reconstructed pseudo-random binary sequence (PRBS) eye diagrams across three modes with those measured by an oscilloscope at 32 Gb/s. The EH and EW obtained in all three modes exhibit strong consistency. The eye reconstruction times under FMSM and MSM are 955 μs and 1515 μs, respectively, whereas the measurement times for EW and EH under NSM are 4.64 μs and 4.67 μs. Fig. 10(b) compares the EH and EW measured by NSM using various search step sizes against the oscilloscope references. The R^2 values for all cases exceed 0.99, indicating high measurement accuracy.

Fig. 11 comprehensively validates the SBR extraction and de-embedding capabilities of the proposed EOM at 32 Gb/s across three channels of varying lengths. Initially, as shown in Figs. 11(a) and 11(b), the comparison between the MSM and the SBR acquisition mode reveals a high consistency between the PRBS eye diagrams and those generated from continuous "0111" and "1000" patterns. This

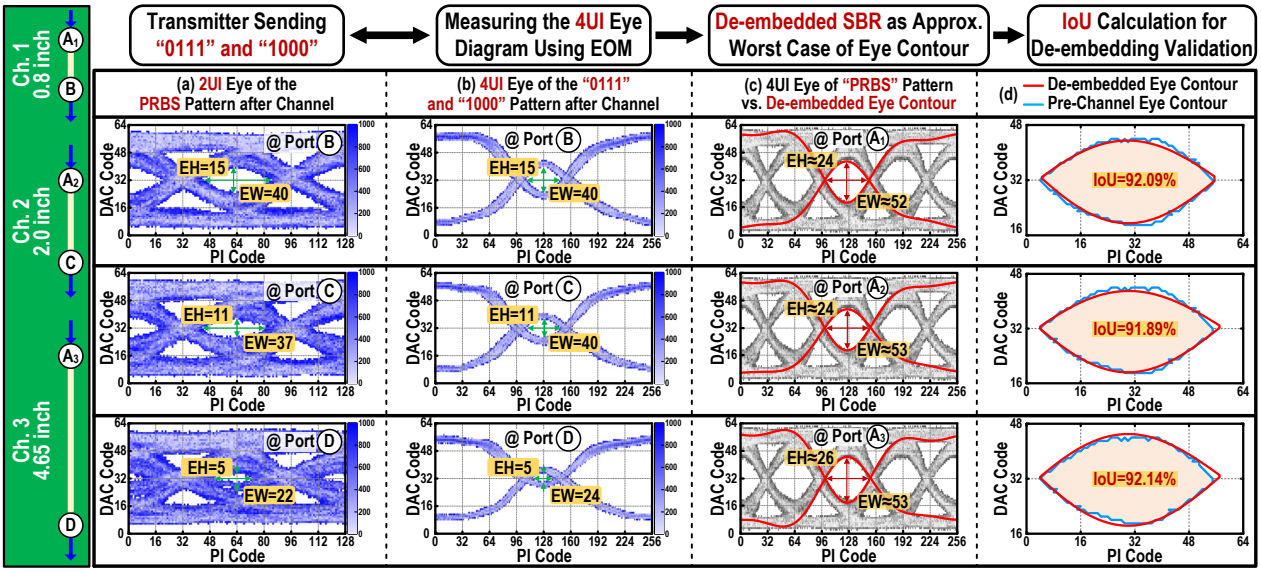

Fig. 11. Measured de-embedding performance.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

Metrics		This Work	TMTT'25 [3]	TVLSI'20 [5]	TCAS-I'17 [6]
EOM Type		1-D/2-D/ Color-Graded	1-D/2-D/ Color-Graded	1-D H	2-D
Technology		28nm CMOS	28nm CMOS	65nm CMOS	40nm CMOS
Signaling		Single-ended	Differential	Differential	Differential
Data Rate (Gb/s)		2 - 32	4 - 26	10	28
De-embedding		Yes	No	No	No
De-embedding Fidelity[a]		92%	N/A	N/A	N/A
Clock Architecture		quarter rate	half rate	one-tenth rate	quarter rate
Resolution	Phase	256	128	64	128
	Ref. Voltage	64	64	2	128
	Samples	2048	1024	1000	2048
Sampling Clock (GHz)		0.5 - 8	2 - 13	1	7
Clock INL_{pp}/DNL_{pp} (LSB)		1.67/1.65@8GHz	2.87/2.16[d]@13G	(N/A)/0.7[f]@1GHz	N/A
Operating Time (μs)	EW/EH	4.64 (EW) / 4.67 (EH)	2.90 (EW) / 3.28 (EH)	64 (EW)	N/A
	Eye Contour	955	597	N/A	4793[d]
	Color-graded	1515	933	N/A	N/A
Power (mW)		18.06 - 20.42[b]	7.2 - 14.55	1.28	3[e]
Area (mm^2)		0.011[b]	0.005	0.027[c]	0.146[d]

[a] The intersection-over-union (IoU) between the de-embedded eye contour calculated from SBR and the PRBS eye contour measured by EOM. [b] Include PI. [c] Include VTC. [d] Evaluated from paper. [e] Only include digital logic. [f] Simulation results.

strong agreement verifies the accuracy of the SBR extraction method. Building on this extracted SBR, the de-embedded eye contours are derived following the process in Fig. 6. Subsequently, Fig. 11(c) compares these de-embedded contours with the pre-channel MSM eye diagram [from Fig. 10(a)], demonstrating excellent alignment. To further quantify this performance, Fig. 11(d) evaluates the similarity between the two eye contours using the intersection over union (IoU) metric. Notably, the IoU values exceed 91% across all three channels, conclusively confirming the effectiveness of the proposed de-embedding method.

Compared with prior art, our work supports single-ended signal measurement and offers a wider operating range to support multiple standards, as summarized in Table I. Furthermore, in addition to providing three conventional acquisition modes, de-embedding is achieved to enable the EOM reuse across multiple lanes for hardware reduction.

IV. CONCLUSION

This article proposes a 2-32 Gb/s reconfigurable multi-lane-shared EOM with three conventional acquisition modes and de-embedding capabilities for single-ended high-density scenarios such as chiplet and memory interfaces. The timing information is provided by a quarter-rate 8-bit PI, which employs balanced load cells and digital calibration techniques to achieve an INL_{pp} of less than 2.5 LSB and a DNL_{pp} of less than 1.7 LSB over the entire operating range. Fabricated in 28-nm CMOS technology, the prototype occupies an area of 0.011 mm^2 and consumes 20.42 mW at 32 Gb/s. Measurement results show that the proposed EOM achieves an R^2 greater than 0.99 across all three modes, and an IoU of 92% during de-embedding for three channels of varying lengths.

ACKNOWLEDGEMENTS

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