A 13-bit 1-GS/s Pipelined-SAR ADC with Adaptive Amplification Time Calibration for an Open-Loop Integrating Amplifier

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***Abstract*—This paper presents a 13-bit 1-GS/s pipelined-SAR ADC featuring an open-loop integrating floating inverter amplifier (FIA) and on-chip background calibration. The flipped voltage follower (FVF)-based FIA achieves high linearity while suffering from inter-stage gain error (IGE) with PVT variation. Therefore, this work proposes an IGE calibration method, which detects the deviation of bit-weight ratio between two stages, and adjusts the amplification time of FIA adaptively. Fabricated in 28-nm CMOS, the prototype ADC achieves a Nyquist SNDR of 62.7 dB and SFDR of 76.3 dB, respectively. The total power is 6.02 mW, including the calibration circuit. This corresponds to a competitive FoM_S of 171.9 dB.**

***Index Terms*—Pipelined-SAR ADC, gain error calibration, floating inverter amplifier, analog correction**

I. Introduction

Pipelined-SAR ADCs have emerged as a promising architecture for wireless communication and instrumentation applications, as they combine the speed advantage of pipeline and the low power of SAR architectures [1]–[3]. The residue amplifier (RA) is a critical building block in pipelined-SAR ADCs and often becomes the bottleneck in terms of conversion speed, power consumption, and robustness. Compared to power-hungry closed-loop amplifiers, open-loop amplifiers stand out for high speed and power efficiency. However, inter-stage gain error (IGE) and nonlinearity result in significant calibration overhead.

Typically, IGE mainly results from RA and can be corrected in digital or analog ways. As shown in Fig. 1, digital correction eliminates transfer function discontinuities by fitting bit weights or digital gain [4]. However, it encounters resolution loss and consumes considerable power running at full speed [5]. In contrast, analog correction directly adjusts the RA, thereby eliminating the gain error intrinsically without resolution loss. In this work, an adaptive amplification time (AAT) calibration is proposed. By tuning the amplification time of the integrating RA, the amplifier gain is driven to converge to the weight ratio of the second-stage MSB to the first-stage LSB. The on-chip background IGE calibration consumes 0.46 mW and occupies 884 μm^2, which accounts for only 7.6% and 6.5% of the total, respectively.

To address the nonlinearity of RA, an open-loop integrating floating inverter amplifier (FIA) is proposed, which employs a flipped voltage follower (FVF) as the G_m cell. It achieves a robust dynamic performance under PVT variation without calibration.

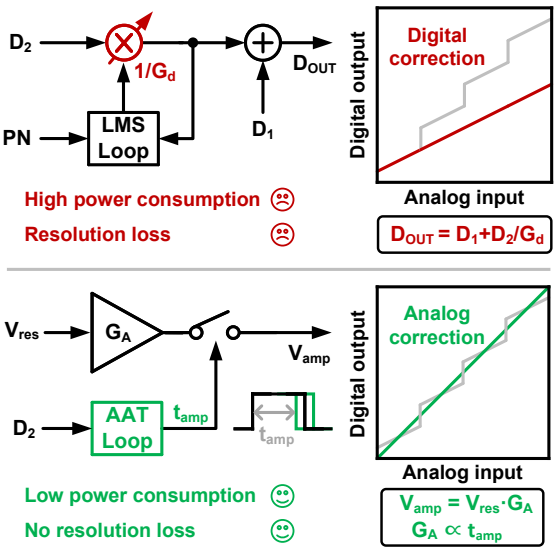

Fig. 1: Comparison of the digital IGE calibration and proposed AAT calibration.

With the proposed open-loop FIA and AAT calibration, a 13-bit 1-GS/s pipelined-SAR ADC prototype is implemented in a 28-nm CMOS. It achieves an SNDR of 62.7 dB and SFDR of 76.3 dB with Nyquist input while consuming 6.02 mW, resulting in a Schreier FoM of 171.9 dB.

II. Pipelined-SAR ADC Architecture and Implementation

The block and timing diagrams of the proposed two-stage 13-bit 1-GS/s pipelined-SAR ADC are shown in Fig. 2. It consists of a 5-bit sub-range SAR ADC and 9-bit 2-way time-interleaved (TI) SAR ADC as the first and second stages, where 1-bit redundancy is inserted to tolerate inter-stage error and noise. The open-loop RA realizes an 8× gain with the second stage reference scaling.

In the first stage, the sampling capacitance of the main capacitive DAC (CDAC) is 800 fF by considering thermal noise and mismatch, while the sub-SAR CDAC is 40 fF to improve the settling speed. To further enhance the conversion

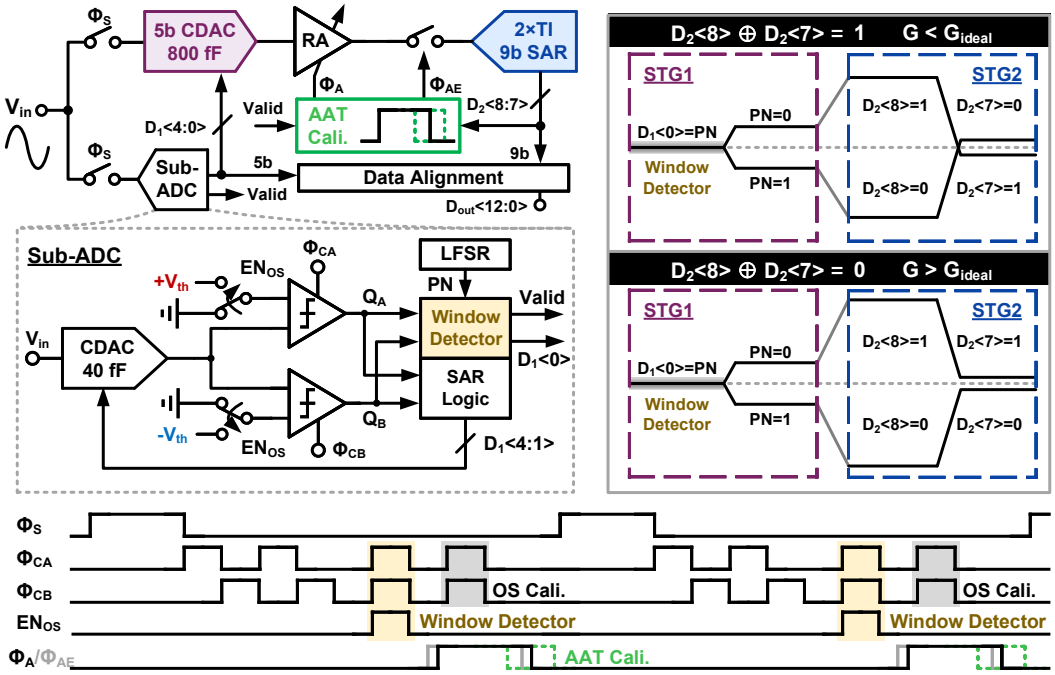

Fig. 2: Block and timing diagrams of the proposed pipelined-SAR ADC and IGE detection principle.

speed, the sub-SAR employs two ping-pong comparators, which resolve the 4 MSB ($D_{1,<4:1>}$) alternately. For the LSB ($D_{1,<0>}$), opposite polarity offsets ($\pm V_{\rm th}$) are injected into the two comparators to form a window detector. When the residue is detected within the window, the comparison results are selected by a pseudo-random noise (PN) sequence which is generated by a linear feedback shift register (LFSR). After the LSB conversion, the RA is activated to amplify the residue, while the ping-pong comparators offsets are removed in parallel by shorting the sub-SAR input. The XOR result of the 2 MSB ($D_{2,<8:7>}$) in the second stage controls a charge pump to update the RA integration time adaptively.

A. Adaptive Amplification Time Calibration

In SAR ADCs, the bit weight is determined by the capacitor ratio and reference voltage, which is expressed as:

$$W_i = \frac{C_i}{C_{\rm tot}} \cdot V_{\rm ref} \tag{1}$$

where C_i is the i-th capacitor, $C_{\rm tot}$ is the total capacitance, and $V_{\rm ref}$ is the reference voltage. In a two-stage pipelined-SAR ADC with 1-bit redundancy, assuming an ideal inter-stage gain, the input swing of the second stage should be half of the ADC full input range. This implies that the weight of the first-stage LSB, after multiplied by the RA gain, equals the weight of the second-stage MSB, which can be expressed as:

$$W_{\rm MSB2} = G_{\rm ideal} \cdot W_{\rm LSB1} \tag{2}$$

where $G_{\rm ideal}$ denotes the ideal amplifier gain. Fig. 2 illustrates the proposed IGE detection principle. Assuming that the input is zero during the comparison of first-stage LSB, the absolute value of the residue voltage equals the first-stage LSB weight $W_{\rm LSB1}$. Subsequently, the amplified residue is sampled by the second stage, where the residue voltage is reduced to $G \cdot W_{\rm LSB1} - W_{\rm MSB2}$ after MSB conversion. If the actual RA gain is larger than $G_{\rm ideal}$, the polarities of the 2 MSB in the second stage ($D_{2,<8>}$ & $D_{2,<7>}$) are identical; otherwise, they are opposite if the actual gain is smaller than $G_{\rm ideal}$. Therefore, the IGE can be identified by an XOR gate of the 2 MSB in the second stage.

However, due to interference introduced by the input signal, calibration is activated only when the input is small. Therefore, a window detector is employed during the first-stage LSB comparison. Once the input signal falls within the window detector, one of the comparator outputs is selected by a PN code. To improve the accuracy and stability of the AAT calibration, offset mismatch of the second-stage comparators and RA should be removed, which is realized by monitoring the second-stage MSB distribution in background [6].

The schematic of the proposed AAT calibration is shown in Fig. 3. If Q_A and Q_B are opposite in the first-stage LSB comparison, window detector will generate an enable signal (Valid). The calibration logic then controls a charge pump to tune the calibration voltage ($V_{\rm CAL}$) based on the result of $D_{2,<8>}$ XOR $D_{2,<7>}$. The calibration voltage adjusts the slope of the ramp signal $V_{\rm T}$ in the timing generator, thereby tuning the amplification time of RA. The tuning time range is set as $\pm$40 ps to cover an IGE of $\pm$10%.

Fig. 4 shows the IGE before and after AAT calibration across PVT variation. It shows that the maximum IGE is reduced from -7.3% to 0.34% after calibration, resulting in

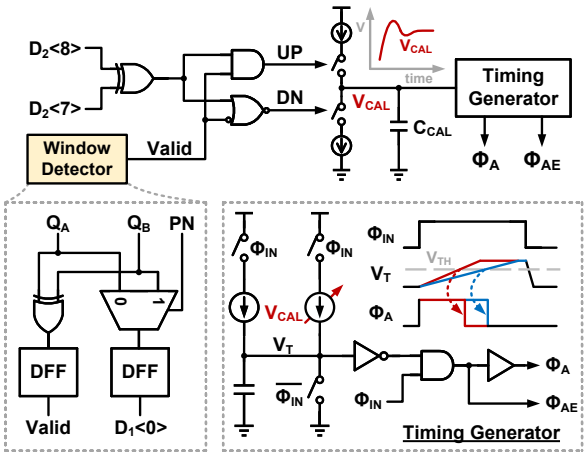

Fig. 3: Schematic of the proposed AAT calibration.

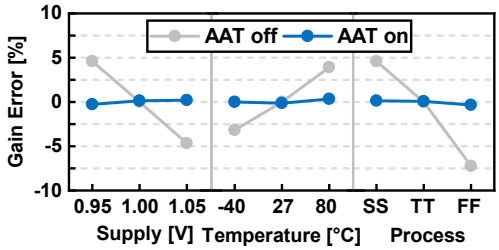

Fig. 4: Gain error across PVT variation before and after calibration.

an SNDR improvement of 13.4 dB. Note that random jitter can affect the calibration accuracy by modulating Φ_A. The simulated rms jitter of Φ_A is 0.6 ps, which is much smaller than its nominal pulse width of 250 ps. Therefore, the presence of jitter has minor impact on the calibration accuracy.

B. Open-loop FVF-based FIA

Fig. 5(a) illustrates the schematic of the proposed open-loop integrating FIA, where a complementary FVF-based G_m cell improves the linearity compared to using an inverter input stage [7]. Additionally, level-shifting capacitors are employed at the input to split the DC bias, which alleviates the voltage headroom. Integration-based amplification relaxes the bandwidth requirement to achieve an 8× gain, and the FIA structure eliminates the need for common-mode feedback (CMFB). Fig. 5(b) and (c) show the simulated total harmonic distortion (THD) of the amplifier versus supply variation and input signal swing under different conditions. It confirms that THD is better than -55 dB and satisfies the backend stage linearity requirement even under the worst PVT condition.

III. Measurement Results

Fabricated in a 28-nm CMOS process, the prototype ADC occupies 0.014 mm^2, as shown in Fig. 6(a). Under a 1-V supply, the ADC core consumes 6.02 mW operating at 1 GS/s, including the on-chip AAT calibration circuit. The power breakdown is shown in Fig. 6(b). Capacitor weights

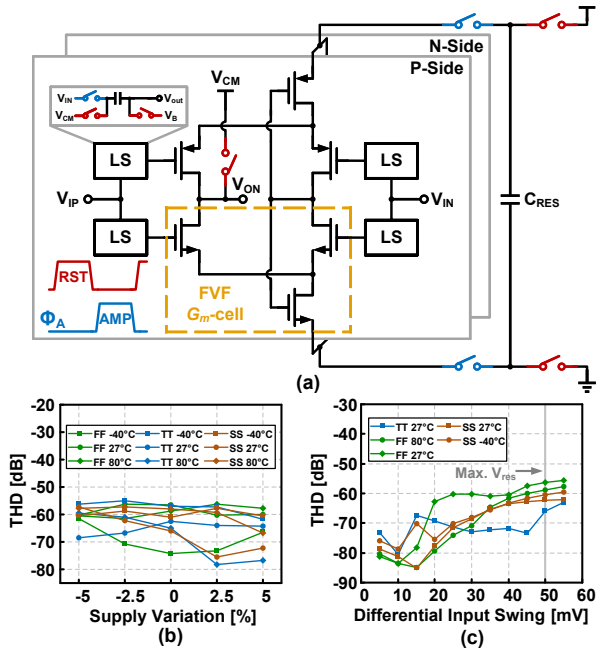

Fig. 5: (a) Schematic of the FVF-based FIA. Simulated THD versus (b) supply variation and (c) input swing.

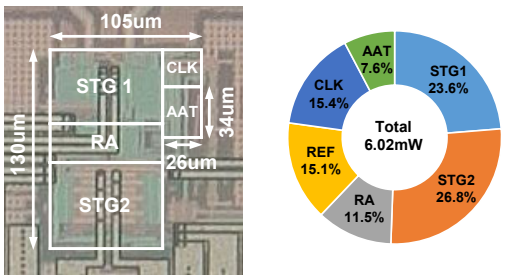

Fig. 6: Die photo and power breakdown of the ADC.

and channel mismatch in the backend TI-SAR are one-time calibrated and fixed in measurements afterward.

Fig. 7(a) and (b) show the measured spectra at low and Nyquist frequency with 1.6-V_{PP} inputs, respectively. The measured SNDR/SFDR after calibration are 63.1/79.2 dB at 57.5 MHz and 62.7/76.3 dB at Nyquist inputs, respectively. Fig. 8 shows the measured DNL and INL after calibration, which are within +1.31/-0.95 and +1.51/-1.85 LSB, respectively.

Fig. 9 illustrates the SNDR and SFDR versus input frequency at 1 GS/s, and sampling rate with 200 MHz input frequency. To verify the robustness of the ADC, 3 randomly selected samples are measured with ambient temperature and supply voltage variations. With the AAT calibration enabled, the SNDR fluctuates less than 3.2 and 2.6 dB, respectively, as shown in Fig. 10.

Table I summarizes the performance of the proposed ADC and compares it with recently published 12-to-14-bit ADCs. With open-loop FVF-based FIA and AAT calibration, the prototype ADC achieves Schreier FoM_S and Walden FoM_W of

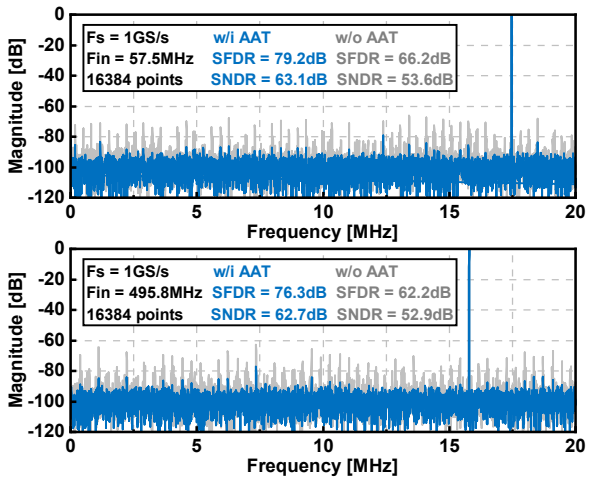

Fig. 7: Measured output spectra (decimated by 25).

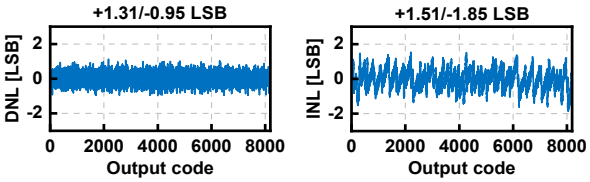

Fig. 8: Measured DNL and INL after calibration.

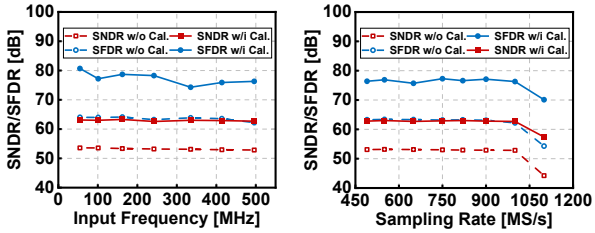

Fig. 9: Measured SNDR and SFDR versus input frequency and sampling rate.

171.9 dB and 5.4 fJ/conv.-step, respectively, which are in-line with the state-of-the-art works.

IV. Conclusion

This work proposes an open-loop integrating FIA and adaptive amplification time calibration for IGE in pipelined-SAR ADC. The calibration detects the deviation of bit-weight ratio between the first and second stages, and adjusts the amplification time of RA, which corrects IGE effectively with low hardware cost. The proposed FVF-based FIA exhibits robust linearity across PVT variation with superior energy efficiency. Thanks to the two novel techniques, the 13-bit 1-GS/s ADC prototype achieves a robust performance and a competitive Schreier FoM of 171.9 dB.

Acknowledgment

This work was supported by the National Key Research and Development Program of China (2023YFB4403303), and National Natural Science Foundation of China (62422406).

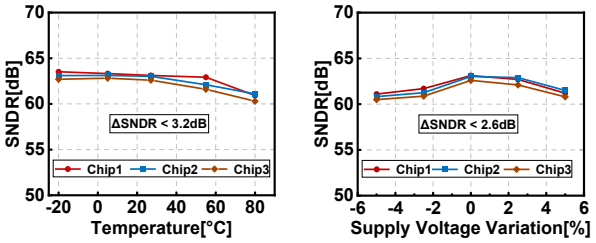

Fig. 10: Measured SNDR versus temperature and supply variations with 3 samples.

TABLE I: Performance Summary and Comparison

	This Work	ISSCC 2023 [2]	VLSI 2024 [7]	CICC 2022 [1]	JSSC 2023 [3]
Architecture	**Pipe-SAR**	Pipe-SAR	Pipe-SAR	Pipe-SAR	Pipe-SAR
RA Type	**OL FIA**	CL Ringamp	CL Ringamp	OL Inverter	CL FIA
Process	**28nm**	28nm	22nm	40nm	28nm
Resolution [bit]	**13**	12	13	13	14
Fs [MS/s]	**1000**	1000	475	625	500
Supply [V]	**1.0**	1.0	1.0	1.1/1.2	1/1.2
Area [mm^2]	**0.014**	0.016	0.038	0.022	0.018
Power [mW]	**6.02**	6.9	9.93	7.05	6.34
SNDR @Nyq. [dB]	**62.7**	62.5	65.9	62.4	64.2
SFDR @Nyq. [dB]	**76.3**	80.5	73.0	70.0	80.5
FoM_S [dB]	**171.9**	171.1	169.7	168.9	170.2
FoM_W [fJ/step]	**5.4**	6.3	13.0	10.5	9.6
IGE Calibration	**BG**	BG	BG	FG	FG
	On-chip	Off-chip	On-chip	Off-chip	On-chip

OL: Open-loop CL: Closed-loop BG: Background FG: Foreground

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