A 3-19 GHz Injection-Locked Clock Multiplier with Optimal Edge Frequency Tracking Loop Achieving 131 fs_{rms} jitter and −74 dBc Injection Spur

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***Abstract*—This paper presents a ring-oscillator-based injection-locked clock multiplier (ILCM) operating from 3 GHz to 19 GHz, achieving an RMS jitter of 131 fs at the center frequency of 10 GHz and a minimum RMS jitter of 94 fs at 12 GHz, and an injection spur of −74 dBc. The injection spur is suppressed by the proposed frequency tracking loop (FTL), which corrects the output frequency precisely at an optimal edge, avoiding the injection-induced frequency fluctuation. This is ensured by Primary DLL, Optimal Edge Search, and Injection Edge Calibration. Additionally, low jitter at high output frequencies is realized by controlling the injection frequency according to the output frequency.**

Keywords—Injection-Locked Clock Multiplier (ILCM), PLL, Ring Oscillator, Spur Suppression

I. Introduction

Wide frequency range PLLs are required for wireline and wireless communications supporting multiple standards. Ring-oscillator-based PLLs offer a wide frequency range, small area, and process scalability; however, they suffer from poor jitter. To suppress jitter, a cascaded PLL, consisting of a 1st LC-oscillator-based PLL (LC-PLL) and a 2nd ring-oscillator-based PLL (RO-PLL), is an effective approach. Since the 2nd RO-PLL is generally the dominant contributor to overall jitter performance in cascaded PLLs, this paper focuses on improving the 2nd RO-PLL's performance.

Using a ring-oscillator-based ILCM (RO-ILCM) for the 2nd RO-PLL enables further jitter reduction. However, spurs arise when the oscillator's free-running frequency is not equal to an integer multiple of the injection frequency. To address this issue, several frequency correction methods for ILCMs have been proposed [1-6]. Since the ILCM in [6], shown in Fig. 1, implements a Digitally-Controlled Delay Line (DCDL) in the REF signal path, the operating frequency of the DCDL is reduced, and its jitter is suppressed by the loop dynamics. Therefore, this architecture is suitable for a wide frequency range and low-jitter ILCM. The delay locked loop (DLL) synchronizes the REFD and OUT phases. The FTL corrects frequency error by detecting phase drift Δϕ through intermittent injection gating when GATE is high.

As shown in Fig. 2 (top), even though the oscillator's free-running frequency is at the target value, the output frequency fluctuates immediately after injection. Therefore, when the frequency is corrected by the FTL at the edge of OUT just after injection, which is the non-optimal edge, the time-to-digital converter (TDC) detects undesired phase errors, resulting in increased frequency error and spurs.

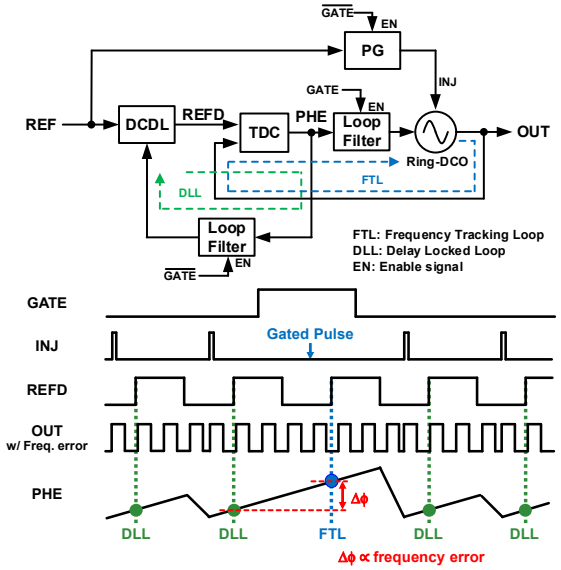


Fig.1. Block diagram of a conventional ILCM and frequency correction method [6].

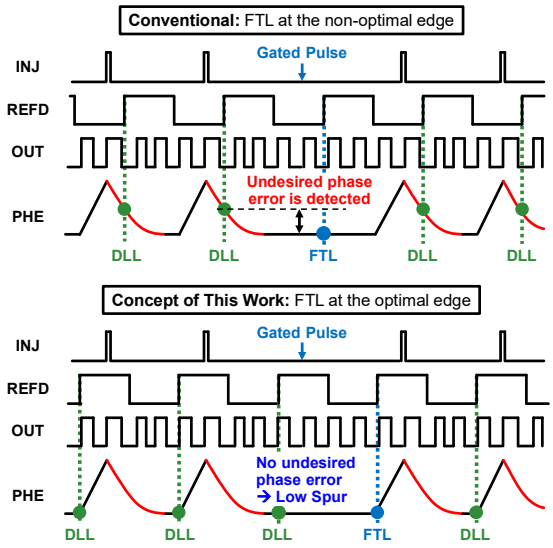


Fig. 2. The impact of the phase error due to injection-induced frequency fluctuation on FTL.

Fig. 2 (bottom) shows the concept of this work. By correcting the frequency at the edge of OUT just prior to injection, which is the optimal edge, the impact of injection-induced frequency fluctuation is mitigated. As a result, undesired phase error detection is avoided, and the spur is suppressed.

Additionally, a trade-off exists between the injection frequency of the 2nd RO-ILCM and the frequency tuning range (FTR) of the 1st LC-PLL in wide frequency range cascaded PLLs. At high output frequencies, jitter increases due to injection strength β reduction for two reasons: (1) increased bias current I_{BIAS} of the DCO for higher oscillation frequency ($\beta \propto 1/I_{BIAS}$) (2) difficulty in adjusting the optimal injection pulse width, which is one-quarter of the oscillation period [7]. While higher injection frequency reduces jitter, it results in a smaller minimum multiplication ratio N_{min} between injection and output frequencies for the 2nd RO-ILCM. This results in an expanded FTR specification ($=1/(2N_{min}+1)$) for the 1st LC-PLL, which degrades its jitter performance.

II. Proposed Injection-Locked Clock Multiplier

A. Optimal Edge Frequency Tracking

Fig. 3 shows the block diagram of the proposed RO-ILCM that realizes the concept shown in Fig. 2 (bottom). It consists of an RO-based digitally-controlled oscillator (DCO), a pulse generator (PG), a replica PG with the same delay as the PG, a TDC, a DCDL, a divider (DIV) with a multi-phase generator (MPG), a bang-bang phase detector (BBPD), loop filters, multiplexers (MUXs), a control block (CTRL), and a counter-based frequency acquisition loop that is disabled after the initial acquisition.

To correct the output frequency precisely, an optimal edge is searched using the following procedure. First, the DCO is roughly tuned to the target frequency by the counter-based frequency acquisition loop and the PG output pulse INJ is injected to the DCO. Then, 'Primary DLL' shown in Fig. 4 aligns the DCDL output REFD to the replica PG delay output REPINJ with SEL set to 0 from CTRL. Next, 'Optimal Edge Search' shown in Fig. 5 is performed with SEL set to 1. The DCDL control code is decreased by setting the loop filter input to a fixed value (e.g., −1), causing the REFD edge to lead INJ. The decrement of the DCDL code continues until the edge of OUT just prior to injection is detected by CTRL, which monitors the TDC output signal PHE. The MPG followed by a 16-to-1 MUX extends the delay control range of REFD to one period of REF. When the DCDL control code reaches saturation, CTRL selects another phase from the MPG. Finally, SEL is set to 2 as shown in Fig. 3. The frequency is corrected when GATE from CTRL is high, avoiding undesired phase error detection as shown in Fig. 2 (bottom).

B. Injection Edge Calibration

The DCO shown in Fig. 6 employs a differential three-stage ring oscillator. For successful operation of Primary DLL and Optimal Edge Search, INJ needs to be aligned to the rising edge of OUT_{000}. However, the DCO can be locked to either the rising edge or falling edge of OUT_{000}. Therefore, we propose a calibration to ensure that INJ is aligned to the rising edge of OUT_{000}. The calibration is performed in two steps. In the 1st step, INJ is connected to the gates of M1 and M2, which pull OUT_{060} and OUT_{120} down to ground level. Under this condition, the timing of INJ becomes close to the rising edge of OUT_{000}. In the 2nd step, INJ is connected to the gate of M3, which shorts the differential nodes OUT_{000} and OUT_{180}, and INJ is thereby aligned to the rising edge of OUT_{000}.

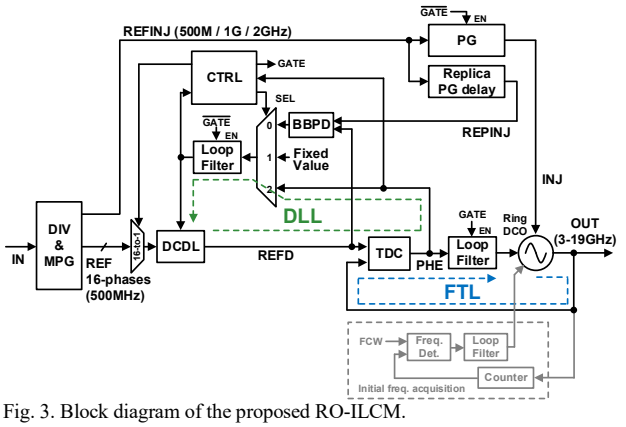


Fig. 3. Block diagram of the proposed RO-ILCM.

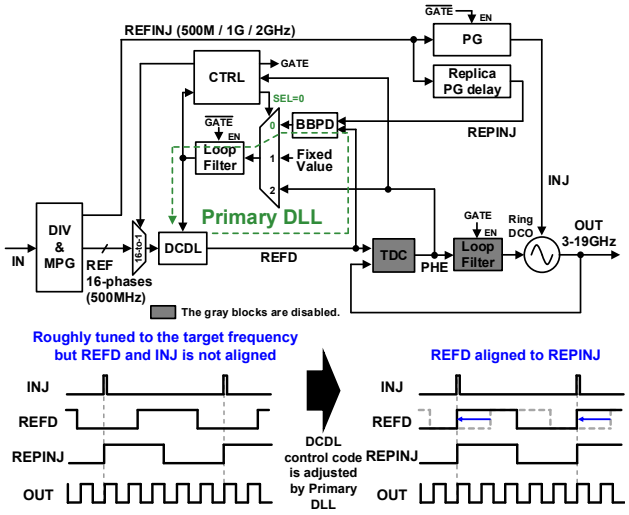


Fig. 4. Operation of Primary DLL: REFD is aligned to REPINJ.

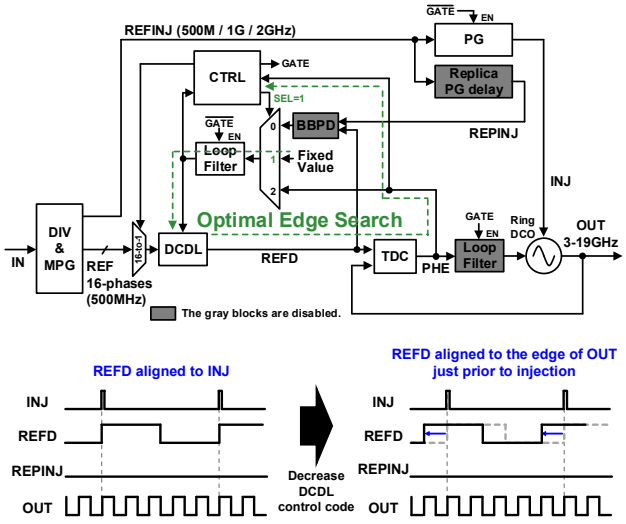


Fig. 5. Optimal Edge Search: REFD is aligned to edge of OUT just prior to injection.

C. Injection Frequency Control

To address the trade-off between the injection frequency of the 2nd RO-ILCM and the FTR specification of the 1st LC-PLL, the injection frequency is controlled to be as high as possible while maintaining N_{min} that achieves an FTR ensuring sufficiently small jitter of the 1st LC-PLL.

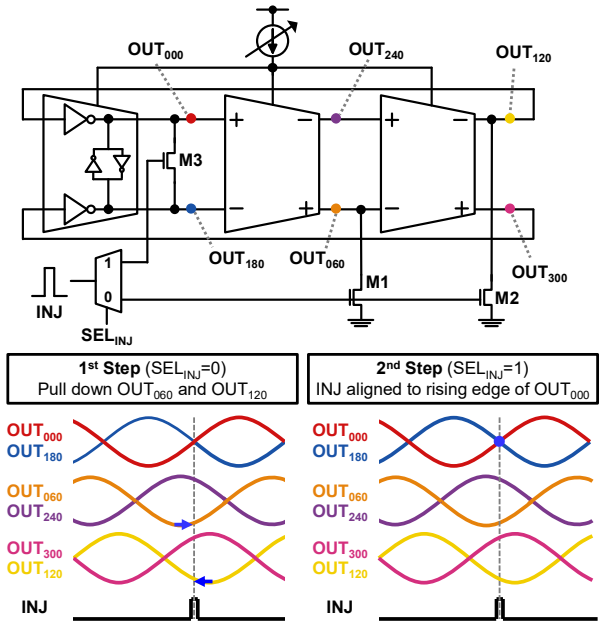


Fig. 6. Block diagram of DCO and operation of injection edge calibration.

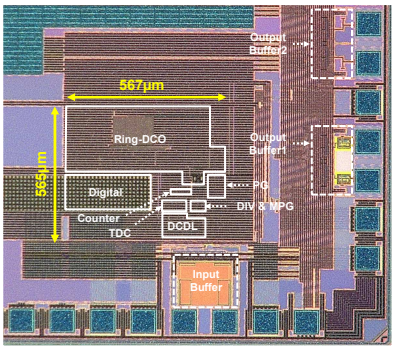
This approach achieves low jitter at high output frequencies and maintains an appropriate FTR for the 1st LC-PLL. In this design, N_{min} is set to 6, and the injection frequency is selectable as 1×, 2×, or 4× the REF frequency.

III. Measurement Results

Fig. 7 shows the proposed RO-ILCM fabricated in a 12 nm CMOS process. The active area is 0.21 mm² and the measured power consumption is 13.06 mW, excluding input/output buffers. In the measurements, a signal generator replaced the 1st LC-PLL output. Fig. 8 shows the phase noise measured at the divide-by-4 output of the 10 GHz RO-ILCM (2.5 GHz), achieving an RMS jitter of 131 fs with an injection frequency of 1 GHz. Fig. 9 shows the RO-ILCM RMS jitter over an output frequency range from 3 GHz to 19 GHz. By controlling the injection frequency, low jitter is achieved at high output frequencies in contrast to fixed injection frequency operation, achieving a minimum RMS jitter of 94 fs at 12 GHz output. Fig. 10 shows the output spectrum measured at the divide-by-4 output of the 10 GHz RO-ILCM (2.5 GHz), with FTL at the optimal and non-optimal edges. The injection spur is −53 dBc at the non-optimal edge, while it is reduced to −74 dBc at the optimal edge, achieving a 21 dB improvement. Fig. 11 shows the injection spur over an output frequency range from 3 GHz to 19 GHz. The injection spur is suppressed over a wide frequency range by frequency correction at the optimal edge. Table I compares this work with state-of-the-art RO-PLLs. This work achieves the widest frequency range and the best FoM_T among RO-PLLs. Furthermore, it achieves lower injection spur compared to other RO-ILCMs and the RO-MDLL.

IV. Conclusion

This paper presents an RO-ILCM for the 2nd RO-PLL in a wide frequency range cascaded PLL, achieving an output frequency range of 3 GHz to 19 GHz, an RMS jitter of 131 fs at the center frequency of 10 GHz and a minimum RMS jitter of 94 fs at 12 GHz, and an injection spur of −74 dBc.



Power Consumption [mW]	
Ring-DCO	4.24
TDC	1.21
DIV & MPG	1.56
PG	0.28
Other Analog Blocks	0.74
Digital	5.03
Total	13.06

Fig. 7. Die micrograph and power consumption breakdown.

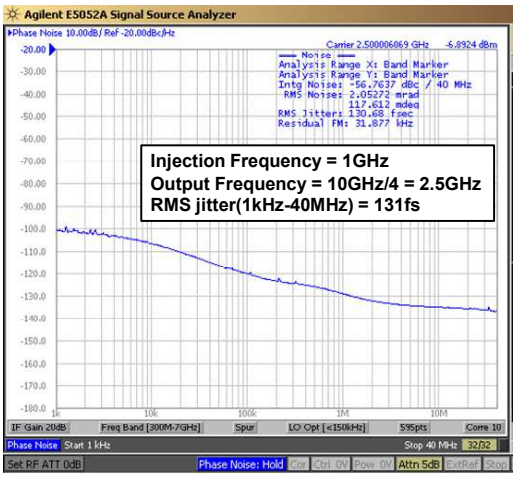


Fig. 8. Measured RO-ILCM phase noise.

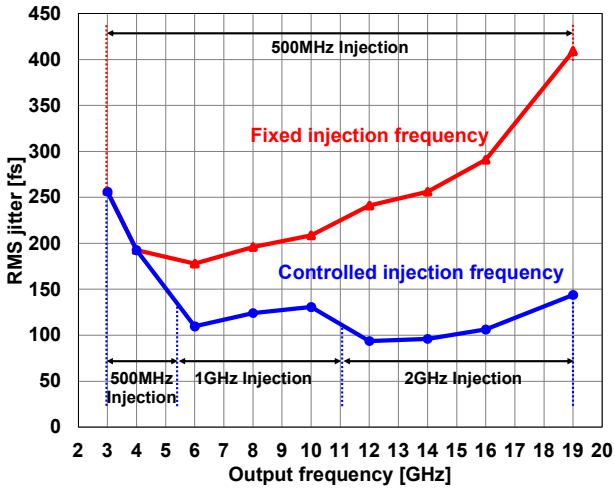


Fig. 9. Measured RO-ILCM RMS jitter over an output frequency range from 3 GHz to 19 GHz.

Using Primary DLL, Optimal Edge Search, and Injection Edge Calibration, frequency correction at the optimal edge is achieved. Consequently, undesired phase error detection is avoided, and the injection spur is suppressed. Furthermore, the injection frequency is controlled to be as high as possible while maintaining N_{min} that achieves an FTR ensuring sufficiently small jitter of the 1st LC-PLL. This approach achieves low jitter at high output frequencies.

TABLE I. Comparison with state-of-the-art RO-PLLs.

	This Work	ISSCC'22 T. Tsai [1]	VLSI'25 Z. Xu [2]	VLSI'24 D. Park [3]	ISSCC'22 S. Park [4]	ISSCC'22 H. Kim [5]	ISSCC'24 M. Khalil [8]
Technology [nm]	12	5	22	40	65	40	22
Architecture	RO-ILCM	LC-ILCM +RO-ILCM	LC-DPLL +RO-ILCM	RO-MDLL	RO-ILCM	RO-ILCM	RO-APLL
Ref. Frequency [MHz]	500*	217.5	38.4	250	120	100	812.5
Output Frequency [GHz]	10	13.92	10	4	8.16	8	13
Output Frequency Range [GHz]	**3-19**	4-17.5	3-15.5	4-5	7.68-8.52	6.4-9.9	6.8-14
FTR [%]	**145.5**	125.6	135.1	22.2	10.4	42.9	69.2
Ref. Spur [dBc]	-61 (-49)**	-72 (-60)**	-	-54	-55	-68	-62
Injection Spur [dBc]	**-74 (-62)****	-	-59			-61	-
Power [mW]	13.1	19.7	6.34	13.3	14.3	12.1	84.9
RMS Jitter [fs]	131	204	621	94	97	177	69
Integration Range [Hz]	1k-40M	100k-100M	10k-500M	1k-40M	1k-100M	10k-90M	10k-100M
FoM [dB]	-247	-241	-236	-249	-249	-244	-244
FoM_T [dB]	**-248**	-242	-237	-243	-239	-241	-242
Active Area [mm^2]	0.21	0.13	0.23	0.045	0.102	0.065	0.125

FTR = (Max Freq. – Min Freq.)/Center Freq. FoM = $10\log_{10}((\text{Jitter}/1[s])^2 \times (\text{Power}/1[mW]))$ $FoM_T = FoM+10\log_{10}(1/FTR)$

*Frequency tracking Ref. Freq. **Normalize Spur to the Output Freq, e.g. +20log(DIV ratio)

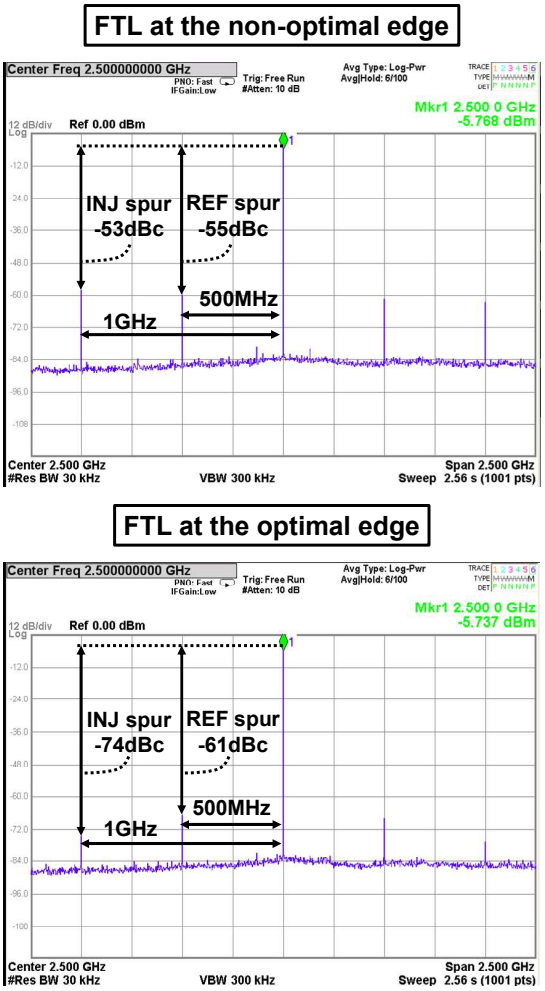


Fig. 10. Measured RO-ILCM output spectrum with FTL at the optimal edge and non-optimal edges.

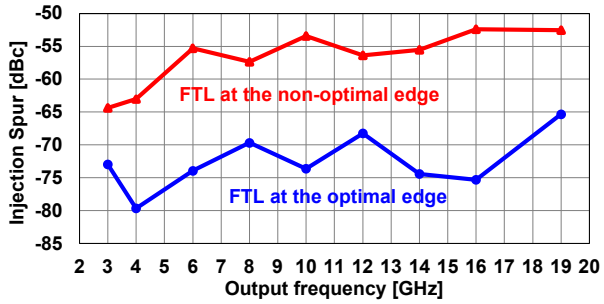


Fig. 11. Measured RO-ILCM injection spur over an output frequency range from 3 GHz to 19 GHz.

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