A 3.0 pJ/b 112 Gb/s Wireline Transceiver with 5-tap DSP-Based TX and Dual-PD-Mode RX in 28-nm CMOS

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***Abstract*—In this paper, we propose a 112 Gb/s TRX with a 5-tap, 7-bit DSP-based TX and analog-based RX. Compared to analog-based TRXs, the proposed TRX offers enhanced equalization capability while eliminating the power- and area-intensive ADC. A discharge enhancement technique and a low-output-skew DAC technique are proposed in TX. A dual-mode phase detector is proposed in CDR to support both the Mueller-Muller phase detector and the assisted bang-bang phase detector, while enabling an edge-sampling calibration with minimal hardware and power overhead. An adaptive threshold scheme is proposed to enable automatic tracking of optimal decision levels. A high-performance clock distribution technique with a tunable inductance network is proposed in the clock path to enable compensation for load capacitance across different frequencies and save power. Fabricated in a 28 nm CMOS process, the proposed TRX achieves a 13.7 dB channel loss compensation with a power efficiency of 3.0 pJ/bit.**

Keywords—DSP, phase detector (PD), threshold adaptive, transceiver (TRX), wireline.

I. Introduction

The growing need for high-speed wireline transmission has driven the data rate to exceed 100 Gb/s per lane. The analog-based architecture is recognized for its advantages in area and power efficiency. However, for TRXs operating beyond 100 Gb/s, stringent timing constraints in the FFE and DFE of analog RXs lead to significantly increased power consumption. To address this, analog RXs without FFE and DFE have been developed for XSR applications. For short-to-medium reach scenarios, stronger equalization is required. The ADC-DSP-based TRX architecture is utilized for applications with high channel loss. However, the power- and area-intensive ADC and the subsequent DSP significantly increase the system costs.

In this work, we present a 112 Gb/s TRX with a 5-tap, 7-bit DSP-based TX and analog-based RX. Compared to analog-based TRXs, the proposed TRX offers enhanced equalization capability while eliminating the power- and area-intensive ADC. A discharge enhancement technique and a low-output-skew DAC technique are proposed in TX. A high-speed, high-accuracy track-and-hold (TAH) technique is proposed in RX. A dual-mode-PD is proposed in CDR to support both Mueller-Muller (MM) PD and MMPD-assisted bang-bang (BB) PD, while enabling an edge-sampling calibration with minimal hardware and power overhead. An adaptive threshold scheme is proposed to enable automatic tracking of optimal decision levels. A high-performance clock distribution technique with a tunable inductance network is proposed to enable compensation for load capacitance across different frequencies and save power. Fabricated in a 28 nm CMOS process, the proposed TRX achieves a 13.7 dB channel loss compensation with a power efficiency of 3.0 pJ/bit.

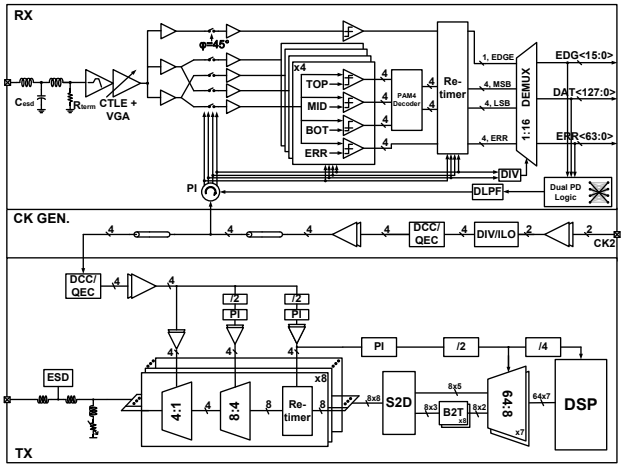

Fig. 1. The architecture of the proposed TRX.

II. Architecture of the Proposed TRX

Fig. 1 shows the architecture of the proposed TRX. In the DSP-based TX, parallel data are generated from PRBS generators and converted into 64x7b data streams by an LUT in the on-chip DSP. The coefficients and the polarities of the 5-tap LUT-based FFE are configurable [1]. After 64:8 serialization, the 2 MSBs are converted into 3 thermometer-coded bits for matching considerations. The resulting 8x8b data are converted to differential signals and serialized by 8:4 serializers. The final 4:1 output stage comprises 1-UI pulse generators and a cascode driver array.

In the analog-based RX, the CTLE and VGA are implemented to provide frequency-domain equalization. 5 track-and-hold paths, 4 for data and 1 for edge, are driven by 3 buffers for isolation considerations. Each data path includes four slicers, three for data detection and one for error monitoring. The recovered data are decoded using a PAM-4 decoder. Edge information is captured by a dedicated slicer in the edge path. After signal retiming, the edge, data, and error signals are deserialized using 1:16 deserializers for subsequent DSP processing. PD is performed using either BB logic or MM logic, while a 360° CML-based PI is used for clock recovery.

A pair of differential clocks is externally supplied. 4 quadrature clock phases are generated by a divider or an injection-locked oscillator and distributed to RX and TX via buffers and transmission lines. In the TX, CMOS-based PIs are used to meet the timing requirements.

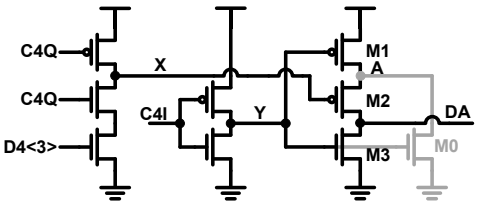

Fig. 2. The schematic of the proposed 1-UI pulse generator.

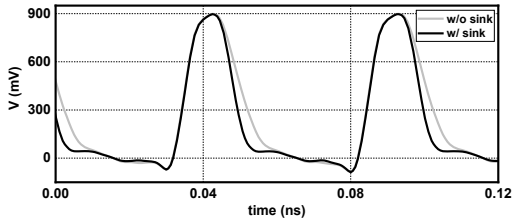

Fig. 3. The simulation results of the proposed 1-UI pulse generator.

III. Circuit Implementation

A. 1-UI Pulse Generator with Discharge Enhancement

For the 1-UI pulse generation circuit, the quality of the generated pulse directly determines the output eye diagram quality. The schematic of the proposed 1-UI pulse generator is shown in Fig. 2. At the output stage, when the input data is at a high level, and both C4I and C4Q are also high, the output node DA generates a high-level data pulse. Subsequently, when C4I transitions to low, transistor M1 is turned off while M3 is turned on, and the output node voltage begins to be pulled down.

However, due to the previously stored charge, node A remains at a high level. Meanwhile, the gate node X of transistor M2 stays low, keeping M2 in the on-state. Node A continues to discharge to the output node through M2. At node DA, while M3 pulls the voltage down, M2 simultaneously provides a charging path, leading to contention between the pull-down and pull-up paths. This slows down the falling transition of the output node, resulting in a tailing effect in the data pulse.

To address this issue, a pull-down transistor M0 is introduced at node A, controlled by the clock C4I. When node DA is pulled down, the charge at node A is discharged through M0, eliminating the undesired charging path to node DA. Conversely, when DA is required to be pulled up, M0 is turned off and does not affect the circuit operation. Simulation results shown in Fig. 4 demonstrate that M0 sharpens the falling edge of the output signal.

B. Low-Output-Skew DAC Technique

Strict matching among different bits in the output DAC is required to ensure good linearity. In addition, any mismatch in the loading of the driver chains can introduce variations in propagation delay and transition times across different bits, leading to timing skew as well as discrepancies in pulse amplitude and width, ultimately degrading the output eye diagram. To address this issue, a low-output-skew DAC technique is proposed in this work.

The structure and the layout of the output DAC of the proposed TX are shown in Fig. 4. To improve the linearity of the output DAC, the 2 MSBs are converted into 3 thermometer-coded bits (T5 to T7), with each bit weighted

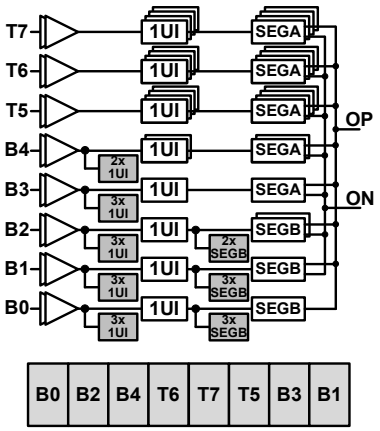

Fig. 4. The structure and the layout arrangement of the output DAC.

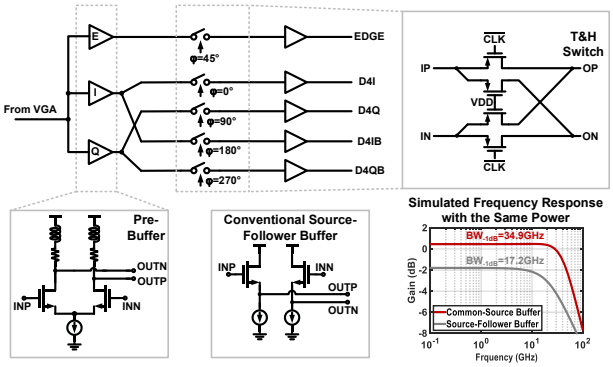

Fig. 5. The schematic of the TAH in the proposed RX.

at twice that of B4. Two types of output cells, SEGA and SEGB, are implemented for matching considerations. SEGA has four times the drive strength of SEGB, while the LSB, B0, is driven by a single-ended output cell with drive capability equal to 0.5x SEGB.

To match the load and delay across the 8-bit output paths, the 1-UI pulse generators are carefully scaled, and dummy cells are inserted for load balancing. The physical layout of the output array in the layout is carefully considered to minimize the impact of process-induced mismatch. To improve matching among DAC bits, higher-weight bit cells are placed at the center of the driver array, while lower-weight bit cells are distributed toward both sides of the array. Within each bit cell, adjacent pulse data signals are interleaved to minimize crosstalk.

C. High-Speed TAH Technique

Fig. 5 illustrates the schematic of the TAH circuit in the proposed TX. In conventional source-follower buffers, achieving a large g_m is challenging, resulting in relatively high output impedance and limited bandwidth. In contrast, for a common-source buffer, a higher bandwidth is enabled by a low load resistance and can be further extended by inductive peaking. In addition, voltage gain can be provided. Therefore, in this work, both the pre- and post-buffers of the TAH circuit are implemented as differential common-source amplifiers to provide isolation and sufficient drive strength.

The sampling switch operates with a 50% duty-cycle clock. The input is buffered separately by the I-path and Q-path buffers to ensure isolation. The sampling switch is realized using a pair of differential PMOS transistors. To

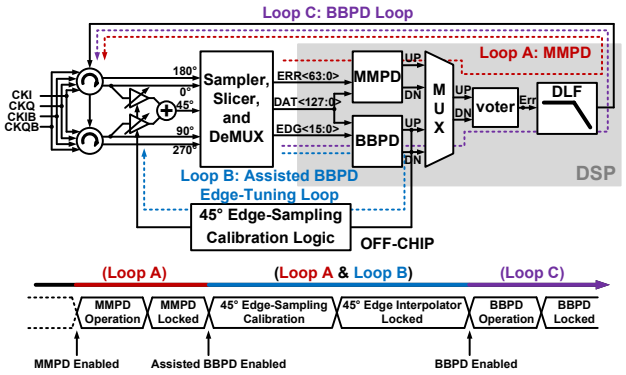

Fig. 6. The block diagram of the proposed dual-mode PD and the operation flow.

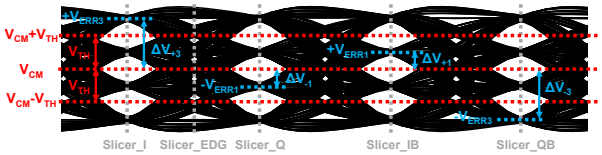

Fig. 7. The diagram of threshold adaptive logic.

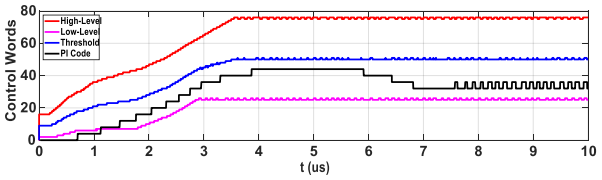

Fig. 8. The simulation results of CDR and threshold adaptive loop.

mitigate data feedthrough, an additional pair of cross-coupled off-state PMOS transistors is introduced in the sampling switch circuit to couple the inverted data from the opposite side to the output.

In conventional TAH circuits, dummy transistors are employed to reduce clock feedthrough. In this design, they are removed to achieve a higher sampling bandwidth, as the resulting feedthrough is predominantly common-mode and can be effectively suppressed by the differential design.

D. Dual-Mode PD and Threshold Adaptive Logic of RX

In CDR, both BBPD and MMPD are implemented in this design. An additional error slicer in each data path supports the MMPD [3]. For BBPD, an assisted 1.25× oversampling scheme is employed, in which one of the four available edges is sampled and calibrated by a loop. The clock distribution network is simplified significantly.

Fig. 6 shows the block diagram and operation flow of the proposed dual-mode PD. An assisted BBPD edge-tuning mode is proposed for 45° edge-sampling calibration, reusing the BBPD hardware with minimal overhead. During operation, the MMPD loop is first activated and locked. Subsequently, the assisted BBPD edge-tuning loop is enabled. The off-chip 45° edge-sampling calibration is employed to generate an optimal edge-sampling clock based on the BBPD results. The loop is then handed over to BBPD to take advantage of its higher PD gain. The voter and digital filter are shared among the two modes, thereby minimizing hardware complexity and power consumption while achieving the dual-mode operation.

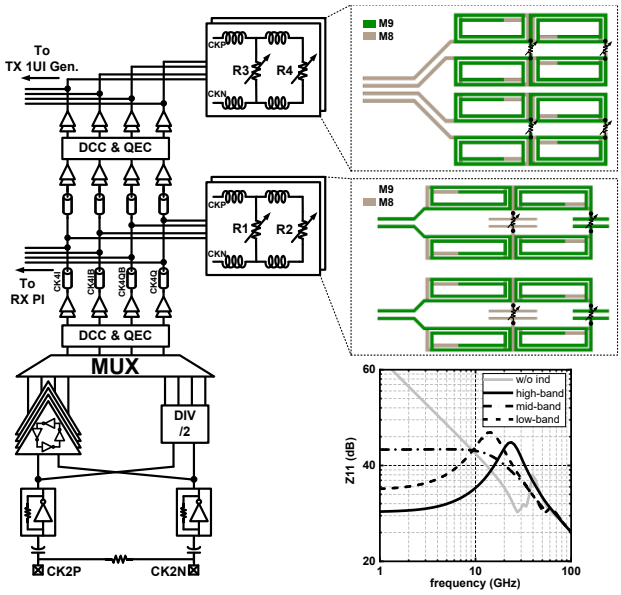

Fig. 9. The structure and the simulation results of the proposed clock path.

Among the two modes, BBPD is recognized for higher PD gain and more robust operation. Compared with 45° clock calibration techniques in the analog domain, the proposed edge-tuning scheme assisted by MMPD achieves a higher accuracy and robustness.

An adaptive threshold loop is achieved by using error slicers to dynamically optimize decision thresholds. As shown in Fig. 7, four error slicers are placed across the I, Q, IB, and QB paths and are configured to track the +3, -1, +1, and -3 PAM-4 signal levels, respectively. In each path, outputs from the data slicers and error slicers are used to adjust threshold levels adaptively. The comparison voltages of four error slicers converge to the corresponding eye levels, while the data-decision threshold is calculated by averaging ΔV_{+3}, ΔV_{+1}, ΔV_{-1}, and ΔV_{-3}. The simulation results shown in Fig. 8 illustrate a good convergence behavior of the adaptive loop, with the threshold voltage stabilizing at the midpoints of the PAM-4 signal levels.

E. High-Performance Clock Distribution Technique

Fig. 9 presents the structure of the proposed clock path. The external differential CML half-speed clock signals are AC-coupled and subsequently converted into CMOS levels. Depending on the operating speed, either an injection-locked quadrature clock generator or a frequency divider is employed to generate C4. A MUX selects the C4 source to support a wide input frequency range from DC up to 14 GHz. A DCC and QEC are implemented in the RX to ensure accurate clock alignment. C4 clocks are then distributed to both the RX and TX via buffers and transmission lines. A DCC and QEC are also implemented to correct clock distortions in the TX separately.

Due to the long transmission lines and heavy capacitive loads, significant clock signal attenuation occurs, particularly at higher frequencies. A high-performance clock distribution technique is proposed to reduce power consumption and provide jitter filtering. Shunt inductors are inserted between differential clock lines. Variable resistors are incorporated to tune the inductance and quality factor of the resonant tank, enabling compensation for load capacitance across different frequencies. 8-shape stacked inductors are utilized to save

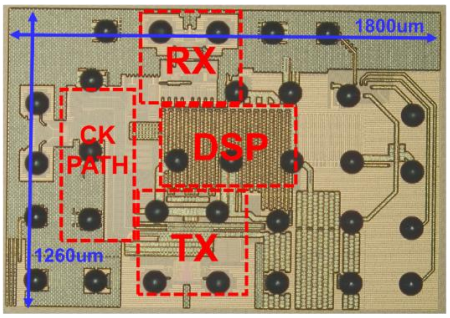

Fig. 10. The die micrograph of the proposed TRX.

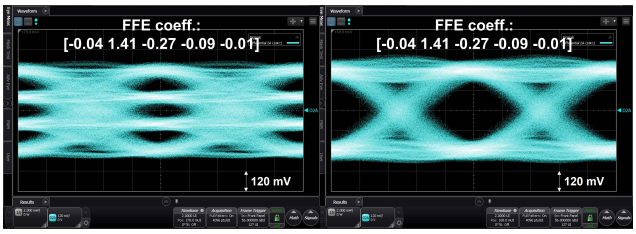

Fig. 11. The measured eye diagram of the proposed TRX.

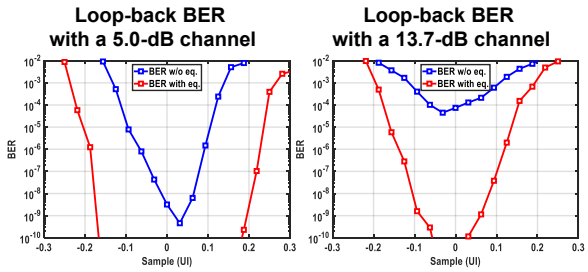

Fig. 12. The measured bathtub curves of the proposed TRX.

	ISSCC'22 [3]	ISSCC'21[4]	ISSCC'21[5]	ISSCC'24 [6]	This work
Technology	28nm	7nm	7nm	28nm	**28nm**
Data Rate (Gb/s)	112	112	112	112	**112**
Modulation	PAM-4	PAM-4	PAM-4	PAM-4	**PAM-4**
Supply Voltage (V)	N/A	1.2/0.9/0.75	N/A	1.2/0.9	**1.4/0.9**
TX architecture	Analog	7b DAC	5b DAC	Analog	**7b DAC**
TX equalization	3-tap FFE	8-tap FFE	5-tap FFE	3-tap FFE	**5-tap FFE**
TX swing (V)	0.8	N/A	N/A	N/A	**1.0**
RX architecture	Analog	ADC	Analog	ADC	**Analog**
RX equalization	CTLE + 4-tap FFE	CTLE + 32-tap FFE + 1-tap DFE	CTLE	CTLE	**CTLE**
Loss @Nyquist (dB)	20.8	26	7	8.5	**13.7**
BER at Max Loss	1E-11	1E-9	1.3E-10	1E-12	**1E-10**
Power Efficiency (pJ/b)	2.3*	8.2	1.7	2.2	**3.0**
FoM (pJ/b/dB, Efficiency/Loss)	0.11*	0.32	0.24	0.26	**0.22**
Area (mm^2)	0.12	0.82	0.23	0.24	**0.47**

* Excluding 4-phase clock generator and adaptation logic.

Fig. 13. Performance comparison with prior works.

area and reduce the coupling effect. Simulation results of the Z11 characteristic of the clock network indicate a broad operational frequency range extending down to DC.

IV. Measurement Results

The proposed TRX has been fabricated in a 28-nm CMOS process and occupies an area of 1.8mm×1.26mm, whose die micrograph is shown in Fig. 10. The core area of the chip is 0.47 mm^2. The performance of the chip is measured through flip-chip packaging and PCB traces. Fig. 11 presents the measured eye diagrams for PRBS7 112 Gb/s PAM-4 and 56 Gb/s NRZ signals, which were captured through a 4 dB-loss channel without any channel loss de-embedding or oscilloscope equalization. The on-chip FFE utilizes coefficients of [-0.04 1.41 -0.27 -0.09 -0.01], corresponding to 1 pre-tap and 3 post-taps. The measured loop-back bathtub curves shown in Fig. 12 demonstrate a BER $<10^{-10}$ at 112 Gb/s with on-chip equalization over a 13.7 dB-loss channel at Nyquist frequency. The entire chip consumes 334 mW (3.0 pJ/b), with 1.6 pJ/b attributed to the TX and clock path and 1.4 pJ/b to the RX, operating from a 0.9/1.4 V supply. Fig. 13 summarizes the TRX performance and compares this work with prior state-of-the-art designs. Compared to other XSR designs, this work demonstrates superior loss compensation with similar power efficiency.

V. Conclusion

A 112 Gb/s TRX with a 5-tap, 7-bit DSP-based TX and analog-based RX is proposed in this paper. The proposed TRX offers enhanced equalization capability while eliminating the power- and area-intensive ADC. A discharge enhancement technique and a low-output-skew DAC technique are proposed in TX. A high-speed, high-accuracy track-and-hold (TAH) technique is proposed in RX. An MMPD and a 1.25× oversampling assisted BBPD are implemented to enhance flexibility across diverse operating conditions. An adaptive threshold loop is proposed to enable automatic tracking of optimal decision levels. A tunable inductance network is proposed in the clock path to enable compensation for load capacitance across different frequencies and save power. Fabricated in a 28 nm CMOS process, the proposed TRX achieves a 13.7 dB channel loss compensation with a power efficiency of 3.0 pJ/bit.

Acknowledgment

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