A14 Pathfinding PDK with Backside Direct Contact for Power and Area Scaling Beyond N2

Yun-Jing Lin, Gabriel M. Soares, Halil Kükner, Subhash Sharma, Juergen Boemmels, Sheng Yang, Lynn Verschueren, Odysseas Zografos, Maarten Van de Put, Anita Farokhnejad, S. M. Yasser Sherazi, and Marie Garcia Bardon

imec, Kapeldreef 75, 3001 Leuven, Belgium

yun-jing.lin@imec.be

Abstract*— This paper extends imec logic Design Pathfinding PDKs (P-PDKs) from N2 to A14 node, further facilitating access to advanced nodes for the design community to support design innovation and system-level exploration. The A14 P-PDK introduces direct Backside Contact (BCT), eliminating the need for middle-of-line Through-Silicon Via (TSVM) used in N2. BCT reduces frontside routing congestion and enhances power delivery efficiency. A14 achieves improved total power consumption and reduced area compared to N2, identifying BCT as a key scaling enabler for advanced logic technologies.** ***Keywords—Pathfinding PDK, Nanosheet, GAA, backside PDN

I. Introduction

Design Pathfinding PDKs are developed to enable the design community to explore advanced nodes before access to manufactured nodes, bridging early technology assumptions to EDA-ready digital design environment. Following imec logic roadmap (Table I), the previous N2 P-PDK introduced Nanosheet (NSH) device architecture with Backside Power Delivery Network (BSPDN) as a scaling booster [1,2]. N2 used Through Silicon Via in the Middle-of-line (TSVM) to connect to the BSPDN. As the semiconductor industry steps into Angstrom nodes, the A14 P-PDK will now allow designers to explore NSH with BSPDN using a new scaling booster, direct Backside Contact (BCT). Table II compares the main features of N2 and A14 PDKs. Defining robust assumptions for P-PDKs requires comprehensive modelling and analysis across both design and technology domains, achieved through Design-Technology Co-Optimization (DTCO).

TABLE I. IMEC Logic Roadmap down to A14

Technology Node	N7	N5	N3	N2	A14
Transistor Structure	FF	FF	FF	**NSH**	**NSH**
Std cell height #tracks	6.5T	6T	6T	6T	5.5T
# Fins/sheets per active	3	2	2	4 sheets	4 sheets
Gate Pitch [nm]	56	48	48	48	45
Metal Pitch (MP) [nm]	40	28	26	22	21
BEOL metal stack (Mx, My, Mz)	Cu 13	Cu 15	Cu 17	FSPDN: Cu 17 BSPDN: Cu 13(FS)+Cu 4(BS)	BSPDN: Cu 13(FS)+Cu 5 (BS)

This paper is structured as follows: Section II presents the A14 technology node definition including power delivery scheme, BEOL interconnect stack, RC parasitic modeling methodology, and the evaluation of A14 performance on Ring Oscillator (RO). Section III details standard cell layouts, design constraints, and cell size comparison between A14 and N2. Section IV outlines the block-level assessment, presenting power and area performance of A14 compared to N2. Section V summarizes the paper with conclusions.

TABLE II. N2 P-PDK vs. A14 P-PDK Features

Feature	N2 TSVM	A14 BCT
Transistor Structure	NSH	NSH
Std cell height #tracks	6T	5.5T
# Sheets per active	4	4
Gate Pitch [nm]	48	45
Metal Pitch (M0) [nm]	22	21
Backside Connection Scheme	Through-Silicon Via to device side	Backside direct contact to device
SDC count in digital library	160	162
Embedded memory	29 SRAM macros	-
Device flavors	ULVT, LVT, SVT, HVT	
V_{dd} characterization	0.5V, 0.7V, 0.9V	
Temperature	25°C, 85°C, 125°C	

II. A14 Technology Definition

A. Backside PDN with BCT

Different contacting schemes are possible to connect the devices to the power delivery present at the wafer backside (Fig. 1). The transition from TSVM to BCT eliminates the need for MOL and frontside landing structures, removing associated area overhead such as pads, enclosures, and via stacks. BCT also fully offloads power routing from the front side to the backside, reducing routing congestion and freeing metal resources for signal interconnects. In addition, the absence of large TSV structures relaxes layout constraints, including keep-out zones and alignment margins, enabling tighter design rules and improved layout density. This combination of reduced routing overhead, simplified connectivity, and enhanced layout flexibility allows for more compact standard cell architectures and ultimately leads to improved area efficiency.

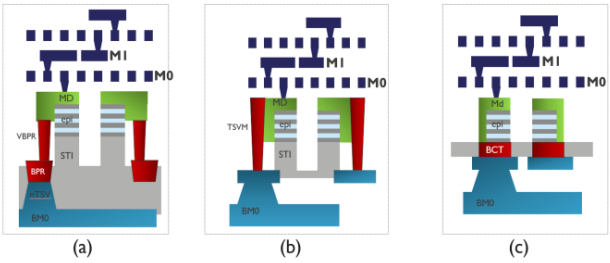


Fig. 1. NSH device cross-sections of different backside contacting schemes: (a) Buried-Power Rail with vertical via (b) TSVM with backside routing and (c) BCT to directly access source/drain EPI.

B. Process Flow

Fig. 2 illustrates the simplified fabrication flow of NSH devices with BCT. The process begins with Si/SiGe superlattice growth, followed by fin patterning, gate patterning and gate spacer formation. Next, the source/drain (S/D) regions are recessed and regrown by in-situ doped epitaxy, the trenches are filled with dielectric, and the dummy gate is replaced by the final replacement metal gate (RMG), similar to N2. The key difference compared to the N2 TSVM scheme is the backside connection module. In N2, TSVMs are etched into the substrate and filled together with the S/D contacts. In A14 BCT, frontside contact trenches are patterned first, the S/D region is metallized, and the frontside BEOL is completed. The wafer is then flipped and thinned for the backside reveal (bulk Si removal), followed by backside contact metallization to directly connect to the S/D region, and finally backside BEOL formation using a damascene process, similar to the frontside.

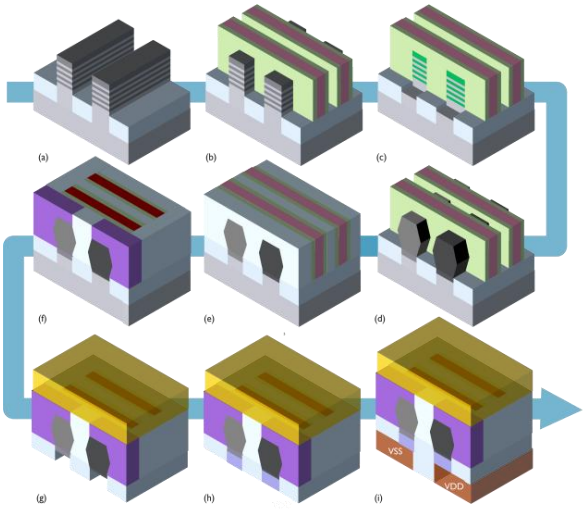


Fig. 2. Process steps of NSH with BSPDN enabled by BCT (a) superlattice growth, (b) gate patterning + gate spacer deposition, (c) fin recess, (d) S/D epi growth, (e) oxide fill + replacement metal gate + gate cut, (f) S/D contact and optional TSVM, (g) FS BEOL stack + Backside reveal, (h) Backside Contact Metallization, (i) Backside BEOL.

C. BEOL Interconnect Stack

A14 BCT P-PDK is released with 18 metal layers for signal routing. Table III contains details on the process assumptions for pitch, dimensions, including resistances and capacitances (R-C) values obtained from semi-empirical model calibration and 2D Synopsys Raphael FX simulations [9]. There are 6 Mx layers (M0-M5), 4 My layers (M6-M9), all fixed at 80 nm pitch, and 3 Mz layers (M10-M12), where M10-M11 are at pitch 160 nm and M12 at 320 nm pitch. Power delivery network is done with 3 dedicated backside metal layers (BM0-BM2) and two more backside metal layers (BM3-BM4) as redistribution layers (RDL).

D. Modeling Methodology

The nanosheet device behavior is captured by a BSIM-CMG [10] model card fitted to TCAD data [12] calibrated to foundry reference data. The BSIM model card represents a single nanosheet. A complete transistor is then built by connecting four of such nanosheet models in parallel, reflecting the A14 device structure. The compact model captures the intrinsic drift-diffusion behavior of the nanosheets, while parasitic resistances and capacitances are treated separately. These four sheets are interconnected through common source/drain EPI regions and a common gate. From the standard cell layouts, the 3D structure is then extruded using Synopsys Sentaurus Structure Editor (SDE) [13] as showing in Fig. 3 for two different logic cells.

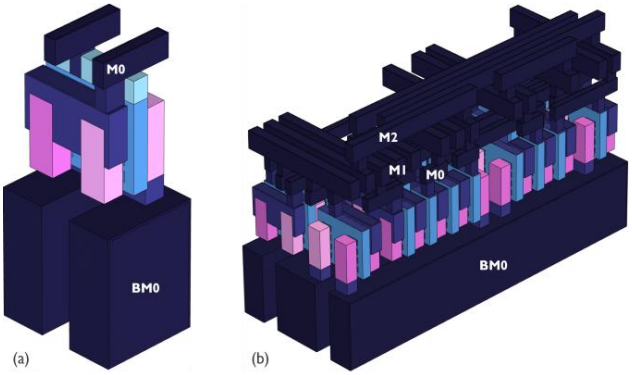


Fig. 3. 3D structure built for A14 BCT PEX extraction, for (a) INVD1 inverter and (b) SDFFSLD1 scan D-flipflop.

TABLE III. BEOL STACK LITHOGRAPHY PROCESS, DIMENSIONS AND RC

Metal	Process	Pitch [nm]	CD [nm]	Height [nm]	R [Ω/μm]	C [fF/μm]
Gate	-	45	-	-	-	-
M0	EUV DP	21	12	22	467.4	0.296
M1	EUV SP	30	18	30	157	0.286
M2	EUV SP	28	16	24	209	0.265
M3	EUV SP	32	20	24	178	0.257
M4	EUV SP	32	20	24	178	0.257
M5	EUV SP	32	20	24	178	0.241
M6	193i SP	80	40	80	16.2	0.207
M7	193i SP	80	40	80	16.2	0.196
M8	193i SP	80	40	80	16.2	0.196
M9	193i SP	80	40	80	16.2	0.196
M10	193 SP	160	80	80	3.3	0.225
M11	193 SP	160	80	160	3.3	0.215
M12	248 SP	320	160	320	0.7	0.263
BM0	193i SP	115	85	115	3.73	0.559
BM1	193i SP	180	90	180	2.2	0.450
BM2	248 SP	320	160	320	0.7	0.517
BM3	248 SP	320	160	320	0.7	0.409
BM4	365 SP	1080	540	540	0.11	0.484

Given that parasitic R and C values highly influence the device operation, the parasitics RC surrounding the nanosheets are extracted from the 3D structure using Synopsys Raphael FX simulations [9]. They are then combined into a single netlist with four BSIM core models [10] for each transistor, together with the parasitic contributions from other FEOL layers, such as EPI shapes, MD, vias, and all related structures.

From Fig. 4, calibrated A14 NSH compact model results are aligned with the N2 NSH reference [2] for both I_d-V_g and C_{gg}-V_{gs} characteristics. Similar transfer behavior is observed in linear regime, V_{ds} = 0.05 V, and saturation regime, V_{ds} = 0.7 V, with a small shift in the subthreshold and near-threshold regions, which is consistent with the fact that the A14 node was designed with a lower off-state current target, with an I_{off} of 1.634 nA compared with 2 nA for N2 node. At the same time, A14 shows lower C_{gg} over V_{gs} range in both regimes, while maintaining the same general bias dependence as N2. This behavior points to reduced effective capacitive loading, expected with the structural scaling of the device and the BEOL stack.

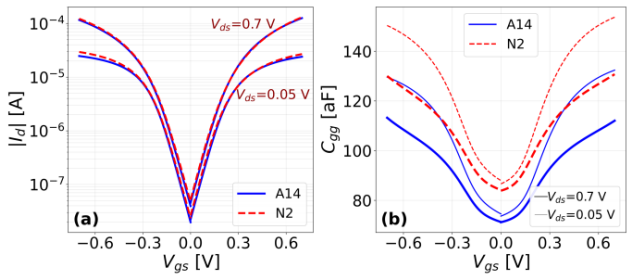


Fig. 4. I_d-V_g and C_{gg}- V_g characteristics for A14 NSH compared to N2 NSH. NFET device from 0 to 0.7 V and PFET device from -0.7 V at V_{gs} axis.

Across process corners, threshold-voltage options, and temperature, the A14 device defines a consistent design space for performance-power trade-offs (Fig. 5). Both nFET and pFET devices exhibit the expected I_{on}/I_{off} relationship, in which lower threshold voltage enhances drive current at the expense of higher off-state current, whereas higher-threshold options support lower-power operation. The temperature dependence shows I_{off} increasing more strongly than drive current while maintaining the relative order among the available device options.

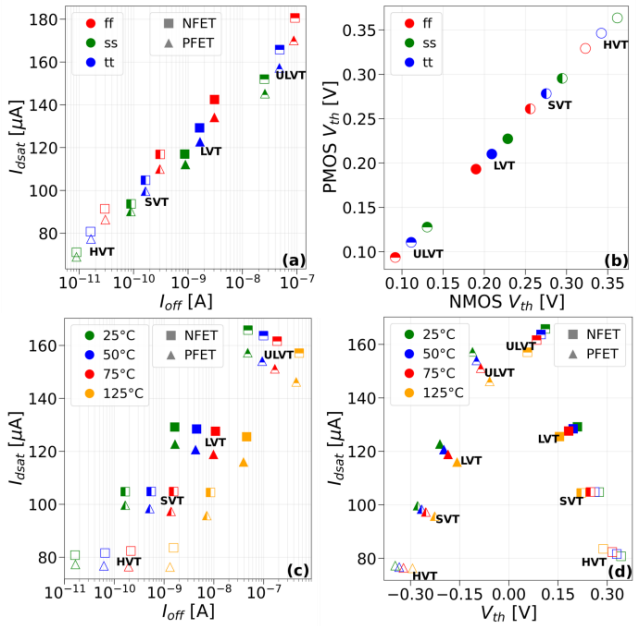


Fig. 5. A14 DC performance. (a) I_{on}, I_{off} of NFET and PFET across process corners for different V_{TH} flavors. (b) Different target V_{TH} flavors (SVT, LVT, ULVT) for NFET and PFET (c) I_{on} vs I_{off} of NFET and PFET for different V_{TH} flavors across different temperatures (d) I_{on} of the various V_{TH} flavors across temperature.

E. Ring Oscillator Evaluation

A14 was benchmarked using a 15-stage ring-oscillator simulation with INVD1 cells at the typical-typical corner using the LVT variant, with V_{dd} swept from 0.2 V to 0.9 V. Realistic BEOL loading was incorporated through the Critical Path Modeling (CPM) method [11], in which equivalent RC parasitics are extracted from implemented critical paths. Two loading scenarios were considered, corresponding to interconnect lengths of 0.5 µm and 1.95 µm, Fig. 6. In both cases, A14 achieves comparable frequency to N2 across the V_{dd} range, while reducing power consumption by approximately 10%. This gain is driven by a reduction in effective capacitance (~10.6%), and a decrease in effective current (~10%), demonstrating the improvement in energy efficiency.

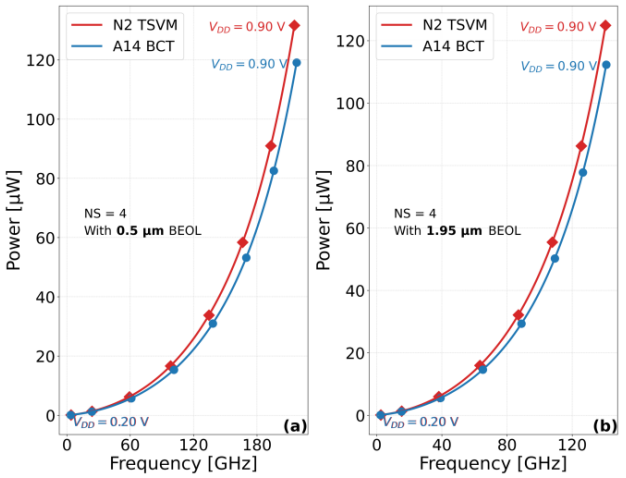
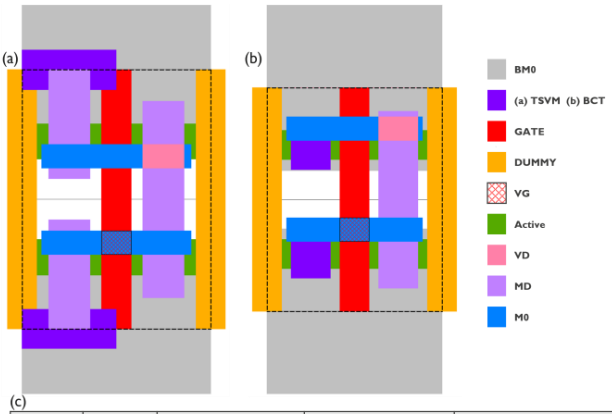


Fig. 6. A14 vs. N2 RO simulation results using INVD1 cells with four stacked nanosheets including BEOL load, sweeping V_{dd} from 0.2 to 0.9 V with: (a) 0.5 µm BEOL (b) 1.95 µm BEOL

III. Standard Cell Library

A library of 162 standard cells with varying numbers of inputs and drive strengths is created in A14 BCT node. The set includes basic/complex combinational cells and sequential cells, e.g. inverters, buffers, nand, nor, and, or, and-or-(invert), or-and-(invert), multiplexer, exclusive or/nor, single and multi-bit (scan) flops, latch, clock gates, full adders and various special cells such as decoupling caps, delay, fill, tap and tie cells. Standard cell libraries have been extracted in [9] and characterized in [15] by using [16] as the external circuit simulator.



Tech Node	Cell Height (nm)	M0		Gate		NSH	
		Pitch (nm)	Width (nm)	Pitch (nm)	Length (nm)	Width (nm)	Spacing (nm)
N2 TSVM	132	22	12	48	15	18	41
A14 BCT	115	21	12	45	15	15	41

Fig. 7. Top layout view of INVD1 standard cell in (a) N2 TSVM (b) A14 BCT, and (c) table with main dimensions

Top layout views of the inverter (INVD1) cell are shown in Fig. 7 for A14 BCT and N2 TSVM nodes, where both layouts are completed with only M0 metal as the horizontal routing layer. Moreover, overall metal usage and pin accessibility in cells are optimized for improved routing efficiency and PPA at block level. The backside power delivery frees the frontside metal tracks at upper/lower cell boundaries and enables further cell height scaling. A14 BCT is scaled down to 5.5T cell height with 4 internal M0 routing tracks, while N2 TSVM is kept at 6T cell height with 4+1

extra internal M0 routing track. The extra routing track can relax the congestion that would be caused in FSPDN and improve the design routability at block level. Standard cells in A14 BCT and N2 TSVM share the same transistor placement and routing. The combined impact of gate CPP reduction from 48nm to 45nm, M0 pitch from 22nm to 21nm, and cell height from 132 nm to 115 nm, achieves a total area reduction of 18% on standard cells from N2 TSVM to A14 BCT node.

IV. Block Level Assessment

For block-level assessment, a benchmark is made for the A14 extracted library with BCT and N2 TSVM libraries. Using Cadence EDA tools [17], both libraries are applied separately to perform physical design experiments under different target frequencies and target utilizations. Fig. 8 shows the results of physical implementation of two designs (Arm Cortex-M0 and an Arm 64-bit HD CPU (Armv8) without no SRAM macros), comparing A14 BCT and N2 TSVM. At iso-frequency, A14 BCT offers area reduction of around 18%, which is consistent with the 18% area reduction at the standard cell level. Total power comparison in Fig. 8 shows that A14 BCT consumes 5-10% less compared to N2 TSVM at the same target frequency and utilization. The physical design results also highlight the benefits of pushing PDN to the backside layers, with PDN distributed on the backside. In the Arm 64-bit HD CPU design, 95.4% of signal nets are completed within Mx layers, with My layers contributing 3.7% more and Mz layers only 0.9%. On total signal wirelength, 73.8% is routed on Mx, 21.0% on My, and 5.0% on Mz. The performance achieved for the designs is intended to demonstrate the PPA difference between A14 and N2 libraries; the performance of the design is not constrained by these specific conditions.

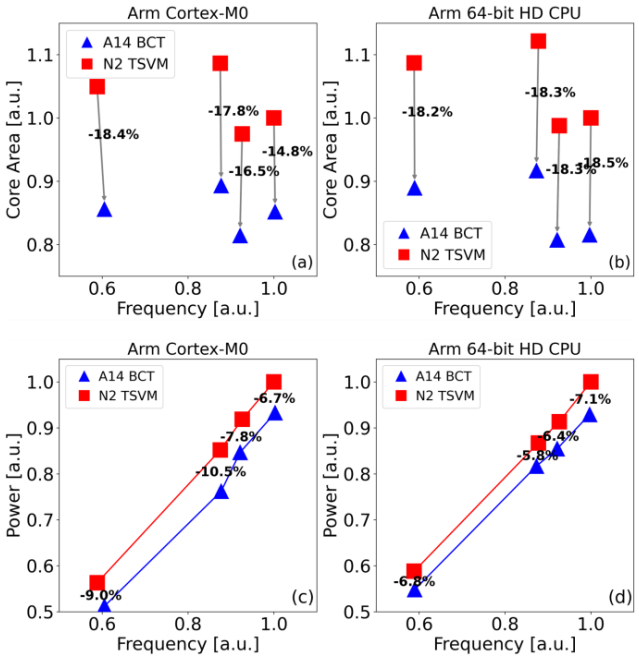


Fig. 8. Physical design results in two designs: Arm M0 and Arm A53 (a)(b) area comparison (c)(d) power comparison between A14 BCT and N2 TSVM

V. Conclusion

Imec A14 P-PDK featuring nanosheets with backside power enabled by direct backside contact (BCT) is released to the wider design community to support early digital design exploration beyond N2. Based on Design-Technology Co-Optimization with silicon-influenced models and parametric extraction flows, the PDK contains a library of 162 standard cells validated at CPU level. Compared with the N2 TSVM scheme, BCT eliminates MOL/frontside landing penalties and shifts power routing fully to the backside, reducing frontside congestion and enabling more compact standard-cell architectures. Block-level physical design results confirm improved PPA, achieving 5–7% total power reduction and ~18% area reduction at iso-frequency.

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References

[1] N. Loubet et al., "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," Proc. Symp. VLSI Techno, Jun. 2017, pp. 230-231.
[2] A. Farokhnejad et al., "N2 Nanosheet Pathfinding-PDK (P-PDKTM) including back-side PDN," 2024 IEEE European Solid-State Electronics Research Conference (ESSERC), Bruges, Belgium, 2024, pp. 17-20.
[3] H. Kükner, G. Mirabelli, S. Yang, Y. Zhou, A. Makarov, Y. Xiang, J. Boemmels, A. Veloso, O. Zografos, P. Weckx, J. Ryckaert, G. Hellings, "High-density standard cell libraries with backside power options in A14 nanosheet node," Proc. SPIE 12954, DTCO and Computational Patterning III, 1295409 (10 April 2024).
[4] S. Yang et al., "PPA and scaling potential of backside power options in N2 and A14 nanosheet technology," 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 2023, pp. 1-2.
[5] S. Yang et al., "Multi-node scaling potential of monolithic CFET," 2025 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2025, pp. 1-4.
[6] Roussel, Ph J., et al. "Semi-empirical interconnect resistance model for advanced technology nodes: A model apt for materials selection based upon test line resistance measurements." 2016 IEEE International Reliability Physics Symposium (IRPS). IEEE, 2016.
[7] J. Y. Lin et al., "3.5T CFET block-Level DTCO for superior PPA in A7 node by split power, hDR cells, optimized pins and BEOL," 2025 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2025, pp. 1-4.
[8] G. Sisto et al., "Block-level evaluation and optimization of backside PDN for high-performance computing at the A14 node," 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 2023, pp. 1-2.
[9] Raphael FX, Synopsys inc, Mountain View, CA, USA
[10] BSIM-CMG MOSFET compact model. [Online] Available: http://bsim.berkeley.edu/models/bsimcmg/.
[11] F. Dell'Atti, A. Farokhnejad, O. Zografos, P. Weckx, J. Ryckaert and P. Heremans, "Interconnect delay modeling of critical paths in angstrom nodes," 2024 IEEE International Interconnect Technology Conference (IITC), San Jose, CA, USA, 2024, pp. 1-3.
[12] Synopsys Sentaurus Device, Synopsys inc. Mountain View, CA, USA.
[13] Synopsys Sentaurus Structure Editor (SDE), Synopsys Inc., Mountain View, CA, USA.
[14] SEMulator 3D, Semiverse Solutions, Lam Research, Fremont, CA, USA.
[15] Liberate, Cadence® Liberate™ Trio™ Characterization Suite.
[16] Spectre, Cadence® Spectre® Circuit Simulator.
[17] Innovus, Cadence® Innovus™ Implementation System.