A 95.7% Efficient, Modified Hysteretic Current Mode Buck-Boost Converter for OLED Displays

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***Abstract*—This article presents a non-inverting buck-boost dc-dc converter addressing the stringent needs for the generation of the positive rail of Organic-Light-Emitting-Diode displays in Li-ion battery-powered consumer devices. Operating in different modes, the proposed converter maintains high efficiency across broad load ranges, without any limitation on the voltage conversion typically found in hybrid converters. The novel modified hysteretic current-mode controller guarantees seamless transitions between different operating modes, as well as superior rejection of fast line transients. A 1 A-capable dc-dc converter has been fabricated in a 180 nm technology, and with a low-profile 1.5 μH inductor a peak efficiency of 95.7% has been measured.**

***Index Terms*—power management, PMIC, non-inverting buck-boost, dc-dc, BCD, PFM, DCM, current-mode, OLED, TDMA**

I. Introduction

Modern consumer applications pose strict requirements in the power management of portable Li-ion battery-powered devices. On one hand, the power-management-integrated-circuits (PMICs) are required to maintain high efficiency across the entire load range. On the other hand, deep miniaturization and compactness severely restrict the available space, especially for passive components, given the maximum thickness of 1mm. In this context, Organic-Light-Emitting-Diode (OLED) panels are connected to the Li-ion battery by means of a flat cable, in which the dedicated PMIC is soldered. The resulting input power-delivery-network (PDN) poses extra challenges on the PMIC design, particularly considering the sensitivity of OLED displays. To not affect the user experience, these panels require a clean and stable power supply to minimize flickering on screen [1]. Any transient affects the voltages of each single pixel's thin-film transistor, leading to undesired variations in the display luminescence [2].

Considering the densely packed consumer devices, the dc-dc converter is requested to properly isolate the OLED display from any other disturbance on the input PDN. For this reason, the converter has to sustain fast line transients (i.e., TDMA, time-division multiple access noise [3]) minimizing any output variation. Given the positive regulated rail requested by the growing demand of wide-dynamic-range panels [4], from below 2 V to above 5 V, and the Li-ion battery range (i.e., from 2.2 V to 5 V considering the PDN voltage drops/spikes), a non-inverting buck-boost (BB) is needed.

Recently, hybrid BB (HBB) converters have been proposed [5]-[7], mainly to improve the efficiency compared to the conventional four-switch BB (CBB). However, they exhibit stringent limitations in the voltage-conversion-ratio (VCR), thwarting their use in Li-ion battery applications and especially OLED. Moreover, the need of additional external passive components (i.e., flying capacitors) severely constrains their usage in densely packed consumer devices, while adding extra costs and reliability issues. In addition, the efficiency improvement given by HBB solutions is not present at light-load, with most of them operating only in continuous-conduction-mode (CCM), or even not being able to guarantee output regulation.

Considering the CBB, extensive research has focused on the control strategies. Thanks to the unison control of the four power switches, single-mode CBBs with two-phase coil current guarantee seamless operation between buck and boost regions, but with a severe efficiency degradation. On the contrary, with the effort of maximizing efficiency, multi-mode CBBs operate the bridge as a buck, a boost or a mix of both according to V_{IN}/V_{OUT} conditions [8]-[9], and here the challenge is to guarantee smooth transitions between modes. To address the aforementioned needs, a multi-mode modified hysteretic current-mode BB featuring high efficiency across whole load range is presented. Not relying on any feed-forward, this BB inherently exhibits seamless transition between modes, and high rejection of fast line transients.

II. Proposed DC-DC Converter

A. Operating Modes

As depicted in Fig. 1, within a single CCM switching cycle the proposed BB features four possible phases PHx, with PH1 and PH2 always performed. In PH1 the coil is directly charged from the battery (V_{IN}), while PH2 can be a magnetizing or demagnetizing phase (depending on V_{IN}/V_{OUT}). In PH3 the inductor is discharged at V_{OUT}, while PH4 is a maintaining phase for the coil current. Depending on the operating conditions, PH3 and/or PH4 are not performed. In fact, in boost-mode (i.e., V_{IN} sufficiently lower than V_{OUT}), the converter performs only PH1 and PH2. In this case, the dc-dc converter performs as a classical boost converter, maximizing the efficiency and current delivery. Given the battery voltage in combination with the typical V_{OUT} of 4.6 V [2], boost-mode is the most likely operating mode. On the opposite side, when V_{IN} is sufficiently higher than V_{OUT} (i.e., buck-mode), the BB exploits also PH3 to properly discharge the coil. Finally, when the battery voltage is close to the output voltage (i.e., BB-mode), a short fourth phase PH4 is added in each switching cycle.

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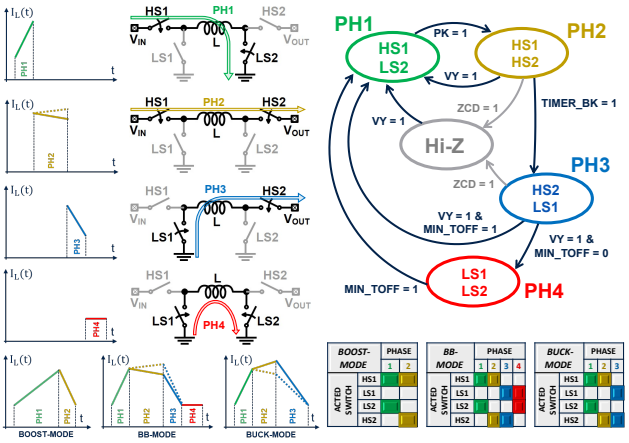

Fig. 1. BB operating phases: $I_L(t)$, acted switches, and controller state-flow.

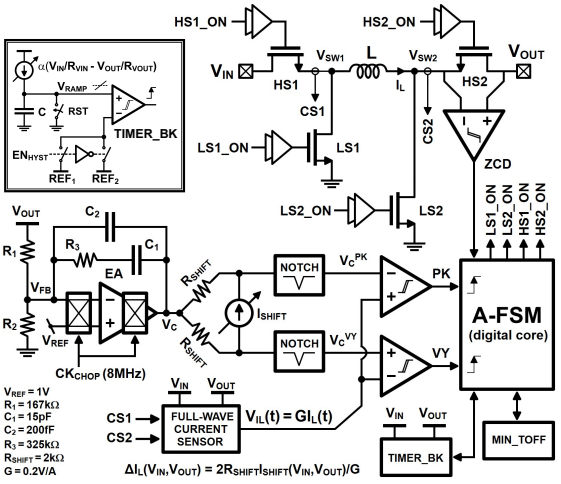

Fig. 2. BB architecture (G is the current-sensing gain), and TIMER_BK realization. V_{OUT} setpoint is set with 100 mV steps by acting on R_2.

B. System Controller

The BB control algorithm, synthesized with an asynchronous-finite-state-machine (A-FSM), is summarized in the state-flow in Fig. 1, with dark transitions for CCM operation. At the beginning of each switching cycle, PH1 is performed until the coil has been V_{IN}-charged at given value (i.e., PK = 1). In the following PH2 a simple timer (TIMER_BK) is started, and PH2 lasts until the first of the following events occur: 1) the coil has been discharged until reaching a set minimum value (i.e., VY = 1), or 2) overflow of TIMER_BK. Depending on the coil current slopes, the former case happens in boost-mode, and in this scenario a new switching cycle is started back with PH1. On the contrary, the latter occurs in buck-mode or BB-mode. In these cases, the coil current in PH2 remains almost flat (i.e., BB-mode, $V_{IN} \sim V_{OUT}$) or increases (i.e., buck-mode, $V_{IN} > V_{OUT}$), and thus failing to reach the set coil current minimum value. When PH3 is reached, another timer (MIN_TOFF) is started, and the coil is V_{OUT}-discharged until reaching a set minimum value (i.e., VY = 1). In this moment, MIN_TOFF is checked. If it has already reached the timeout, then a new switching cycle is started back with PH1. Otherwise, prior starting a new cycle, the BB moves into the buffer phase PH4 until the timeout of MIN_TOFF.

The implemented controller is depicted in Fig. 2. A type-II compensator featuring a two-stage error-amplifier (EA) in closed-loop configuration provides the control voltage V_C. To minimize offset and noise on V_{OUT}, the EA is chopped at F_{CHOP} = 8MHz. Starting from V_C, two symmetric offset voltages are created by means of a couple of matched resistors (R_{SHIFT}) and current mirrors synthesizing I_{SHIFT}, thus obtaining V_C^{PK} and V_C^{VY}, which respectively define the programmed coil peak and valley currents. Prior to feed the inputs of the peak (PK) and valley (VY) comparators, a couple of notch filters are used to limit the EA chopping spur. A pair of sense-FET-based current sensors are implemented on both HS1 as well as HS2 (not shown, being a well known standard in the art), to faithfully recover the combined full-wave coil current, and this information[1] (V_{IL}) is provided to both the aforementioned comparators.

To reduce switching frequency (F_S) variations and maximize the performance, I_{SHIFT} (and thus ΔI_L) is adapted with both V_{IN} and V_{OUT}, and a similar adaptation is performed to set the duration of TIMER_BK. Both the TIMER_BK and MIN_TOFF analog timers are simply based on synthesizing a ramp voltage by sourcing current on a capacitor, and comparing it with respect to a reference voltage. The implementation of TIMER_BK is shown in the inset[2] of Fig. 2, and for proper equalization, the current source is made dependent on both V_{IN} and V_{OUT} (with $R_{VIN} < R_{VOUT}$).

C. Dual-Mode Fully Integrated Self-Bootstrap Driver

The driver of HS2 exploits a bootstrap scheme leveraging the always present switching activity of V_{SW2}, which allows to recharge the on-chip bootstrap capacitor cycle-by-cycle. The same cannot be applied to HS1, since in boost-mode HS1 must be kept ON and LS1 OFF, thus hindering the recharging of C_{BS}. To overcome this limitation, a novel dual-mode self-bootstrap circuit is proposed in Fig. 3, featuring two phases of operation (in each $T_S = 1/F_S$) when the BB is in boost-mode. During $\Phi = 1$, C_{BS} is decoupled from the driver supply V_{DR} and V_{SW1}, thus allowing it to be recharged by grounding its bottom plate. In this phase, HS1 remains ON supplied by an auxiliary capacitor C_{DR}. In the second phase, $\Phi = 0$, C_{BS} is connected back to V_{DR}/V_{SW1}, restoring HS1 driving voltage. With the converter in BB-mode or buck-mode (i.e., V_{SW1} switching), Φ is kept at 0, and the circuit operates as a normal bootstrap driver, with only M_S switching. Given V_{INmin} = 2.2 V, a switched-capacitor voltage-doubler is used to feed a

[1]To note that such current sensors are already available within OLED PMICs, being typically required for telemetry and protection purposes.

[2]MIN_TOFF timer is identical to TIMER_BK, but the current source is simply constant, since there is no need to adapt the duration of PH4 (∼80ns).

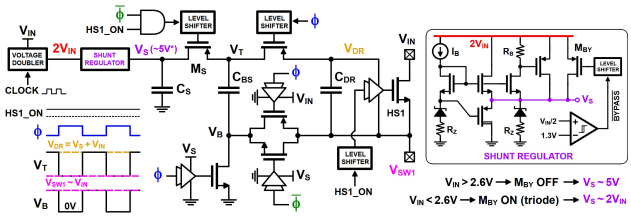

Fig. 3. HS1 Self-Bootstrap driver with shunt regulator: the waveforms refer to the BB converter operating in boost-mode (i.e., only V_{SW2} switching while V_{SW1} is kept at about V_{IN} by HS1 being ON). The shunt regulator is bypassed with M_{BY} when $2V_{IN} < 5.2$ V.

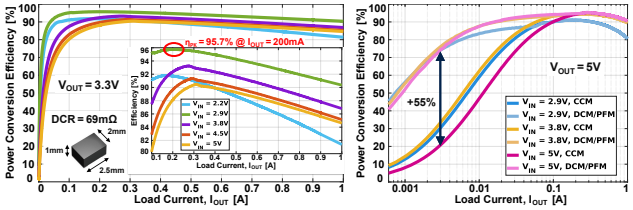

Fig. 5. CCM efficiency measurements at V_{OUT} = 3.3 V (left), and measured efficiency comparison between LPM and CCM (right) with V_{OUT} = 5 V.

zener-and-source-followers-based shunt regulator (Fig. 3 inset on the right), allowing to obtain a suitable clamped voltage V_S to supply all the drivers.

D. Light-load and Mode Transitions

In low-power-mode (LPM), to maximize efficiency at light load a zero-crossing-detector (ZCD) comparator is exploited (Fig. 2) to monitor the coil current and avoid negative currents. As shown by gray-colored transitions in the state-flow of Fig. 1, during any coil discharging phase (i.e., PH2, PH3) the ZCD comparator is monitored, eventually interrupting the demagnetizing phase. In this case, the bridge is maintained in high impedance (i.e., all the power switches are OFF) until a new charging phase is required, whose event is signaled by an increase of V_C, triggering the valley current comparator (i.e., VY = 1). Any transition between modes is automatically performed by the converter, without the need to assess V_{IN}/V_{OUT} and force a particular operating mode. For a given V_{OUT}, the transition between boost-mode and BB-mode happens whenever, approaching V_{OUT}, V_{IN} flattens the coil discharging slope in PH2 such that I_L no longer reaches I_L^{VY} set by the EA, but TIMER_BK triggers. As V_{IN} keeps rising, I_L^{PK} is adaptively reduced, and when the coil discharge phase PH3 is longer than a minimum threshold signaled by the trigger of MIN_TOFF, PH4 is not performed anymore (i.e., transition to buck-mode automatically occurs). To avoid limit-cycle oscillations between modes, proper hysteresis is applied on each timer by changing the reference voltage monitored by the comparator (see EN_{HYST} in the inset of Fig. 2).

III. Experimental Results

The presented BB is part of a PMIC fabricated in a 180 nm Bipolar-CMOS-DMOS (BCD) technology, and it is shown in Fig. 4. Efficiency measurements performed with

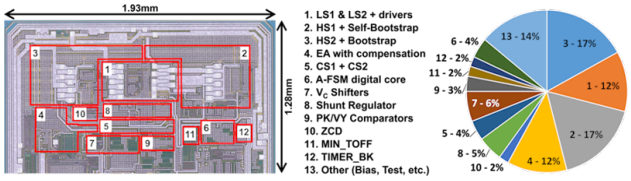

Fig. 4. Die micrograph of the fabricated BB converter and area breakdown.

automatic equipment are showcased in Fig. 5. To be compliant with highly dense consumer applications, a 1.5μH low-profile inductor has been selected, and a peak efficiency of 95.7% has been measured (V_{IN}=2.9V, I_{OUT}=0.2A). In LPM, efficiency improves up to +55% until I_{OUT} reaches 50 mA-0.2 A (V_{IN}-dependent), and then the converter smoothly operates in CCM. To demonstrate seamless mode transitions, a 100 Hz tone swinging between 3 V and 5 V has been applied as V_{IN}, and as presented in Fig. 6, the converter smoothly maintains regulation at V_{OUT} = 4 V (I_{OUT} = 0.1 A) with only a small change of ripple voltage, but without any fluctuation or transient. The results of a TDMA noise test [3] conducted changing V_{IN} from 3.7 V to 4.2 V in 20 μs are presented in Fig. 7 (left), in which the spikes and dips remain below 1mV, at V_{OUT} = 3.3V. When V_{IN} is changed from 3 V to 5 V in 30 μs (right part of Fig. 7), small spikes and dips of about 3.5 mV are measured at V_{OUT} = 3.3 V (I_{OUT} = 0.1 A). As shown in Fig. 8 for different V_{IN}/V_{OUT} conditions, when full load step variations are applied, the BB converter exhibits symmetric responses with a settling time below 20 μs, and maximum overshoot/undershoot of 120 mV/105 mV. To note that in contrast to HBBs [5]-[7], the proposed BB does not suffer of any evident load regulation error, revealing tight regulation accuracy. Table I presents the performance summary compared with prior art. The fabricated BB covers the largest V_{IN} and V_{OUT} ranges, without any VCR limitation that would hinder the use of HBBs

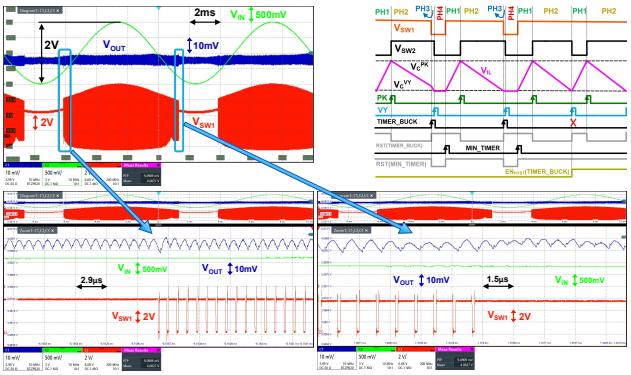

Fig. 6. Seamless mode transitions between boost-mode and BB-mode: 100 Hz V_{IN}-tone while regulating V_{OUT} = 4 V at I_{OUT} = 0.1 A (top left), and zoom-in of the transition regions (bottom). Sketched on the top right, key signals of the controller illustrate the mode change when V_{IN} decreases.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS STATE-OF-THE-ART WORKS

		JSSC'25 [5]	JSSC'25 [6]	JSSC'24 [7]	TPEL'21 [8]	TIE'19 [9]	**This Work**
Technology [nm]		180 BCD	180 CMOS	180 CMOS	130 CMOS	180 BCD	180 BCD
Topology[(a)]		Hybrid (DP)	Hybrid (BS)	Hybrid (IL)	CBB	CBB	CBB
V_{IN} [V] / V_{OUT} [V]		2.7-4.2 / 3.4	2.7-4.2 / 3.4	2.5-4.5 / 3-6	2.3-5 / 1.5-3.6	2.7-4.2 / 3.4	2.2-5 / 1.8-5.2
Max I_{OUT} [A] / Silicon Area [mm^2]		1 / 1.7	1 / 3.2	1 / 3.52	1 / 2.8	1.1 / 5.79	1 / 2.5
On-die Power Density [W/mm^2][(b)]		2	1.05	1.68	1.3	0.65	2.08
Inductor F_{SW} in CCM [MHz]		1	1	2	6	1	$\sim$ 1 - 2.5
L [μH] (DCR [mΩ], thickness [mm])		2.2 (170, 1.2)	4.7 (250, 1.2)	4.7 (9, 4.7)	0.22 (-, -)	4.7 (-, -)	1.5 (69, 1)
Off-chip Total Capacitance [μF]		14.7	30.2[(c)]	20	10	10	14.1
VCR Limits (ideal)		0.5 - 1	0.5 - 2	0 - 2	none	none	none
Line Transient	ΔV_{OUT} [mV]	-	-	5.8	30	-	3.5
	applied ΔV_{IN} [V]	-	-	3.7 $\Leftrightarrow$ 4.2	3.3 $\Leftrightarrow$ 4.4	-	3 $\Leftrightarrow$ 5
Load Step	ΔV_{OUT+} / ΔV_{OUT-} [mV]	270 / 275	160 /150	153 / 210	65 / 70	250 / 300	105 / 120
	applied ΔI_{OUT} [A]	0.5 $\Leftrightarrow$ 1	0 $\Leftrightarrow$ 1	0.1 $\Leftrightarrow$ 1	0.5 $\Leftrightarrow$ 1	0.1 $\Leftrightarrow$ 1	0 $\Leftrightarrow$ 1
PCE [%][(d)]	Peak / Light-Load @ 1mA	97.3 / -	95.5 / -	96.6 / -	91.7 / 82[(e)]	90.9 / -	95.7 / 55

[5] does not operate seamless between modes (i.e., at mode change a large V_{OUT} transient occurs with inrush current due to hard-charging C_{FLY}).
[(a)] DP = dual-path, BS = bilaterally-symmetrical, IL = inductor-last. [(b)] On-die power density = Max I_{OUT} x Max V_{OUT} / Silicon Area.
[(c)] 100 nF capacitors are needed for two charge-pumps. [(d)] PCE = power conversion efficiency (measured). [(e)] Estimated from measurements.

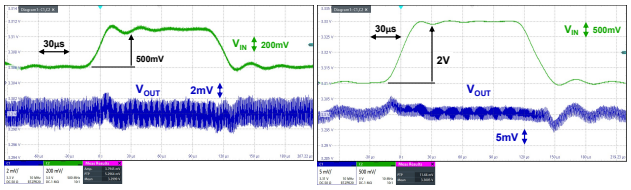

Fig. 7. Measured responses for emulated TDMA noise test (V_{IN} = 3.7 V $\Leftrightarrow$ 4.2 V) with V_{OUT} = 4 V (left), and 2 V/30 μs fast line transient (V_{IN} = 3 V $\Leftrightarrow$ 5 V) at V_{OUT} = 3.3 V (right).

[5]-[7]. Despite the thinnest coil, this work delivers the highest power density, and competitive peak efficiency. Regarding the dynamic responses, the presented BB outperforms the others, exhibiting the highest TDMA noise immunity, as well as minimum overshoot/undershoot during load transients.

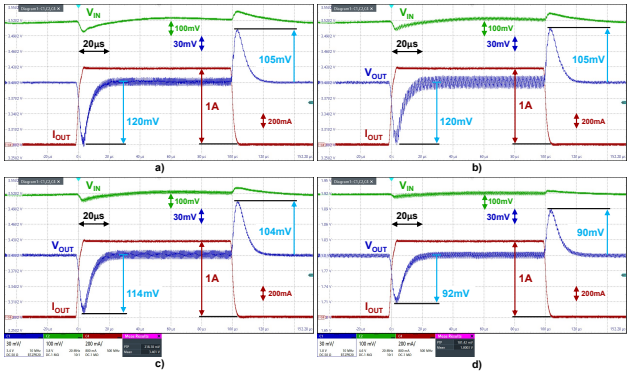

Fig. 8. Load-step transient responses (I_{OUT} = 0 A $\Leftrightarrow$ I_{OUT} = 1 A) with: a) V_{IN} = 2.7 V and V_{OUT} = 3.4 V, b) V_{IN} = V_{OUT} = 3.4 V, c) V_{IN} = 4.2 V and V_{OUT} = 3.4 V, d) V_{IN} = 5 V and V_{OUT} = 1.8 V.

IV. CONCLUSION

A novel BB with a modified hysteretic current-mode control has been presented. This new BB controller allows to reach a superior rejection of TDMA noise, outperform state-of-the-art converters on the load transient responses while guaranteeing seamless transition between modes, making the presented converter particularly suited for OLED displays. In contrast to hybrid converters that pose extra costs due to added external components and exhibit VCR limitations, the proposed converter is particularly attractive for highly dense and efficient consumer applications.

REFERENCES

[1] F. Mao et. al., "A hybrid single-inductor bipolar triple-output dc–dc converter with high-quality positive outputs for amoled displays," in *IEEE Trans. on Circ. and Sys. I*, vol. 70, no. 1, pp. 506–517, Jan. 2023.
[2] Manish Kumar Barwar et. al., "Demystifying the Devices Behind the LED Light: LED Driver Circuits," in *IEEE Industrial Electronics Magazine*, vol. 17, no. 1, pp. 55–66, 2023.
[3] S. Park et. al., "Modeling, measurement, and analysis of audio frequency ground integrity for a TDMA smartphone system," in *IEEE Trans. Compon., Packag. Manuf. Tech.*, vol. 8, no. 4, pp. 519–530, Apr. 2018.
[4] Yuge Huang et. al., "Mini-LED, micro-LED and OLED displays: Present status and future perspectives," in *Light: Science & Applications*, vol. 9, no. 1, pp. 1–16, June 2020.
[5] Ji Jin et al., "A Battery-to-3.4 V Hybrid Buck-Boost Converter With Always Reduced Conduction Loss," in *IEEE Journal of Solid-State Circuits*, vol. 60, no. 6, pp. 2194–2205, June 2025.
[6] Dae-Hyeon Kim et al., "A Power-Efficient Single-Mode Buck–Boost DC–DC Converter With Bilaterally Symmetrical Hybrid Topology," in *IEEE J. of Solid-State Circ.*, vol. 59, no. 12, pp. 4137–4149, Dec. 2024.
[7] J.-H. Kim et al., "A Single-Duty-Cycled Buck–Boost Converter Achieving Low Output Ripple and Seamless Mode Transition," in *IEEE Journal of Solid-State Circuits*, vol. 60, no. 4, pp. 1248–1264, April 2025.
[8] Manmeet Singh and Ayman A. Fayed, "A 1-A 6-MHz Digitally Assisted Buck–Boost Converter With Seamless Mode Transitions and Fast Dynamic Performance for Mobile Devices," in *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4338–4351, April 2021.
[9] Ki-Duk Kim et. al., "A Noninverting Buck–Boost Converter With State-Based Current Control for Li-ion Battery Management in Mobile Applications," in *IEEE Trans. on Ind. Ele.*, vol. 66, no. 12, Dec. 2019.