A SAW-Referenced PLL achieving 19.2-fs Jitter in Integer-N Mode and ±1.5-ppm Frequency Stability in Temperature Compensated Fractional-N Mode

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***Abstract*—This paper presents a 303-MHz surface-acoustic-wave (SAW) oscillator reference for a complementary charge-sampling PLL and a temperature-compensated frequency generator. To achieve low jitter and low close-in phase noise, a SAW driver with dynamic resistance tuning and tail resonance filtering is introduced, while a high-gain complementary charge-sampling phase detector suppresses in-band noise with low power. In the temperature-compensation mode, a digital fractional-N PLL combined with a low-noise temperature-sensing and filtering path corrects the SAW frequency drift. In integer-N Mode, the prototype achieves 19.2 fs RMS jitter at 11.24 GHz with 28.4 mW power consumption, corresponding to a -260 dB FoM. In fractional-N mode, it attains ±1.5 ppm frequency stability with 72 fs jitter and 42.3 mW power.**

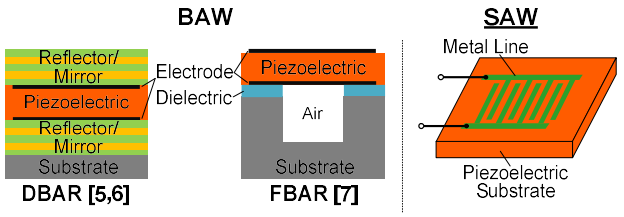
Keywords—surface acoustic wave oscillator, charge-sampling PLL, fractional-N PLL, temperature compensation

I. Introduction

Modern communication systems and consumer electronics require clock generators with low jitter, low phase noise (PN), low power consumption, and good frequency stability over temperature. Quartz crystal resonators provide a high quality factor (Q>50k) and excellent temperature stability (<20 ppm). However, using a crystal oscillator (XO) as the reference of a phase-locked loop (PLL) makes low-jitter generation difficult for two reasons. First, the slow sinusoidal XO waveform requires a large power-hungry squaring buffer to achieve low PN. Second, the XO frequency is typically below 100 MHz, so the large multiplication ratio in the PLL degrades the in-band PN. For example, [1] achieves 16.1 fs jitter with eight 100 MHz XOs, but at the cost of 1 W power consumption, whereas designs with a similar reference frequency exceed 30 fs jitter [2]-[4]. A higher reference frequency is therefore attractive for improving power efficiency. Although overtone-mode XOs can exceed 200 MHz, they often suffer from lower Q and higher motional resistance. Alternatively, gigahertz-range bulk acoustic wave (BAW) [5], [6] and film bulk acoustic resonator (FBAR) oscillators [7] offer higher reference frequencies, as shown in Fig. 1. State-of-the-art BAW oscillators [5], [8] achieve <15 fs jitter with <30 mW power consumption, but their moderate frequency stability and relatively low Q (<2000) still degrade the close-in PN.

II. SAW-Referenced Dual-Mode PLL

To address these limitations, this work uses a surface acoustic wave (SAW) oscillator as a low-jitter, low-close-in-PN reference. As shown in Fig. 1, the SAW resonator uses interdigital transducers on a piezoelectric substrate to enable



	Crystal	BAW [5-7]	SAW [15]
Quality Factor	High(>50k)	Low(<2k)	High(>10k)
Resonant Freq. [MHz]	Low(<100)	High(>1000)	High(>300)
Temp. Sensitivity [ppm]	Low(~20)	High(~100)	High(~150)

Fig. 1. Comparison of crystal, BAW, and SAW resonators in terms of structure and key metrics.

bidirectional electro-acoustic transduction, providing an operating frequency> 3× that of quartz crystals, >5× the Q of BAW/FBAR resonators, low cost, and a compact footprint [9]. The proposed system supports two modes: an integer-N complementary charge-sampling phase-locked loop (CCSPLL) mode and a temperature-compensated fractional-N phase-locked loop (FNPLL) mode. The on-chip SAW driver employs dynamic swing boosting and tail filtering to generate a low-PN 303 MHz reference. In the integer-N mode, a high-gain complementary charge-sampling phase detector (CCSPD) suppresses the in-band PN with low power. In the temperature-compensated mode, the phase error is digitized by a phase-frequency detector (PFD), a pulse-width-to-voltage converter (PVC), and a 1-bit first-order continuous-time delta-sigma analog-to-digital converter (CT delta-sigma ADC).

A. Architecture and Operating Modes

Fig. 2 shows the system block diagram. In the integer-N mode, the CCSPLL is driven directly by the 303 MHz fundamental output of the SAW oscillator, and the digital FNPLL path is disabled. In the temperature-compensated mode, the integer-N path is disabled, and the digital FNPLL, along with the temperature-compensation loop, is enabled. The compensation code generated by the temperature sensor and digital filter is added to the frequency command word (FCW) to adjust the output frequency. A 32-bit third-order digital delta-sigma modulator (DSM) controls the feedback divider and provides 0.23 ppb frequency resolution. To suppress DSM-induced spurs and close-in PN degradation, the DSM is dithered with a differentiated pseudo-random number generator (PRNG). The DSM runs at 606 MHz, twice the reference frequency, which lowers the quantization-noise contribution and supports loop

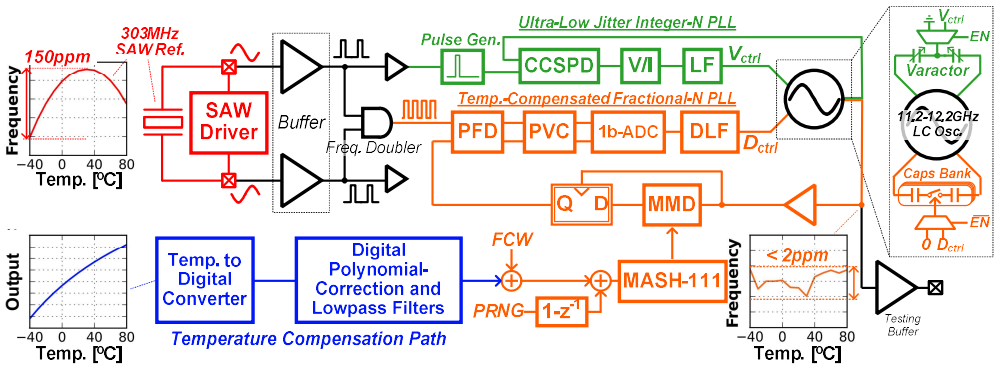
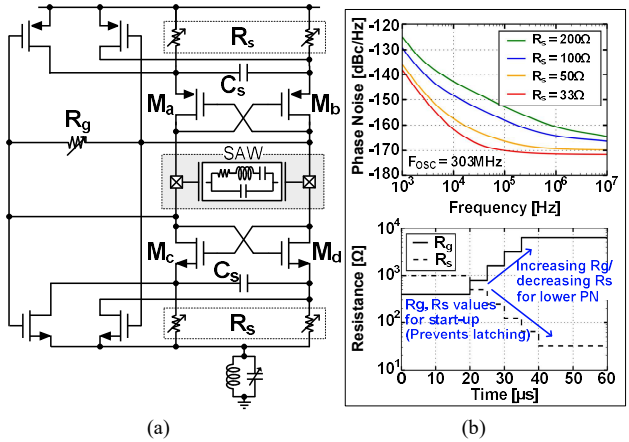


Fig. 2. The proposed PLL system using SAW resonator as a reference clock.



(a) (b)

Fig. 3. (a) schematic of the proposed SAW driver and (b) simulated phase noise and startup procedure.

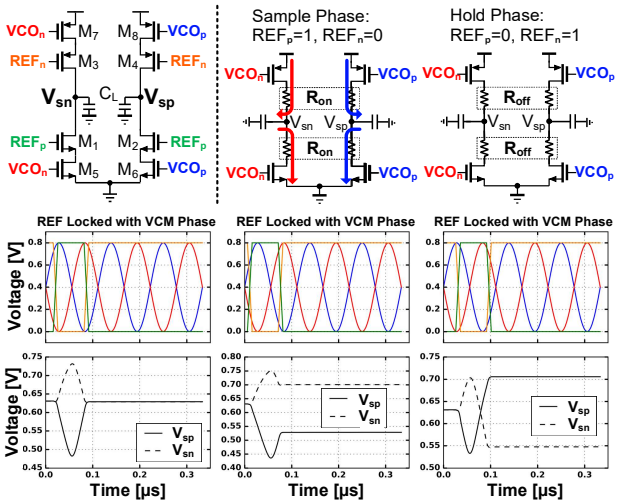


Fig. 4. The operation principle of the proposed complementary charge-sampling phase detector (CCSPD).

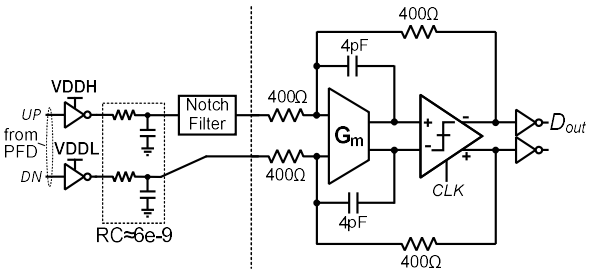
bandwidths above 1 MHz. A PFD and a linear PVC accommodate phase errors of up to four digitally controlled oscillator (DCO) periods arising from DSM quantization and deterministic jitter from the reference doubler, thereby preventing significant noise folding. The PVC output is digitized by the 1-bit first-order CT delta-sigma ADC, and the resulting digital signal is filtered before controlling the DCO. Note that power overhead of the PVC and ADC remains negligible compared to overall power consumption.

B. SAW Driver and Charge-Sampling Phase Detector

Fig. 3(a) shows the SAW resonator driver. The resonator has a typical motional resistance of 20 ohm, a motional inductance of 80 mH, and an unloaded quality factor of 12k. Source-degeneration capacitors (C_s) and resistors (R_s) suppress megahertz-range RC relaxation oscillation. A 3-bit tunable resistor (R_g) biases the resonator, whose high dc impedance can otherwise cause dc latch-up. A reliable start-up requires R_g to be much smaller than R_s, but this condition reduces the oscillation amplitude and worsens the PN. To relax this trade-off, the proposed driver dynamically tunes R_g and R_s, as shown in Fig. 3(b). At start-up, R_g is set smaller than R_s to guarantee oscillation. After start-up, both resistors are adjusted stepwise to maximize the swing, which improves the simulated PN by 10 dB at 1 MHz offset. Large swings can also force transistors M_a-M_d into the triode region, lowering the effective resonator Q and increasing the PN. To prevent this effect, a common-mode resonant network is placed at the tail node so that the LC tank presents a high impedance at 606 MHz. The 5 nH tail inductor is implemented with a 9-turn inductor (0.05 mm^2), and a 6-bit capacitor array tunes the resonance against process variation. Fig. 4 shows the complementary charge-sampling phase detector. When the reference is high (REF_p=1 and REF_n=0), switches M_1-M_4 turn on, and transconductance devices M_5-M_8 together with the load capacitors (C_L) integrate the phase error between the voltage-controlled oscillator (VCO) and the reference into the differential outputs V_{sn} and V_{sp}. As in prior NMOS-only samplers [2], [10], the reference samples the VCO zero crossing in lock. Unlike prior designs, the proposed phase detector minimizes common-mode variation even with small sampling capacitance, increasing the detector gain by more than 5× to 2 V/rad. The resulting in-band phase-detector and voltage-to-current converter noise is suppressed to -140 dBc/Hz at an 11 GHz output while consuming only 0.23 mW. During the low phase of the reference (REF_p=0 and REF_n=1), M_1-M_4 behave as large resistors (R_{off}), so the sampling capacitor partially discharges through R_{off} and forms a lossy integrator. This pole requires a small sampling capacitor for stability. Simulations show that with a 10 MHz loop bandwidth, the phase margin degrades by less than 5 degrees for sampling capacitors below 50 fF across process, voltage, and temperature (PVT) variations.

C. Temperature-Sensing and Compensation Circuitry

Fig. 5 shows the schematics of the PVC and the 1-bit CT delta-sigma ADC. The PVC uses two inverters followed by RC filters to attenuate high-frequency DSM noise. Two



(a) (b)

Fig. 5. Schematics of (a) pulse-width-to-voltage converter and (b) 1b ADC.

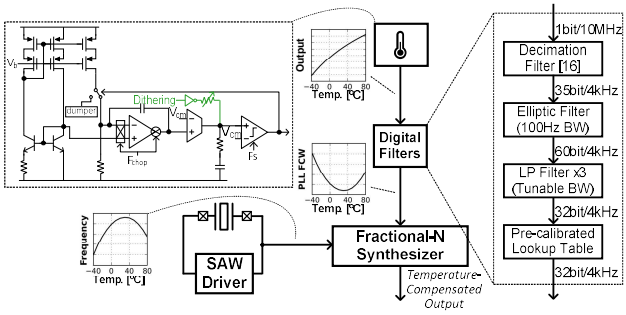


Fig. 6. Block diagram of the temperature compensation path.

supply voltages, VDDH and VDDL, create a fixed time offset equal to 0.5·(1-VDDL/VDDH) times the reference period between the reference and feedback paths. This delay keeps the PFD and PVC in their linear operating region when the PLL is locked, so only UP pulses carry phase information and DSM noise folding is reduced. The thermal noise of the ADC is designed to avoid in-band PN degradation, and its quantization noise is negligible thanks to its high operating speed. Fig. 6 shows the temperature-compensation loop. A temperature sensor measures the chip temperature, and its digitally filtered output corrects the SAW frequency drift by adjusting the frequency multiplication ratio. The sensor uses an NPN-based front end followed by a second-order CT delta-sigma ADC [11], which removes the need for a power-hungry error amplifier. Dynamic element matching (DEM) and chopping suppress flicker noise in the current sources and first integrator, thereby reducing close-in PN degradation. An on-chip PRNG dithers the comparator input to avoid tonal behavior when the bitstream is near 0.5. To prevent the temperature-sensor noise from degrading the PLL output, the bitstream is first processed by a sinc^3 decimation filter [16], then by a fifth-order elliptic low-pass filter, and finally by a third-order bandwidth-programmable low-pass filter. A fifth-order polynomial correction filter then linearizes the strongly nonlinear temperature dependence of the SAW resonator.

III. Measurement Results

A. Phase Noise, Jitter, and Power Consumption

The prototype, which includes the SAW-driven CCSPLL in the integer-N mode and the temperature-compensated frequency generator in the temperature-compensated mode, was fabricated in a 22 nm FDSOI process. Fig. 7 shows the die micrograph and power breakdown. The circuit consumes 28.4 mW in the integer-N mode and 42.3 mW in the temperature-compensated mode. As shown in Fig. 8(a), the

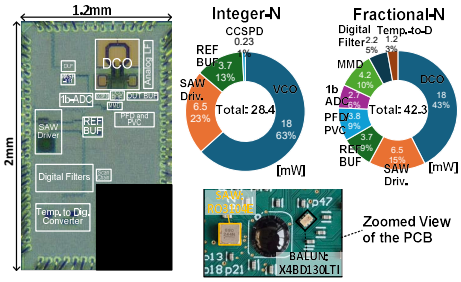


Fig. 7. Die micrograph, power breakdown, and zoomed PCB view.

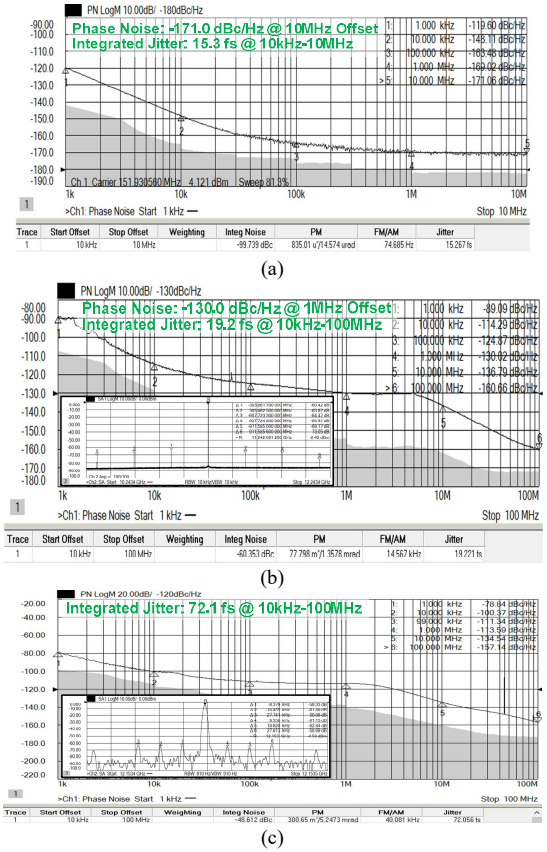
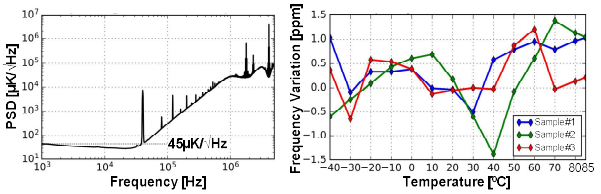


Fig. 8. Measured phase noise of (a) the SAW oscillator, (b) the integer-N PLL output, and (c) the temperature-compensated fractional-N PLL output.

SAW oscillator achieves a state-of-the-art PN floor of -171 dBc/Hz at 10 MHz offset and 15.3 fs integrated jitter from 10 kHz to 10 MHz. As shown in Fig. 8(b), the integer-N output exhibits an in-band noise floor of -130 dBc/Hz and 19.2 fs rms jitter integrated from 10 kHz to 100 MHz at 11.24 GHz. In the temperature-compensated fractional-N mode, the measured integrated jitter is 72 fs from 10 kHz to 100 MHz while providing ±1.5 ppm frequency stability. The measured fractional spur is below -59 dBc.

B. Measured Temperature-Sensing and Stability Results

Fig. 9(a) shows the measured power spectral density (PSD) of the temperature sensor before decimation. The spectrum is thermal-noise limited up to 20 kHz, with a floor of 45 μK/√Hz. Tones at multiples of 40 kHz arise from DEM and chopping. Fig. 9(b) shows that three measured chips achieve a frequency stability better than ±1.5 ppm from -40 ºC to +85 ºC.



(a) (b)

Fig. 9. Measured temperature-sensor and frequency-stability results: (a) PSD of the temperature sensor and (b) measured frequency variation.

TABLE I
COMPARISON WITH VARIOUS OSCILLATORS

	This Work	ISSCC'25 [13]	ISSCC'23 [5]	RFIC'22 [6]	RFIC'21 [7]	JSSC'19 K. M. Megawer	JSSC'19 A. Karimi-Bidhendi	JSSC'18 K. M. Lei	JSSC'16 S. Iguchi
Resonator Type	SAW	Crystal	BAW	BAW	FBAR	Crystal	Crystal	Crystal	Crystal
Motion Resistance [Ω]	16	8 to 20	N/A	N/A	N/A	11.25	15	19	10
Motion Inductance [mH]	0.085	0.5 to 1.2	N/A	N/A	N/A	3.3	2.749	11.1	4
Quality Factor	10k	30k to 75k	N/A	>1000	N/A	100k	55k	88k	98k
Frequency [MHz]	303.8	96	2500	2520	2492	54	48	24	39
Power [mW]	6.5	2.4	N/A	0.675	0.416	0.198	0.18	0.0318	0.181
PN @1kHz [dBc/Hz] Norm. to 100MHz Carrier	-130.1	-133.8	N/A	-104.8	-107*	-134.2	-128.6	-121.6*	-138.8
PN @1MHz [dBc/Hz] Norm. to 100MHz Carrier	-172.5	-166.5	-160/9	N/A	-168*	-157.8	N/A	-143.6*	-166.8
FoM @1kHz [dB]	222.0	230.0	N/A	206.5	209*	241.2	236.1	236.6*	246.2
FoM @1MHz [dB]	204.4	202.7	N/A	N/A	212*	204.8	N/A	198.6*	214.2

*Estimate from data

C. Comparison with Prior Work

Table I compares the proposed reference with prior low-PN oscillators and shows low PN at both 1 kHz and 1 MHz offsets. Note that in our measurement, the noise of the 3.7 mW reference buffer is included. Table II shows that, among prior low-jitter integer-N PLLs, only [12] achieves 1.9 dB better conventional FoM, but its system FoM (FoMs) degrades by 8.8 dB once the reference power is included. Compared with [13], the proposed work achieves 3.3× lower jitter, a 4.6 dB better FoMs, and 5× smaller area. Relative to [1] and [14], the proposed work reduces the PLL-core power by more than 3.6× and the reference power by more than 26×, while improving the FoM and FoMs by at least 4 dB and 7.7 dB, respectively. Table III further shows that, among prior temperature-compensated frequency generators, the proposed design achieves the lowest jitter while maintaining competitive frequency stability and low power.

IV. CONCLUSION

This work presents a SAW-referenced frequency generator that combines a low-close-in-PN SAW oscillator, a complementary charge-sampling PLL, and a digital temperature-compensation loop. Fabricated in a 22 nm FDSOI process, the prototype achieves 19.2 fs rms jitter and a -260 dB system FoMs in the integer-N mode, and ±1.5 ppm frequency stability with 72 fs integrated jitter in the temperature-compensated mode.

ACKNOWLEDGMENT

This project was supported by the SNSF Starting Grants 2022 (#211210). The authors would like to thank GlobalFoundries for providing silicon fabrication through the 22FDX university program.

TABLE II
INTEGER-N PLL COMPARISON

	This Work	ISSCC'25 [14]	JSSC'24 [1]	JSSC'23 [12]	ISSCC'25 [13]	JSSC'25 [17]	RFIC'20 [2]
Process	22nm FDSOI	65nm CMOS	65nm CMOS	28nm CMOS	22nm FDSOI	7nm FinFET	40nm CMOS
Architecture	CCSPLL	CPPLL	SPLL	SPLL	SSPLL	XOR-PLL	CSPLL
Fref [MHz]	303	250	100	250	96	2285	100
Fout [GHz]	11.24 to 12.15	13	4.8 to 5.6	20	4.6	4.8 to 5	9.8 to 12.2
Ref Spur [dBc]	-60	-98.5	-71	-66	-71.7	<-70*	-65.7
RMS Jitter [fs]	19.2	15.8	16.1	20.9	63.3	91	50.5
Integration BW [Hz]	10k to 100M	10k to 100M	10k to 40M	10k to 40M	1k to 100M	10k to 100M	1k to 100M
Power [mW]	21.9	79.5	83	12	5.08	0.96	5
Ref. Osc. Power [mW]	6.5	170	1000†	170	2.38	N/A	150
Core Area [mm²]	0.21	0.518	1.1	0.06	1.14	0.18	0.13
FoM [dB] (w/o Ref. Osc. Pwr.)	-260.9	-257	-256.7	-262.8	-256.9	-261	-258.9
FoMs [dB] (w/ Ref. Osc. Pwr.)	-259.8	-252.1**	-245.5**	-251.0**	-255.2	N/A	-244.0**

*Referred to 5GHz **Not optimized for FoMs †Using 8 VCXOs

TABLE III
TEMPERATURE-COMPENSATED FREQUENCY GENERATOR COMPARISON

	This Work	ISSCC'23 [5]	Skyworks Si545	SiTime SiT9366	ISSCC'20 [8]	ISSCC'12 [18]
Process	22nm FDSOI	65nm CMOS	N/A	N/A	65nm CMOS	180nm CMOS
Resonator	SAW (303MHz)	BAW (2.5GHz)	Crystal	MEMS	BAW (2520MHz)	MEMS (48MHz)
TC Topology	Frac PLL	FOD	Frac PLL	Frac PLL	Frac PLL	Frac PLL
Freq Range	11.5 to 12.2GHz	0.5 to 400MHz	15 to 2100MHz	1 to 220MHz	2400	0.5 to 220
Freq. Stability [ppm]	±1.5	±4	±7	±10	±10	±0.2
Temp. Range [°C]	-40 to 85	-40 to 85	-40 to 85	-40 to 105	-40 to 85	-40 to 85
Jitter [fs]	72 (10K to 100MHz)	88** (12K to 20MHz)	80 (12K to 20MHz)	225 (12K to 20MHz)	N/A	573 (12K to 20MHz)
PN@1kHz [dBc/Hz]*	-123.7	N/A	-136.9	N/A	-103.6	N/A
PN@1MHz [dBc/Hz]*	-151.3	-160.9	-155.9	N/A	N/A	N/A
Supply Current [mA]	30	69	107	89	N/A	33
Power [mW]	42.3	N/A	193	223	1.4***	109
Active Area [mm²]	0.47	N/A	N/A	N/A	1.36	N/A

*Normalized to 100MHz carrier **Only FOD jitter ***Only oscillator and divider

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