Cryogenic Vertical Nanowire Anti-Ambipolar Transistor with Low-Voltage Operation

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***Abstract*—The electrical characteristics of a vertical III–V nanowire anti-ambipolar transistor are evaluated down to 10 K. The InAs–GaSb heterostructure in gate-all-around geometry combines strong electrostatic control with compact geometry. Transfer characteristics are measured at two drain biases, and the key anti-ambipolar figures of merit are extracted across the temperature range. A strong cryogenic enhancement is observed, with reduced valley currents, sharper transfer characteristics, and strongly improved peak-to-valley ratio at low temperature. Benchmarking against previously reported cryogenic anti-ambipolar devices shows that the vertical nanowire platform is highly competitive and promising for scaled low-temperature electronics.**

***Index Terms*—III–V, vertical transistor, nanowire, anti-ambipolar, negative transconductance, cryogenic.**

I. Introduction

Anti-ambipolar transistors (AATs) are an emerging transistor technology that is being explored for applications beyond CMOS. The AAT is a device whose transfer characteristic is non-monotonic and exhibits a peak current within a specific gate-voltage range combined with a region of negative transconductance (g_{m}) [1]. AATs are promising building blocks for multivalued logic, fast-switching devices, and oscillator circuits [1]. In particular, for ternary logic concepts, AATs can provide a low-leakage conduction path by confining current flow to a narrow voltage window [2]. In addition, AAT behavior has been integrated into vertical nanowire FETs with ferroelectric gate oxides to switch analog functionality, potentially enabling ultra-compact analog signal processing and content-addressable memories [3], [4]. The key figures of merit used to assess AAT performance are the peak drain current ($I_{\mathrm{D,peak}}$), the gate voltage at peak current ($V_{\mathrm{G,peak}}$), the peak-to-valley ratio (PVR), and the on-state window (ΔV_{on}).

As logic and mixed-signal technologies continue to scale, there is an increasing demand for new device functionality and concepts that combine a small footprint, strong electrostatic control, and advanced alternative channel materials. One such technology is the vertical nanowire field-effect transistor (VNWFET), which is particularly attractive because the channel length, source and drain contacts, and device footprint can be decoupled from one another, enabling dense integration while maintaining excellent electrostatic control through the gate-all-around geometry [5]. Among the candidate material systems, III–V semiconductors, and InAs in particular, have shown excellent performance in metal-oxide-semiconductor field-effect transistors (MOSFETs) [6]. This performance is enabled by the high carrier mobility and injection velocity of InAs. However, InAs naturally favors n-type conduction, so additional materials must be co-integrated to realize p-type device functionality. One such material is GaSb, for which p-type nanowire MOSFETs have already been demonstrated. Moreover, GaSb is compatible with vapor–liquid–solid (VLS) growth on InAs substrates and has also been demonstrated on InAs buffer layers grown on Si wafers [7].

Although modern integrated electronics build on n- and p-MOS devices, whose scalability and low static power make them excellent for digital IC design, a growing number of complementary device technologies are emerging. These non-CMOS devices exhibit figures of merit that, while not necessarily optimal for logic circuits, are advantageous in other applications. Furthermore, for quantum and cryogenic integrated systems, it becomes essential to develop electronics that operate not only at ambient conditions but also with high performance at cryogenic temperatures. Several AAT concepts have previously been characterized at cryogenic temperatures, yet such studies remain sparse and, to the best of our knowledge, none have been reported for a vertical nanowire geometry [8]–[11]. In this study, the temperature-dependent electrical characteristics of a III–V nanowire AAT are investigated down to 10 K. By analyzing the transfer characteristics (I_{D}–V_{G}), the key AAT figures of merit are extracted. Specifically, the peak current, peak position, peak-to-valley ratio, and on-state window are evaluated as functions of temperature for two drain voltages. Strong thermal effects are observed in all these metrics, highlighting the importance of cryogenic characterization. In addition, the extracted figures of merit are benchmarked across the full temperature range against previously reported AAT technologies studied at cryo-

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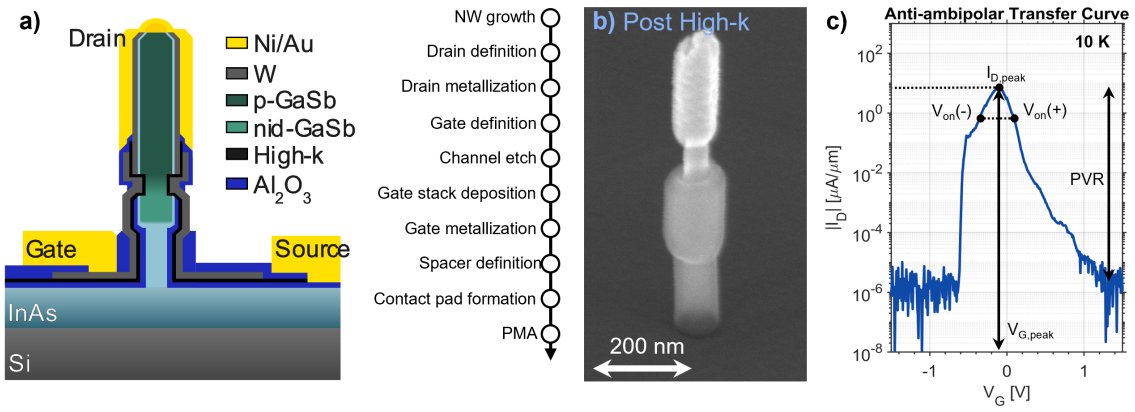

Fig. 1. (a) Cross-sectional schematic of the vertical nanowire field-effect transistor exhibiting anti-ambipolar transfer characteristics (not to scale), together with the main fabrication steps. (b) SEM image of an example device during fabrication, acquired after deposition of the high-k layer. (c) Anti-ambipolar transfer characteristics of the transistor measured at 10 K.

genic temperatures. The results show that the vertical nanowire platform is competitive across all relevant metrics and, when combined with its small footprint, is a strong candidate for scaled AAT implementations operating at low temperatures.

II. Device Fabrication and Experimental Setup

InAs–GaSb nanowires (NWs) were grown by metal-organic vapor phase epitaxy (MOVPE) using the VLS technique on a prepatterned Si wafer with an n^+-InAs buffer layer. The NW consists of an n-type Sn-doped InAs bottom section, which forms the source and the InAs/GaSb tunneling junction, a non-intentionally doped GaSb channel section (nid-GaSb), and a Zn-doped p-type GaSb drain section. In addition, a Sn-doped n^+-InAs shell covers the GaSb drain section. Transistor fabrication followed a gate-last process that began with the formation of the drain contact. An alumina spacer was deposited and selectively removed in the drain region using a resist etch-back process to define the drain-contact length. The W drain contact was then sputtered and anisotropically etched, leaving metal on the NW sidewall. The resist was further thinned to define the gate length, after which the alumina in the gate region was removed. The GaSb-based channel diameter was reduced by 20 nm (from approximately 55 nm) using digital etching, and a bilayer high-k gate dielectric (Al_2O_3/HfO_2) with an equivalent oxide thickness of approximately 1 nm was deposited by atomic layer deposition (ALD) after a final native-oxide etch (1:10 HCl, 30 s). The gate metal (W) was subsequently sputtered and patterned. The device was completed by a second spacer definition, contact metallization, and post-metallization annealing (PMA). A schematic illustration of the device is shown in Fig. 1(a), together with a process flow summarizing the main processing steps. The device geometry was characterized by scanning electron microscopy (SEM). An example SEM image acquired mid-processing is shown in Fig. 1(b). From SEM, the nanowire channel diameter was determined to be 35 nm. The nanowire circumference was used as the normalization length for the drain current. A more detailed process description is given by Zhu et al. [12]. Electrical characterization was carried out in a Lake Shore CRX-6.5K cryogenic probe station over a temperature range extending down to 10 K using a B1500A parameter analyzer.

III. Experimental Results

An example anti-ambipolar transfer curve measured at 10 K for a gate-voltage sweep from -1.5 V to 1.5 V is shown in Fig. 1(c). The graph highlights the key AAT performance metrics: $I_{\mathrm{D,peak}}$, $V_{\mathrm{G,peak}}$, $V_{\mathrm{on}}(\pm)$, and PVR. Here, ΔV_{on} is defined as $|V_{\mathrm{on}}(+) - V_{\mathrm{on}}(-)|$, where $V_{\mathrm{on}}(\pm)$ is extracted at 10% of $I_{\mathrm{D,peak}}$ to simplify benchmarking across platforms. The transfer characteristic contains a region of negative transconductance after the peak current, unlike a conventional MOSFET. The anti-ambipolar behavior arises from gate-dependent alignment of the two heterojunction regions in the device. At negative gate bias, band-to-band tunneling can occur at the n^{++}-InAs/nid-GaSb junction, but the total current is limited by a barrier in the gated nid-GaSb/p-GaSb region. As V_{G} is increased toward $V_{\mathrm{G,peak}}$, this barrier is lowered, completing the conduction path and maximizing the current. At more positive gate bias, the gate reduces the tunneling probability at the InAs/nid-GaSb junction by decreasing the local band overlap and increasing the effective tunneling width. This gives rise to negative transconductance and the falling right-hand branch of the transfer curve. Notably, these effects occur at expected voltages given the nature of the material system and the gate geometry.

In Fig. 2(a)–(d), the transfer characteristics are plotted for both gate-bias ranges and the two drain voltages. Figs. 2(a) and 2(b) show the I_{D}–V_{G} data at $V_{\mathrm{D}} = 500$ mV for negative and positive gate sweeps, respectively. For the negative sweep, the highest currents are observed at 250 K and 200 K, reaching approximately 20 μA/μm. As the device is cooled down, a change in temperature-dependent transport regime likely also contributes to the apparent shift in the threshold voltage with temperature. As the temperature is reduced below 100 K,

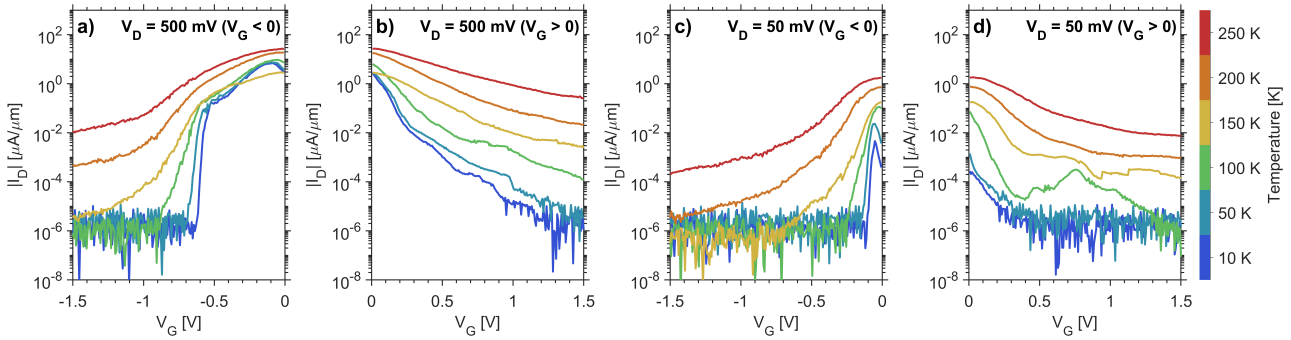

Fig. 2. Anti-ambipolar transfer characteristics (I_{D}–V_{G}) of the device at different temperatures: (a) negative gate-voltage sweeps at $V_{\mathrm{D}} = 500$ mV, (b) positive gate-voltage sweeps at $V_{\mathrm{D}} = 500$ mV, (c) negative gate-voltage sweeps at $V_{\mathrm{D}} = 50$ mV, and (d) positive gate-voltage sweeps at $V_{\mathrm{D}} = 50$ mV.

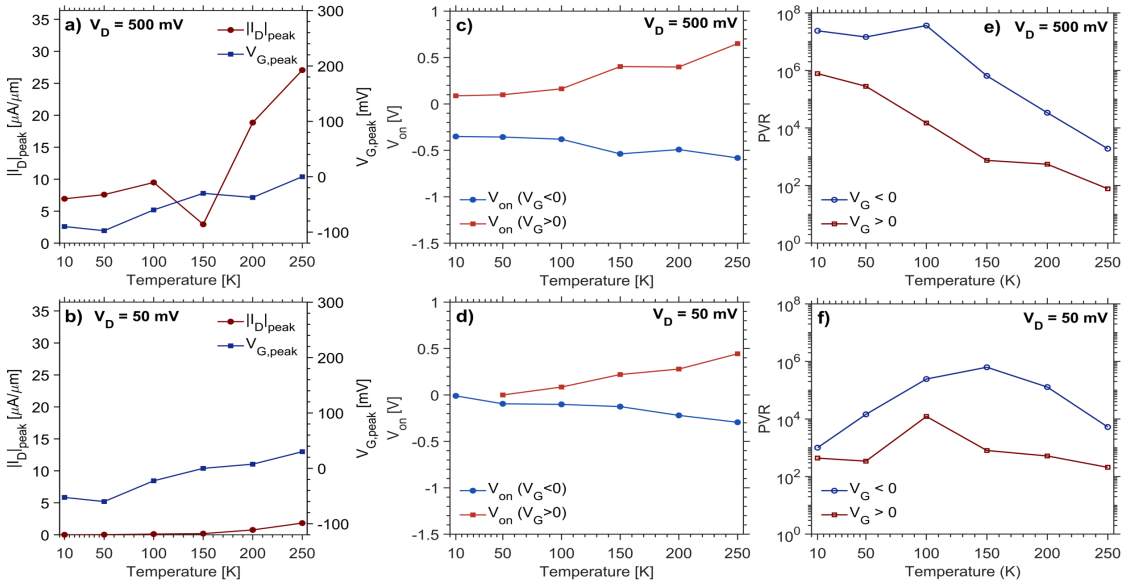

Fig. 3. Extracted anti-ambipolar figures of merit as a function of temperature. (a) $I_{\mathrm{D,peak}}$ and $V_{\mathrm{G,peak}}$ at $V_{\mathrm{D}} = 500$ mV. (b) $I_{\mathrm{D,peak}}$ and $V_{\mathrm{G,peak}}$ at $V_{\mathrm{D}} = 50$ mV. (c) V_{on} for negative and positive gate bias at $V_{\mathrm{D}} = 500$ mV. (d) V_{on} for negative and positive gate bias at $V_{\mathrm{D}} = 50$ mV. (e) PVR at $V_{\mathrm{D}} = 500$ mV. (f) PVR at $V_{\mathrm{D}} = 50$ mV.

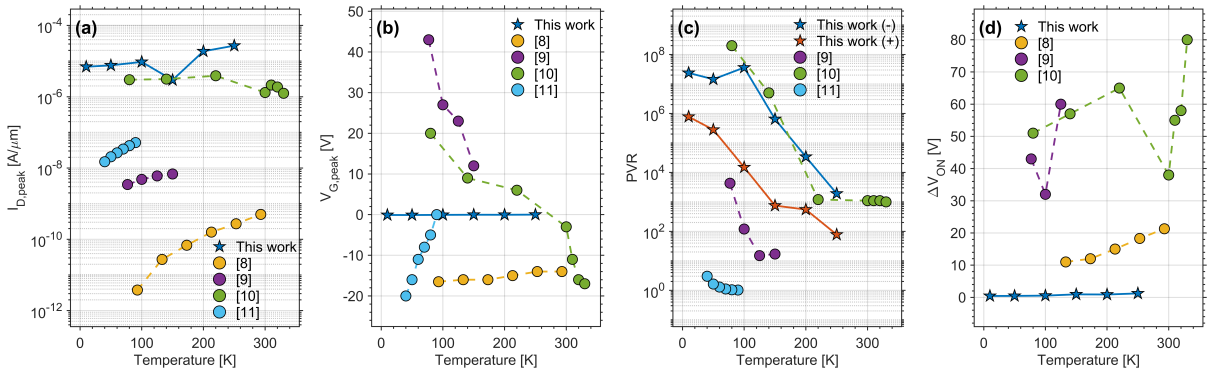

Fig. 4. Benchmarking of anti-ambipolar figures of merit as a function of temperature: (a) $I_{\mathrm{D,peak}}$, (b) $V_{\mathrm{G,peak}}$, (c) PVR, and (d) ΔV_{on}. Literature values were digitized and extracted from published transfer curves where not explicitly reported.

the transport appears increasingly tunneling-dominated. At the three lowest temperatures, the off-state current approaches the measurement floor, while a residual current bump remains near -0.2 V, as can be seen in Fig. 2(a). This feature is likely related to a temperature-induced shift in the conditions that lead to the onset of conduction, possibly related to the suppression of thermally activated carrier transport. Between 50 K and 10 K, only minor additional changes are observed, suggesting that the dominant thermal effects have largely saturated. The positive sweep at the same drain bias is shown in Fig. 2(b). Here, the transfer curves evolve less dramatically with temperature, indicating that a different transport-limiting mechanism dominates on this side of the peak, which is consistent with the asymmetric heterostructure discussed above. Similar trends are observed at $V_{\mathrm{D}} = 50$ mV in Figs. 2(c) and 2(d). The lower drain bias reduces drain-field-induced effects at the junctions and therefore produces slightly different conduction characteristics. The strongest low-bias effects appear at the lowest temperatures, where the current peak becomes substantially sharper, corresponding to a smaller ΔV_{on}. While this is beneficial for applications such as multivalued logic and frequency doubling, the substantially reduced current levels at low drain bias may limit practical circuit use.

From Fig. 2(a)–(d), the previously defined AAT figures of merit are extracted and summarized in Figs. 3(a)–(f). Figs. 3(a) and 3(b) show $I_{\mathrm{D,peak}}$ and $V_{\mathrm{G,peak}}$ as functions of temperature for $V_{\mathrm{D}} = 500$ mV and $V_{\mathrm{D}} = 50$ mV, respectively. As expected, $I_{\mathrm{D,peak}}$ decreases markedly when the drain bias is reduced. Importantly, the peak position remains relatively stable for both drain-bias conditions, staying close to zero gate bias. A weak drift toward larger $|V_{\mathrm{G,peak}}|$ is observed with decreasing temperature in both cases. Figs. 3(c) and 3(d) show the extracted V_{on} across temperatures for the two drain biases. The narrow current peak is generally maintained throughout the temperature range. Some data points are omitted because the corresponding sweep does not satisfy the 10% of $I_{\mathrm{D,peak}}$ criterion used to define V_{on}. Finally, the PVR is plotted as a function of temperature for $V_{\mathrm{D}} = 500$ mV in Fig. 3(e) and for $V_{\mathrm{D}} = 50$ mV in Fig. 3(f). At $V_{\mathrm{D}} = 500$ mV, the PVR becomes exceptionally high at low temperature, exceeding 10^7 for the negative sweep. By 100 K, the extracted PVR is already limited by the measurement floor. The positive sweep exhibits a lower PVR, since the corresponding off-state current reaches the measurement noise floor only at larger gate voltages. At $V_{\mathrm{D}} = 50$ mV, the lower peak currents suppress the achievable PVR across both high and low temperatures.

Figs. 4(a)–(d) benchmark the extracted figures of merit against other AAT platforms, including organic DNTT/PTCDI-C_{13} [8], vertically stacked p-SnS/n-$MoSe_2$ [9], an $As_{0.4}P_{0.6}$/$PdSe_2$ van der Waals heterojunction [10], and multilayer MoS_2 [11]. For all devices, $I_{\mathrm{D,peak}}$ is normalized by the reported or estimated gate width; for the present device, the nanowire circumference is used. While current normalization by gate width enables first-order comparison across platforms, differences in device geometry and current flow path should still be kept in mind. Metrics that could not be reliably extracted from the literature were excluded from the comparison. The benchmark shows that the vertical nanowire AAT is competitive across all key metrics and is particularly strong in voltage-related performance, exhibiting near-zero $V_{\mathrm{G,peak}}$ and small ΔV_{on} across the temperature range while maintaining high $I_{\mathrm{D,peak}}$ and PVR.

IV. Conclusion

A vertical nanowire anti-ambipolar transistor has been characterized down to 10 K. Cryogenic operation substantially enhances the anti-ambipolar response, giving a reduced valley current, a narrower on-state window, and a much higher peak-to-valley ratio while maintaining low-bias operation. The device also shows competitive performance compared with previously reported cryogenic anti-ambipolar technologies. These results highlight the vertical nanowire platform as a strong candidate for compact anti-ambipolar electronics at cryogenic temperatures.

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