An Interface-Modulated Antiferroelectric-to-Ferroelectric Transition Strategy in Doped HfO_2 Achieving Record High Permittivity for Energy Efficient Memories

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***Abstract*— We report a comprehensive demonstration of a novel atomistic interface-engineering strategy for inducing the antiferroelectric-to-ferroelectric phase transition in Si-doped HfO_2, achieving a morphotropic phase boundary (MPB) that yields a record-high relative permittivity (67 at 298 K and 77 at 403 K). By engineering interfaces with ultrathin Al_2O_3 and TiO_2 layers in a multilayer stack, we stabilize the MPB, enabling low-voltage operation suitable for DDR5 technology and future neuromorphic applications. The devices exhibit fast switching (5 microseconds at 1.1 V), excellent endurance (exceeding 10 to the 8^{th} cycles with no visible fatigue), minimal frequency dispersion, and robust lifetime under stress. Structural and electrical characterizations confirm the interface traps modulation, outperforming state-of-the-art hafnia-based films in κ and low-voltage switching. This scalable approach overcomes the limitations of conventional bulk dielectric doping, enabling a broader optimization trade-off space and offering a viable pathway for integrating other doped HfO_2 antiferroelectrics into 3D FeRAM and AI-accelerator memory hierarchies.**

Keywords—High-κ Dielectrics, Interface Engineering, Energy Efficient Memories, Antiferroelectric-to-Ferroelectric Transition

I. Introduction

Scaling dynamic random access memory (DRAM) capacitors for advanced technology nodes, particularly under low-voltage DDR5 operation, requires dielectric materials that combine high permittivity, low leakage, and strong reliability [1]. HfO_2-based dielectrics have emerged as leading candidates to replace conventional high-κ materials due to their CMOS compatibility and excellent scalability [2]. However, simultaneously achieving a high dielectric constant (κ) and fast switching at reduced operating voltages remains challenging, as these properties are typically antagonistic within bulk-doped films [3], [4].

One promising route to enhance dielectric response is the formation of a morphotropic phase boundary (MPB) between the antiferroelectric (AFE) and ferroelectric (FE) in fluorite-structured hafnia. In this regime, phase coexistence can synergistically boost permittivity. MPB formation has been realized through composition tuning [5], pressure engineering [6] , and electric-field cycling [7], yielding films with low equivalent oxide thickness (EOT) and dielectric constants exceeding 60 [8], [9]. However, strategies based solely on bulk doping [10], thickness scaling, and crystallization temperature optimization often suffer from limited phase stability, poor interfacial defect control, and switching speeds incompatible with DDR5 supply voltages.

Interfacial engineering like the one proposed in this work provides an alternative and potentially more effective pathway. Ultrathin interlayers such as Al_2O_3 and TiO_2, deposited by atomic layer deposition (ALD), offer precise

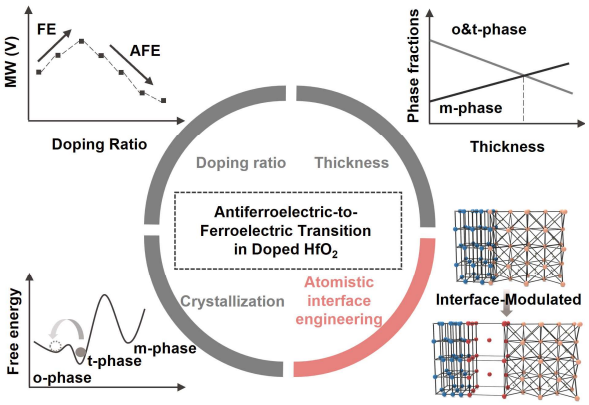

Fig. 1. Schematic illustration of the Antiferroelectric-to-Ferroelectric (AFE-to-FE) transition in doped HfO_2 thin films. The central diagram highlights the four key modulation factors: doping ratio, film thickness, crystallization process, and our atomistic interface engineering.

thickness control, excellent conformality, and the ability to tailor interfacial charge states (**Fig. 1**). Despite this potential, a systematic, atomistically-informed framework that exploits interlayers to drive an AFE-to-FE phase transition and stabilize an MPB in HfO_2 dielectrics has not been reported.

Here, we introduce an interface-modulated atomistic engineering strategy in which ultrathin TiO_2 and Al_2O_3 interlayers are precisely integrated into a Si-doped HfO_2 gate stack via an ALD process. By engineering the interfacial trap density and internal electric field profile, we induce a controllable AFE-to-FE phase transition and stabilize an MPB, achieving a record relative permittivity of $\kappa = 67$ at 298 K and $\kappa = 77$ at 403 K in a 10 nm film, accompanied by ultrafast switching of 5 µs at the DDR5 supply voltage and endurance exceeding 10^8 cycles without measurable fatigue. Comprehensive structural, electrical, and reliability characterizations unambiguously attribute these property enhancements to interfacial modifications alone, with the bulk crystallographic phase remaining unperturbed. This *scalable, interface-centric strategy* resolves the fundamental trade-offs inherent to bulk doping and establishes a viable pathway toward incorporating doped high-κ HfO_2 dielectrics into 3D FeRAM and AI-accelerator memory hierarchies.

II. Results and Discussion

Table I compares three capacitor stack architectures (Caps. A, B, and C) and their key properties, highlighting the interfacial layers. Cap. A represents an AFE dominant structure incorporating a TiO_2 bottom interlayer. Cap. B is derived from Cap. A by selectively removing the top TiN electrode through wet etching, which introduces interfacial defects. Cap. C adopts an engineered MPB configuration that integrates both TiO_2 and an ultrathin Al_2O_3 interlayer.

TABLE I. COMPARISON OF 3 STACKS AND KEY PROPERTIES

	Cap. A	Cap. B	Cap. C
Stack	MIFM	MIFM	MIFIM
Bottom IL	TiO_2 1.5 nm		
AFE	Si doped HfO_2 (Si:Hf = 1:36) 7.5 nm		
Top IL	×	×	Al_2O_3 1nm
A supplementary processing step	×	Top TiN etching	Top TiN etching & Top IL deposition
κ (at 0 V at 298 K)	58	27	**67**
Switching time (at 1.1 V)	200 μs	1 ms	5 μs

IL:interlayer

TABLE I. Comparison of capacitor stacks and key electrical properties, highlighting our record high-κ (67) value at 10 nm films, with ultra-fast switching speed (5 μs at 1.1 V)

Specifically, a 1 nm Al_2O_3 layer is deposited via ALD to modulate interfacial trap states (**Fig. 2**). This interface optimization yields a superior relative permittivity (κ = 67) and an ultrafast switching time of 5 μs, representing an improvement over recent reports. Our all-ALD, atomistically precise interface engineering strategy reshapes the trap landscape to induce an antiferroelectric-to-ferroelectric phase transition, exceeding the performance limits of bulk-doped high-κ dielectrics in a process compatible with high-volume manufacturing. The electrical sample evolution is presented in **Fig. 3**. Cap. A resembles a typical AFE system, characterized by pinched P–E loops and dual-peak κ–V curves. In contrast, Cap. B displays a transition to stabilized FE ordering with open hysteresis and single-peak capacitance profiles. Notably, Cap. C demonstrates intermediate electrical signatures characteristic of an MPB state, resulting in a maximized κ value near 0 bias. To quantitatively analyze switching dynamics, first-order reversal curve (FORC) measurements were conducted (**Fig. 3(c)**). With the applied field sweep, the P–E curve and switching current density corresponding to each reversal field E_r can be attained. The switching density $\rho^-(E_r, E)$ was then calculated using the following equation:

$$\rho^-(E_r, E) = \frac{1}{2} * \frac{\partial^2 P_{FORC}^-(E_r, E)}{\partial E_r \partial E} \qquad (1)$$

The resulting FORC distribution maps reveal distinct switching nuclei and electric field distributions among the three capacitor stacks. Cap. C exhibits broadened and asymmetric FORC features, indicating the coexistence of AFE and FE domains.

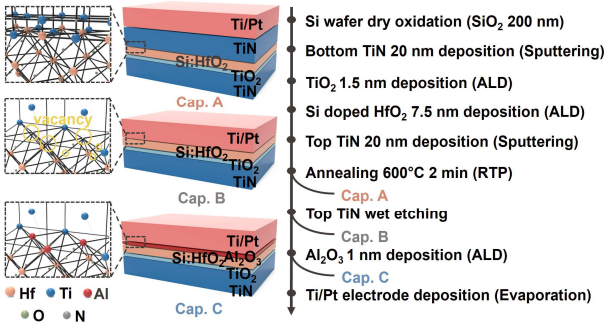

Fig. 2. Schematic illustration of the stacks for Cap. A, B, and C, highlighting the integration of TiO_2 and Al_2O_3 interfacial layers. The atomistic models depict the elemental arrangement and vacancy distribution within the functional layers.

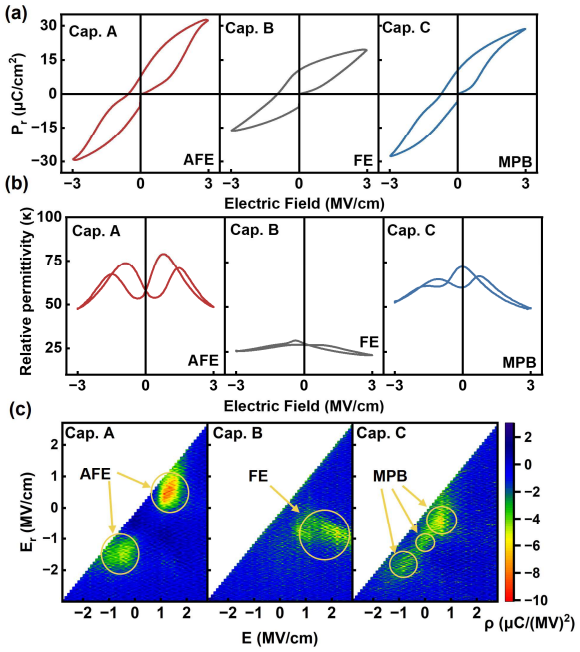

Fig. 3. (a) Polarization-Electric field (P-E) hysteresis loops and (b) Relative Permittivity-Voltage (κ-V) curves for Cap. A (AFE), Cap. B (FE), and Cap. C (MPB). The double-peak feature in the κ-V curve of Cap. A and the pinched loop in P-E confirm the AFE behavior, while the transition to a single peak and open loop in Cap. B/C illustrates the phase modulation from FE to MPB states. (c) FORC distribution maps for Cap. A, B, and C, which aligns with the structural and band-gap modulations.

This behavior correlates with interface-induced internal electric fields, as further supported by energy band simulations. Grazing-incidence X-ray diffraction (**Fig. 4(a)**) confirms that the bulk crystallographic structure of the AFE film remains unchanged from Cap. A to Cap. C, indicating that the observed electrical property variations originate from interfacial modifications. Subjecting the bilayer dielectric to high-bias stress induces extreme electric fields (on the order of MV/cm) within the ultra-thin layers (**Fig. 4(d)**), leading to the following phenomena: (1) non-negligible leakage currents, wherein the Al_2O_3 layer functions as an equivalent resistance (**Fig. 4(c)**); (2) charge injection into the interface-adjacent layer driven by the field due to the uncompensated

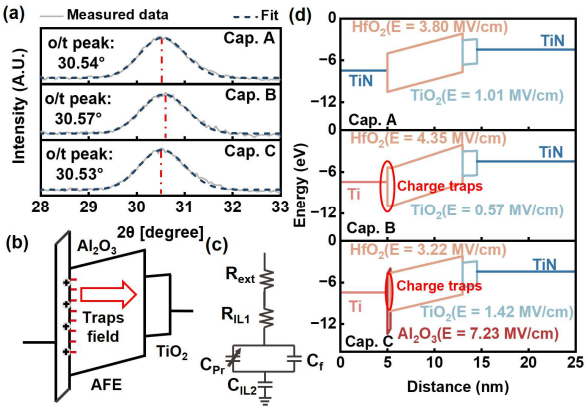

Fig. 4. (a) Grazing incidence X-ray diffraction (GIXRD) patterns of Cap. A, B, and C. (b) Schematic illustration of the trap-induced internal field within the stack. (c) Equivalent circuit model. (d) Simulated energy band diagrams for Cap. A, B, and C under bias. Red ellipses highlight the localized charge traps at the interfaces, which significantly influence the potential distribution.

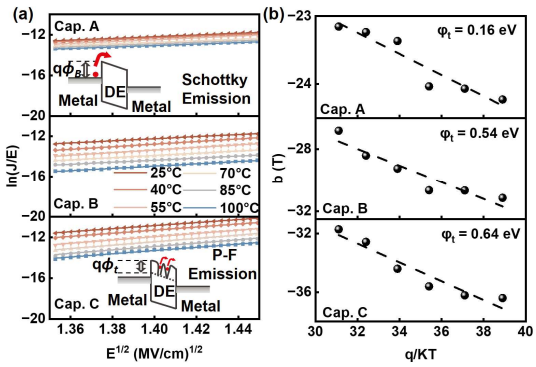

Fig. 5. (a) Experimental plots of ln(J/E) versus $E^{1/2}$ for samples across a temperature range from 298 K to 373 K. Insets show the schematic energy band diagrams for emission. (b) Extraction of ϕ_t by plotting the intercept b(T) as a function of q/kT, which extracted trap barrier heights for 3 stacks.

polarization; and (3) the retention of trapped charges, which persist until a sufficient counter-voltage is applied. The built-in field originating from these trapped charges breaks the symmetry of the antiferroelectric switching (**Fig. 4(b)**), attenuates the characteristic 'pinched' hysteresis at 0 bias, and effectively emulates a ferroelectric-like state.

Conduction mechanisms across all samples are well described by the Poole–Frenkel (PF) emission model [11], as shown in **Fig. 5(a–b)**. The relationship between current density and electric field can be expressed as:

$$log\left(\frac{J}{E}\right) = \frac{q}{2.3kT}\sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_r}} - \frac{q\phi_t}{2.3kT} + logC \qquad (2)$$

where J is the current density, E is the electric field, T is the temperature, ϕ_t is the trap barrier height, q is the elementary charge, k is the Boltzmann constant, and C is a pre-exponential constant.

From this model, the trap depth can be extracted, which serves as a direct indicator of the defect density within the dielectric layer. The extracted trap energies are approximately 0.64 eV below the conduction band for Cap. C and 0.54 eV for Cap. B, consistent with oxygen-vacancy related trap states. In contrast, Cap. A exhibits trap energies more consistent with defect levels associated with interstitial hydrogen, explaining the observed changes in electrical behavior following wet etching.

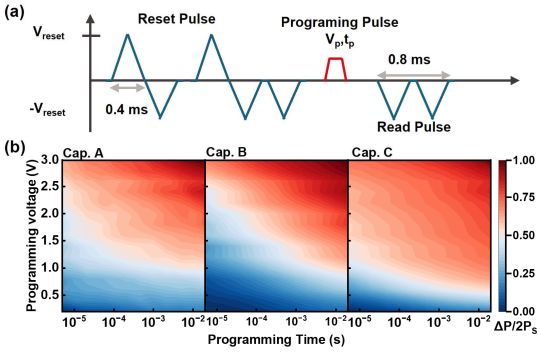

Fig. 6. (a) Pulse measurement sequence consisting of reset, programming, and read pulses. (b) Normalized switched polarization heatmaps as a function of programming voltage and time.

Fig. 6(a) shows the applied pulse sequence, which includes reset, program, and read operations. The characteristic switching time τ is extracted in accordance with the nucleation-limited switching model. The characteristic switching time $\tau(E_a, E)$ can be expressed as:

$$\tau(E_a, E) = \tau_\infty exp\left\{\left(\frac{E_a}{E}\right)^\alpha\right\} \qquad (3)$$

where E denotes the local electric field, E_a represents the activation field, α is the power-law exponent, τ is the characteristic switching time, and τ_∞ is the pre-exponential factor. The applicability of this model is consistent with the heterogeneous nucleation behavior expected at MPB compositions. **Fig. 6(b)** presents two-dimensional heatmaps of the normalized switched polarization $\Delta P/2P_S$ for Cap. A, Cap. B, and Cap. C as functions of programming voltage (0.2 to 3.0 V) and programming time (5 µs to 10 ms). MPB Cap. C achieves complete polarization reversal at voltages as low as 1.1 V with switching times as short as 5 µs. These results directly confirm the compatibility of the interface-modulated MPB design with DDR5 supply-voltage constraints and demonstrate its potential for high-speed, low-power embedded memory applications.

Further structural and electrical insights into MPB Cap. C were obtained through atomistic-level interface engineering. Cross-sectional TEM imaging of the heterostructure **(Fig. 7)** reveals abrupt, diffusion-free interfaces throughout the stack, demonstrating precise layer-by-layer growth control. Elemental EDS mapping corroborates the well-defined vertical compositional profile: the Hf and Si signals confirm that the Si-doped HfO_2 layer is spatially confined to the center of the stack; the Al signal delineates an ultrathin Al_2O_3 interlayer immediately above the HfO_2; and the Ti signal is consistently detected at both the top Ti adhesion layer and the bottom TiN electrode, affirming the structural integrity of the full device stack.

Fig. 8(a) presents the temperature dependence of the relative permittivity, κ, measured over the range of 298–453 K, which reaches a peak value of 77.28 at 403 K — surpassing the theoretical upper limit attainable by bulk doping strategies alone. **Fig. 8(b)** displays the frequency dispersion of κ and the dielectric loss tangent (tan δ) across the 10–100 kHz range. The permittivity exhibits minimal frequency dependence, remaining nearly constant between 60 and 70, while tan δ stays below 0.14 throughout the entire measurement window.

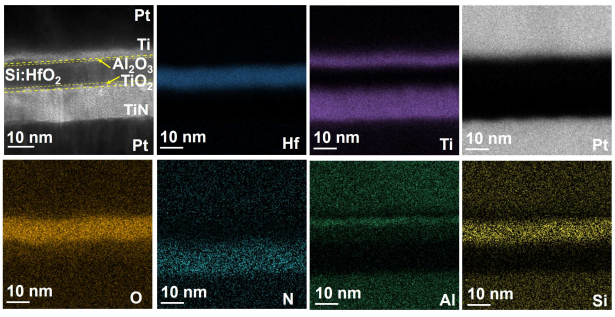

Fig. 7. Cross-sectional transmission electron microscopy (TEM) image and corresponding energy-dispersive X-ray spectroscopy (EDS) mapping of the Pt/Ti/Al_2O_3/Si:HfO_2/TiO_2/TiN/Pt structure. The localized distribution of Hf, Ti, O, N, Al, and Si confirms the well-defined interfaces and successful integration of the multilayer dielectric stack.

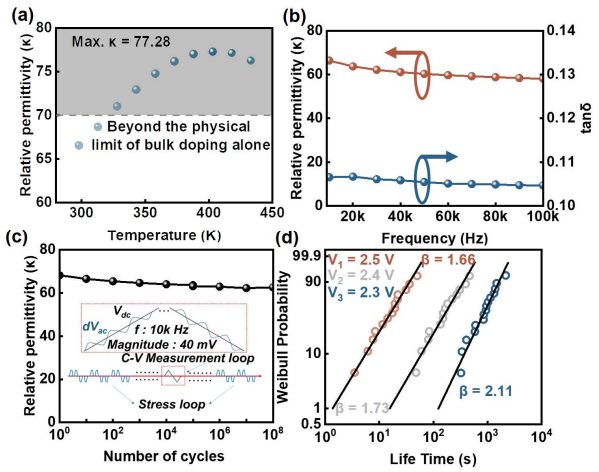

Fig. 8. (a) Temperature dependence of the relative permittivity, reaching a value of 67 at 298 K and maximum value of 77 at 403 K. (b) Frequency dispersion of the relative permittivity and dissipation factor from 10 kHz to 100 kHz. (c) Endurance characteristics of the relative permittivity over 10^8 switching cycles. (d) Devices lifetime under different voltage stress.

The absence of appreciable frequency dispersion indicates that the interface-modulated dielectric stack introduces no additional lossy polarization relaxation mechanisms. **Fig. 8(c)** demonstrates the endurance performance over up to 10^8 bipolar switching cycles, confirming that the atomistic interface engineering strategy does not induce structural fatigue under prolonged electrical stress. **Fig. 8(d)** presents the time-dependent dielectric breakdown characteristics analyzed via Weibull statistics under constant voltage stress. Extrapolation of the failure distributions to the nominal DDR5 operating voltage predicts an operational lifetime exceeding 10 years, thereby validating the long-term reliability of the proposed device architecture under realistic use conditions.

The key metrics presented in **TABLE II** are all experimentally extracted, including thickness, DDR5-V_{DD} switching time, relative permittivity (κ), endurance, and leakage current density. For quantitative benchmarking, Table II compares our results with representative state-of-the-art studies, demonstrating that our material engineering achieves one of the best trade-offs among these performance metrics.

TABLE II. COMPARISON WITH STATE OF THE ART

Material	Thi. (nm)	τ_{sw} (at 1.1 V)	κ	End.	J (A/cm^2)	Ref.
Al:HfO_2	9.2	-	68	1×10^{10}	2×10^{-5}	(1)
HZO	10.0	300 µs	-	$<10^8$	-	(2)
HZO	6.0	500 µs	48	$<10^8$	-	(3)
HZO	6.5	-	47	-	1×10^{-6}	(4)
HZO	6.0	-	48	10^6	$<1\times10^{-7}$	(5)
HZO	5.0	80 ns	-	-	-	(6)
HZO	10.0	100 µs	-	-	-	(7)
HZO	6.0	-	49	10^{11}	$<1\times10^{-7}$	(8)
HZO	4.6	-	66	10^8	7×10^{-5}	(9)
Si:HfO_2	**10.0**	**5 µs**	**67**	**$>10^8$**	**3×10^{-6}**	**This work**

Thi.: Thickness End.: Endurance

III. CONCLUSION

This work reports an in-depth engineering investigation of atomistic interface-modulated AFE-to-FE transition in Si-doped HfO_2 thin films, enabling an MPB that yields a record-high κ of 67 at 298 K and 77 at 403 K with superior switching kinetics and EOTs of 0.58 nm and 0.51 nm, respectively. Beyond Si- or Zr-doping, the proposed atomistic interface engineering strategy can be generalized across all AFE HfO_2 implementations to achieve an MPB, bypassing current state-of-the art bulk-doping limitations to advance the development of future high-κ-based FE and AFE for energy-efficient memories.

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