A -107.3dB THD+N Feedback-After-LC Capacitively Coupled Chopper Class-D Audio Amplifier with 126dB Dynamic Range

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***Abstract*—This paper presents a feedback-after-LC capacitively-coupled chopper analog-input Class-D audio amplifier (CDA) that achieves high dynamic range and high linearity by employing a novel filtered CIFF-B loop structure. Fabricated in a 0.18 µm BCD CMOS process, the prototype achieves a dynamic range (DR) of 126 dB and a peak total harmonic distortion plus noise (THD+N) of -107.3 dB. The CDA delivers >7.8W into an 8 Ω load under a 12V supply, while achieving a peak efficiency of 88%.**

Keywords—Class-D audio amplifier, high dynamic range, THD+N, capacitively-coupled chopper CDA, filtered CIFF-B

I. INTRODUCTION

Class-D amplifiers (CDAs) are widely employed in audio applications thanks to their high power efficiency compared to the Class-AB counterparts. For very high-performance audio systems, an ultra-high dynamic range (DR) approaching 130 dB is desired to match the dynamic range of human ears, while low THD+N is required to ensure high sound fidelity. Conventional CDAs implemented with resistive feedback networks, as shown in Fig. 1 (a), introduce an inherent trade-off between thermal noise and input impedance, limiting the DR often below ~115dB [1-5]. To break this fundamental trade-off, capacitively-coupled chopper CDAs have been proposed, as shown in Fig.1(b), which can significantly increase the input impedance without noise penalty, thereby enabling high DR (121.4dB) [6]. Additionally, a feedback-after-LC topology is adopted to compensate for the nonlinearity introduced by the LC filter, thereby achieving high overall system linearity with small inductor bulk. However, its DR is still limited by a trade-off between noise and linearity performance as discussed below.

Fig. 2 shows a simplified feedback-after-LC capacitively-coupled chopper CDA proposed in a prior work [6], which consists of an overall capacitive feedback network to define the audio signal amplification. Inside the loop, an inner capacitively-coupled chopper amplifier (CCCA) with a gain defined by C_{IN}/C_{GAIN} is employed to suppress the noise from the following loop filter stages. To achieve high loop gain, which is required to obtain high linearity, multiple loop filter stages are employed, and an additional feedback path from the switching node is introduced to form an inner loop (last stage), which, together with the LC filter, results in an overall phase shift of approximately 90° at the LC cutoff frequency and therefore is simplified and modeled as an integrator. Lastly, a cascade-of-integrators-with-feedback (CIFB) architecture is adopted for stability. Ideally, the noise of the entire CDA should be dominated by that of the CCCA. However, to achieve ultra-low noise, the noise of the following integrator can become a limiting factor due to the

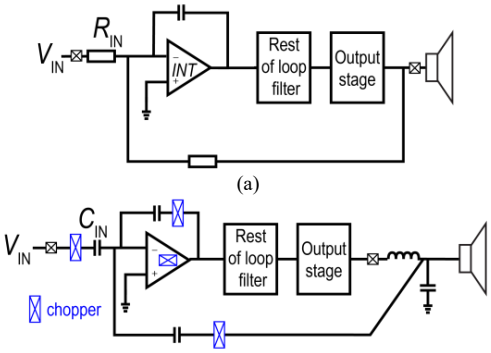


Fig. 1. (a) Resistive feedback CDA. (b) Capacitively-coupled chopper CDA

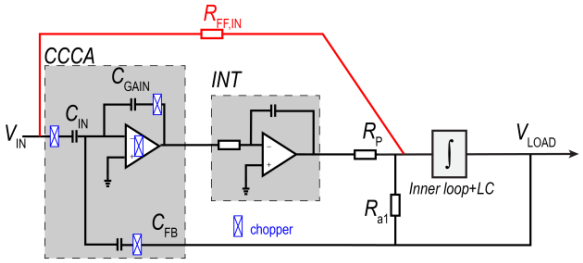


Fig. 2. A simplified capacitively-coupled chopper CDA[6]

following two reasons: 1. To obtain loop stability, the required 1st integrator time constant could require a relatively large integrator resistor in the range of tens to hundreds of kΩ, given a certain chip area constraint often limited by the integrator capacitor size (typically ~100 pF). 2. The inner CCCA closed-loop gain is limited by its output linear swing under a full-scale (FS) input signal, limiting noise suppression in the following stage. To mitigate this issue without significantly increasing chip area and/or degrading linearity, a common approach is to introduce a feedforward path from the input, as shown in Fig. 2 ($R_{FF,IN}$) [6], thereby increasing the CCCA closed-loop gain without saturating its output and further suppressing integrator noise. Nevertheless, doing so would load the input with an additional resistor, degrading the input impedance. Moreover, when a digital-input implementation is adopted [7-8], in which the input capacitors can be converted into a CDAC, this additional feedforward path would require an additional digital-to-analog converter (DAC), thereby increasing system complexity.

To mitigate the aforementioned issues, this work proposes a novel filtered CIFF-B loop filter structure that maximizes CCCA gain while avoiding additional input loading and degrading system performance.

II. PROPOSED CLASS-D AUDIO AMPLIFIER

A. Proposed Loop Filter Architecture

As shown in Fig. 2, the fast feedback path a_1 (R_{a1}) (necessary for stability) introduces a signal component of $a_1 \cdot V_{LOAD}$ at the summing node at the input of the inner loop. To fully cancel this component, the direct input feedforward factor $a_{FF,IN}$ ($R_{FF,IN}$) must satisfy the equation below

$$a_{FF,IN} = \frac{a_1 \cdot V_{LOAD}}{V_{IN}} = \frac{a_1}{a_{FB}} \quad (1)$$

To eliminate direct source loading, the first intuitive solution would be to move the feedforward path to the output of the CCCA, known as the CIFF structure, as shown in Fig. 3 (a). Since the signal component at the CCCA output is amplified by a factor G relative to the input, the required feedforward factor at the CCCA output becomes

$$a_{FF,CCCA} = \frac{a_{FF,IN}}{G} = \frac{a_1}{a_{FB} \cdot G} \quad (2)$$

However, this $a_{FF,CCCA}$ path is no longer a purely feedforward path and modifies the loop transfer function. Specifically, it introduces an equivalent feedback term of $-a_{FB} \cdot G \cdot a_{FF,CCCA}$. To maintain the same loop transfer function would inevitably remove the fast feedback path a_1, which imposes stringent requirements on the CCCA, as it must simultaneously achieve high accuracy and fast settling up to the entire loop filter bandwidth f_u (~500kHz). To mitigate this issue while preserving the advantages of the CIFF-B structure, the feedforward path $a_{FF,CCCA}$ is split into two paths in different frequency domains, as illustrated in Fig. 3(b): a new low-pass-filtered feedforward path $H_{FF,CCCA}(s)$ and a high-pass-filtered feedback path, $H_{a1}(s)$. The transfer functions of the two paths ($H_{FF,CCCA}$, H_{a1}) are given by Eqs. 3 and 4, respectively. To ensure an unaltered loop transfer function, the same corner frequency should be used for both paths, which can be realized accurately by passive components and will be discussed in detail in Section D.

$$H_{FF,CCCA}(s) = \frac{a_{FF,CCCA}}{1 + s/\omega_{LPF}} \quad (3)$$

$$H_{a1}(s) = a_1 \frac{s/\omega_{HPF}}{1 + s/\omega_{HPF}} \quad (4)$$

Fig. 4 shows the simulated CDA phase margin as a function of the CCCA bandwidth. With a ~500kHz f_u, the system phase margin of CIFF structure would degrade rapidly as the CCCA bandwidth decreases. To maintain sufficient phase margin, the CCCA bandwidth must be at least 20× higher than the loop's unity-gain frequency, which consumes significant power. In contrast, the proposed filtered CIFF-B structure can achieve the same phase margin with a much lower CCCA bandwidth; therefore, it greatly relaxes the speed requirement of the CCCA.

B. Overall CDA Architecture

The overall architecture of the proposed CDA is shown in Fig. 5. It consists of an inner CCCA operating in a 1.8V domain, a 12 V three-level pulse width modulation(PWM)-based output stage with a switching frequency fSW = 4.92 MHz, and a capacitive-coupled chopper feedback taken after the LC filter [6-7]. The CCCA operates at a chopping frequency of fchop=447kHz, with a 17 ns deadband implemented to suppress chopping-induced transients. Same as [6], a resonator stage is built around amplifier A_1 and A_2 to improve the loop gain approaching 20kHz, and a lead

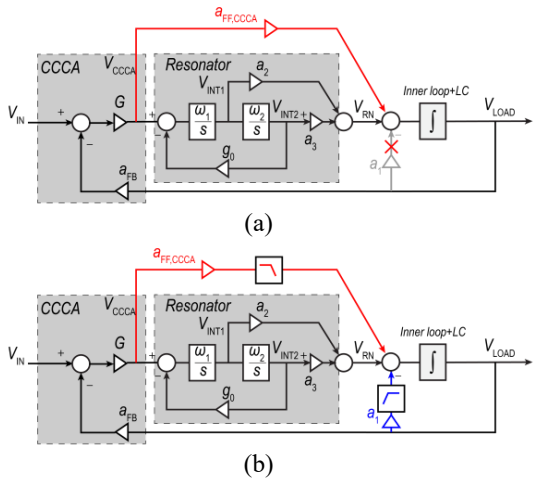


Fig. 3. (a) CIFF (b) Proposed filtered CIFF-B

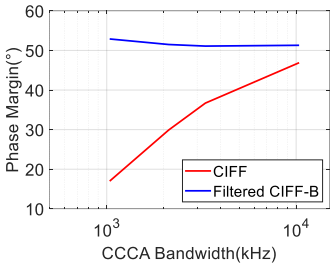


Fig. 4. Phase Margin versus CCCA bandwidth

compensator stage is built around the output stage and A_3 to form an inner loop to stabilize the feedback-after-LC loop. Both the low-pass feedforward path ($R_{FF,CCCA1}$, $R_{FF,CCCA2}$, $C_{FF,CCCA}$) and the high-pass feedback path (R_{a1} C_{a1}) are fully realized using passive components, eliminating the need for additional amplifiers and thereby improving power efficiency with great design simplicity.

C. Noise

To achieve a DR >125dB with a 1.8V supply at the input, an input-referred noise of <0.7μV_{rms} must be obtained. To suppress the 1st integrator's noise where R_{INT1}=40kΩ, the CCCA's gain (C_{IN}/C_{GAIN}) is designed to be 32 to reduce the integrator noise to ~0.16 μV_{rms}. Compared to the case without the proposed filtered CIFF-B loop filter, the achievable CCCA gain would be limited to ~8 for the same CCCA output swing, which would then require a 10kΩ R_{INT1} for the same noise performance. This would result in a 4x increase in C_{INT1} to 340 pF (680 pF for a differential implementation), thus a significant area overhead. It should be noted that the low-pass feedforward path contributes negligible noise even with $R_{FF,CCCA1}$ =144kΩ. This is because the audio-band noise of R_{INT1} is amplified by the high-gain resonator path, making the noise of $R_{FF,CCCA1}$ negligible at the summing node at the input of A_3.

D. Design of filtered CIFF-B corner frequency

The selection of the corner frequency of the forward and feedback paths plays a critical role in balancing signal swing and system performance. As shown in Fig. 3(b), within the audio band, the feedforward path $H_{FF,CCCA}$ carries little signal components since the high-gain resonator path dominates in this frequency range. However, the high-pass feedback path H_{a1} could still introduce a residual signal

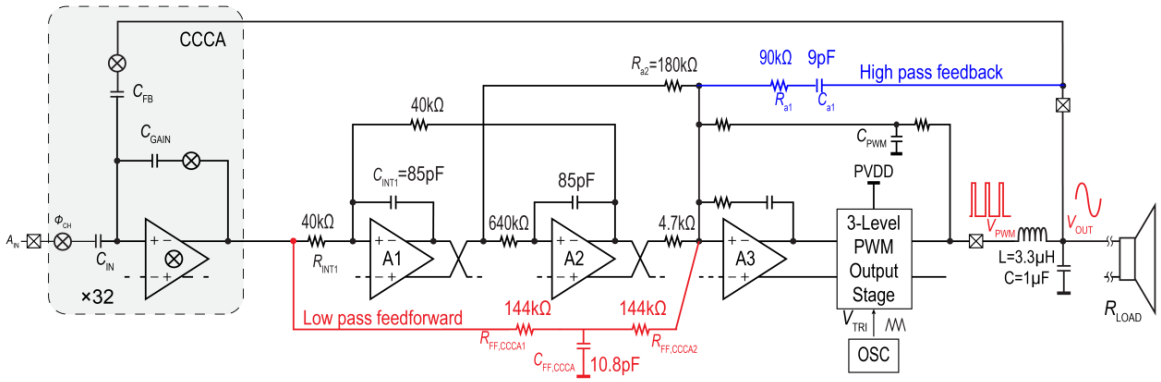


Fig. 5. Proposed analog input class-d audio amplifier

component of $V_{LOAD}\cdot H_{a1}$, especially when the corner frequency is close to the audio band. To cancel this component, the resonator output V_{RN} must generate an equivalent signal. The required signal component reaches its maximum at the highest audio frequency (20 kHz). At this frequency, V_{INT1} is more dominant than V_{INT2}, and thus

$$V_{RN}@20kHz \approx V_{INT1}@20kHz\cdot a_2 \tag{5}$$

Accordingly, the signal component at the INT1 output at 20 kHz and the corresponding signal component at the CCCA output V_{CCCA} can be expressed as

$$V_{INT1}@20kHz = \frac{V_{LOAD}\cdot a_1}{a_2}\cdot\frac{s(20kHz)/\omega_{HPF}}{1+s(20kHz)/\omega_{HPF}} \tag{6}$$

$$V_{CCCA}@20kHz = \frac{V_{INT1}@20kHz}{\omega_l/s(20kHz)} \tag{7}$$

To effectively suppress the signal component at the CCCA output, the high-pass corner frequency ω_{HPF} must be sufficiently higher than the audio band (20kHz). Fig. 6 illustrates the signal swing at the outputs of INT1 and the CCCA under a $1V_{peak}$ input at 20 kHz. It is shown that a low corner frequency results in excessive signal swing at both the CCCA and INT1 outputs, leading to out-of-range operation. Conversely, if the corner frequency is too high, the CCCA must process a significant portion of the high-frequency signal, making the operation resemble that of a CIFF structure and increasing the speed requirement. Therefore, the corner frequency is chosen to be ten times higher than the maximum audio signal frequency (20 kHz), providing an optimal trade-off between signal attenuation and amplifier bandwidth.

Assuming that the CCCA provides an ideal gain G, the resonator is effectively bypassed by $H_{FF,CCCA}$ around f_u. As a result, the signal path from V_{LOAD} to the input of the inner loop can be expressed as follows:

$$\beta \approx H_{a1} + H_{FF,CCCA}\cdot G\cdot a_{FB} = a_1\cdot\beta_0 \tag{8}$$

$$\beta_0 = \frac{s/\omega_{HPF}}{1+s/\omega_{HPF}} + \frac{1}{1+s/\omega_{LPF}} \tag{9}$$

Fig. 7(a) shows the normalized feedback factor β_0, which should ideally be 0dB. If the low-pass corner frequency ω_{LPF} is 2x lower than ω_{HPF}, a phase dip appears around 100 kHz, which may lead to unintended zero crossings and negative gain margin. Conversely, if ω_{LPF} is 2x higher than ω_{HPF}, the additional phase lag degrades the phase margin. Fig. 7(b) shows the loop gain around LC filter. Selecting ω_{LPF} equals to ω_{HPF} provides an optimal trade-off and ensures stable operation.

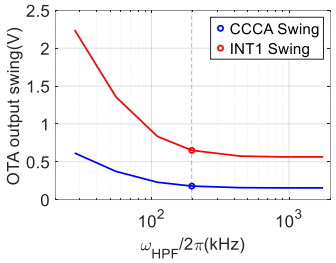


Fig. 6. INT1 and CCCA output signal swing at 1 Vpeak input, 20 kH

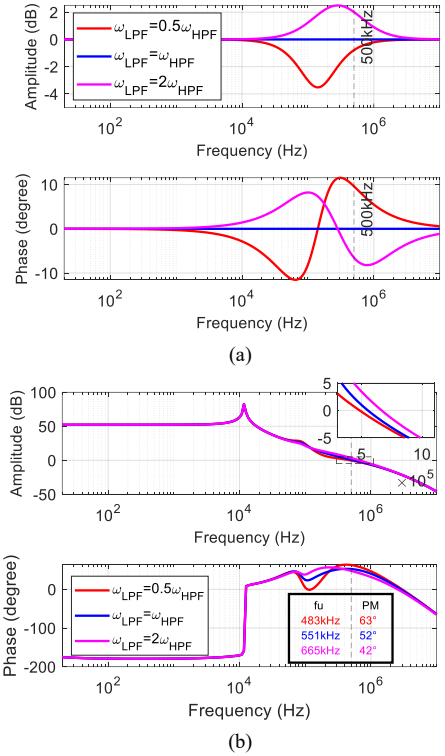


Fig. 7. (a) Normalized feedback factor β_0. (b) Loop gain around LC filter

In reality, component mismatch will result in a slight mismatch between the two paths. However, Monte Carlo simulations show a negligible impact (PM varies ~1°)

III. Measurement Results

The proposed CDA prototype is fabricated in a 0.18 µm BCD process, occupying a die area of 8.3 mm², shown in Fig. 8(a). Fig. 8(b) shows the measured power supply rejection ratio (PSRR) across the audio band, with an injected 2 Vpp supply ripple. The PSRR reaches 109 dB at 217 Hz and remains 78.6 dB at 20 kHz. Fig. 9(a) shows the output spectrum when the amplifier drives an 8 Ω load with a -6.7 dBFS, 6 kHz sinusoidal input, corresponding to an output power of 1.65 W. At this power level, a peak THD+N of -107.3 dB is measured. With a −80 dBFS input, the measured SNR is 46 dB, corresponding to a DR of 126 dB, as shown in Fig. 9 (b).

Fig. 10(a) presents the measured THD+N as a function of output power for a 1kHz and 6 kHz input, respectively. The CDA can maintain a THD+N <100dB up to 7.8W when driving an 8 Ω load. The maximum output power is simply limited by the supply and the load. The measured power efficiency versus output power, shown in Fig. 10(b), achieves a peak efficiency of 88%.

Table I summarizes the performance comparison with state-of-the-art analog-input CDAs. The proposed design achieves the highest DR and the lowest noise among reported monolithic audio CDAs while maintaining competitive performance regarding THD+N and PSRR.

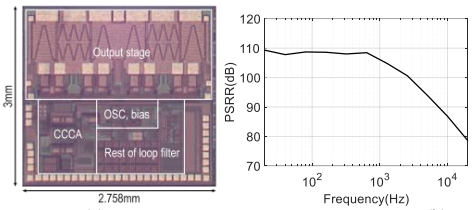
TABLE I. Comparison with State-Of-The-Arts

	This work	[6]	[5]	[3]	[4]
Process (nm)	180	180	-	180	130
Feedback Network	Cap	Cap	Res	Res	Res
Input loading	Cap	Cap+Res	Res	Res	Res
Supply (V)	12	14.4	4.5-18	14.4	2.5-10
$I_{Q,PVDD}$ (mA)	9.4	9	60	7.6	2.6
R_{LOAD} (Ω)	8	8	2-4	8	8
$P_{OUT,MAX}$ (W)	7.8[e]	11[bf]	21[bf]	14[f]	5.8[f]
Efficiency	88%	93%	88%	90%	93%
THD+N(dB) @1kHz	-102.4	-110	-78	-105	-101
THD+N(dB) @6kHz	-107.3	-113[b]	-57[b]	-106.3	-
DR (dB)	126	121.4	-	109[c]	112[c]
A-wt. Output Noise (μV_{RMS})	4.83	8.0	42	28.2[a]	17.1[a]
PSRR (dB) (20~20kHz)	109-79	89-71	80	86~68	118[d]

[a] Calculate from DR and Pout,max
[b] Extracted from figure
[c] Peak SNR
[d] Measured with 217Hz
[e] 0.001% THD+N
[f] 1% THD+N

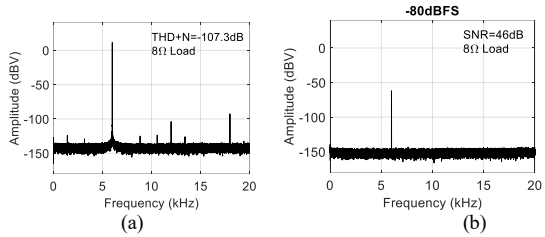
IV. Conclusion

This paper presents an analog-input Class-D audio amplifier that achieves a significant improvement in dynamic range (DR). The proposed filtered CIFF-B architecture enables a high-gain preamplifier without adding extra resistive input impedance, avoiding the limitations of conventional resistive feedforward approaches. Fabricated in a 180-nm process, the prototype achieves an A-weighted integrated noise of 4.83 µ V_{rms} and a DR of 126 dB, demonstrating the effectiveness of the proposed technique for high-performance audio applications.



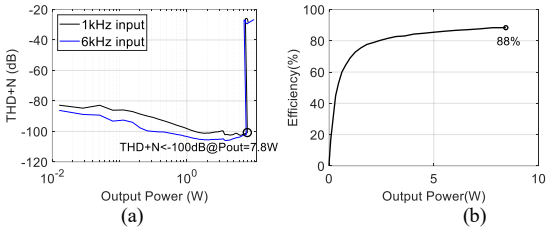
(a) (b)

Fig. 8. (a) Die micrograph; (b) PSRR versus frequency.



(a) (b)

Fig. 9. (a) Measurement output spectrum of minimum THD+N. (b) Measurement output spectrum at -80dBFS.



(a) (b)

Fig. 10. (a) THD+N over power; (b) Efficiency over power.

References

[1] Y. Z. Qiu, S. H. Chien, and T. H. Kuo, "A 0.4-mA quiescent-current, 0.00091% THD+N Class-D audio amplifier with low-complexity frequency equalization for PWM-residual-aliasing reduction," IEEE J. Solid-State Circuits, vol. 57, no. 2, pp. 423–433, Feb. 2022.

[2] K. Zhou, J. Zhou, Y. Tang, J. Li, Z. Hong, and J. Xu, "A 0.00055% THD+N Class-D audio amplifier with capacitive feedforward PWM and wide-band aliasing reduction," IEEE J. Solid-State Circuits, vol. 59, no. 12, pp. 4045–4056, Dec. 2024.

[3] H. Zhang, H. Fan, M. Zhang, M. Berkhout, and Q. Fan, "A −106.3 dB THD+N feedback-after-LC Class-D audio amplifier employing current feedback to enable 530 kHz LC-filter cutoff frequency," in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), Feb. 2024, vol. 67, pp. 382–384.

[4] I. Cho, M. Y. Choi, J. Byun, J. H. Lee, M. Lee, D. Kim, and J. Lee, "A 5.8 W, 0.00086% THD+N, 118 dB PSRR class-D audio amplifier with passive output common-mode compensation technique for wide output power range," in Proc. IEEE Symp. VLSI Technology and Circuits (VLSI Technology and Circuits), Jun. 2024, pp. 1–2.

[5] Texas Instruments. TPA6304-Q1 Automotive Class-D Audio Amplifier Datasheet. Accessed: Apr. 10, 2026. [Online]. Available: https://www.ti.com/lit/gpn/tpa6304-q1.

[6] H. Zhang, M. Berkhout, K. A. Makinwa, and Q. Fan, "A 121.4-dB DR capacitively coupled chopper Class-D audio amplifier," IEEE J. Solid-State Circuits, vol. 57, no. 12, pp. 3736–3745, Dec. 2022.

[7] H. Zhang, M. Berkhout, K. A. Makinwa, and Q. Fan, "A 120.9-dB DR digital-input capacitively coupled chopper Class-D audio amplifier," IEEE J. Solid-State Circuits, vol. 58, no. 12, pp. 3470–3480, Dec. 2023.

[8] J. W. Cyue and T. H. Kuo, "A low-EMI, high-DR Class-D audio amplifier with double-sided voltage-boosting modulation," IEEE J. Solid-State Circuits, 2025.