A 16.8-μW 3-Axis Digital Vibration Sensor Based on Source-Degenerated Dynamic Amplifier With Integration-Time-Based Gain Tuning

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***Abstract*—This article presents a 3-axis digital vibration sensor with a figure of merit (FoM) of 2.8 pJ. To address the noise–power tradeoff in battery-powered vibration monitoring applications, a fully dynamic discrete-time open-loop readout architecture based on a source-degenerated floating-inverter amplifier (SD-FIA) is proposed. The proposed interface circuits improve energy efficiency by implementing a boxcar-sampling-based dynamic amplifier with an intrinsic anti-aliasing filter. In addition, source degeneration resistors are implemented to extend the linear input range of the dynamic amplifier. To compensate for gain variations caused by process, voltage, temperature (PVT), and parasitic capacitances, an integration-time-based (T_{int}-based) gain-tuning technique is introduced using a reference capacitor. In addition, a C_{os} cancellation loop is incorporated to prevent saturation of the open-loop front end in the presence of offset capacitance. Fabricated in a 65-nm CMOS process, the prototype achieves an input-referred noise density of 139 $\mu g/\sqrt{Hz}$ over a 5 kHz bandwidth while consuming 16.8 μW from a 1.2 V supply.**

***Index Terms*—Vibration sensor interface, floating inverter amplifier, low power**

I. Introduction

Vibration sensors are increasingly used in Internet of Things (IoT) applications such as motion monitoring and acoustic measurement [1]–[3]. In these battery-powered applications, it is essential to balance the noise and power consumption of the sensor interface [4]. Prior works typically employ charge-sensitive amplifiers (CSAs) [1] or chopped continuous-time voltage (CTV) techniques [2] to suppress input-referred noise; however, these approaches incur static power consumption. In contrast, dynamic amplifiers (DAs) eliminate static power dissipation and scale dynamic power with the operating frequency [4]. DAs are often employed in a closed-loop configuration to enhance robustness against process, voltage, and temperature (PVT) variations. However, they require complete settling and inherently suffer from noise folding, resulting in a larger noise penalty [4]. At a given target bandwidth (5 kHz), the trade-off between noise and power consumption in interface circuits results in a figure of merit (FoM) exceeding 4.6 pJ in prior works [3]. To mitigate the sampling noise folding, this work proposes a fully-dynamic discrete-time, open-loop sensor interface based on a source-degenerated floating-inverter amplifier (SD-FIA), achieving an improved figure of merit (FoM) of 2.8 pJ. Furthermore, an integration-time-based (T_{int}-based) gain tuning technique is employed to enhance gain stability. Moreover, an offset capacitance (C_{os}) cancellation scheme is introduced to prevent saturation of the open-loop amplification.

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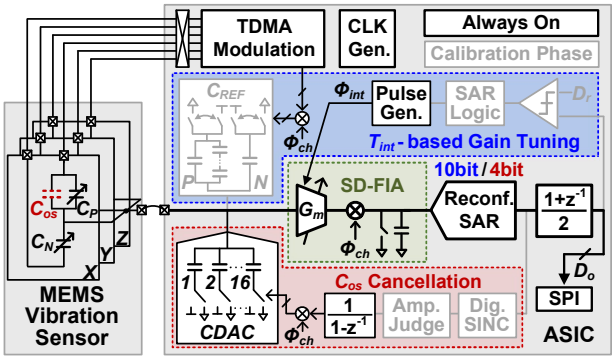

Fig. 1. The system architecture of the proposed vibration sensor.

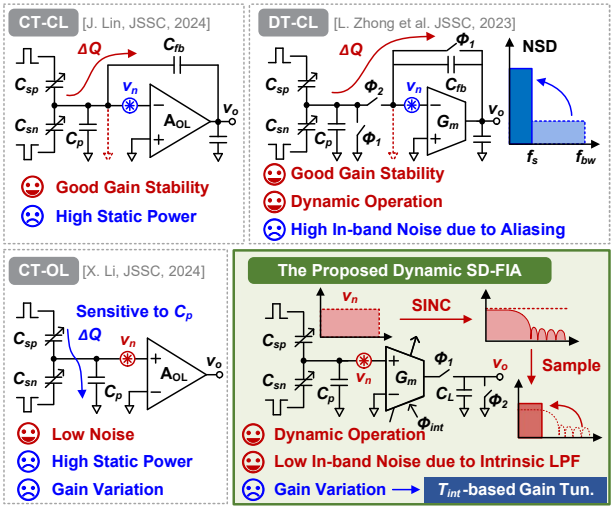

Fig. 2. Comparison of the proposed boxcar-sampling-based dynamic SD-FIA interface with existing MEMS capacitive sensor interfaces based on CT-CL, DT-CL and CT-OL architectures.

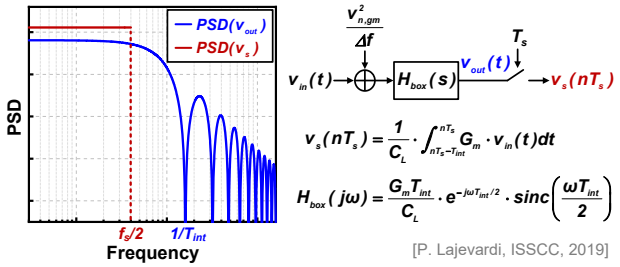

Fig. 3. The operation of the proposed OL dynamic amplifier is equivalent to boxcar sampling [5].

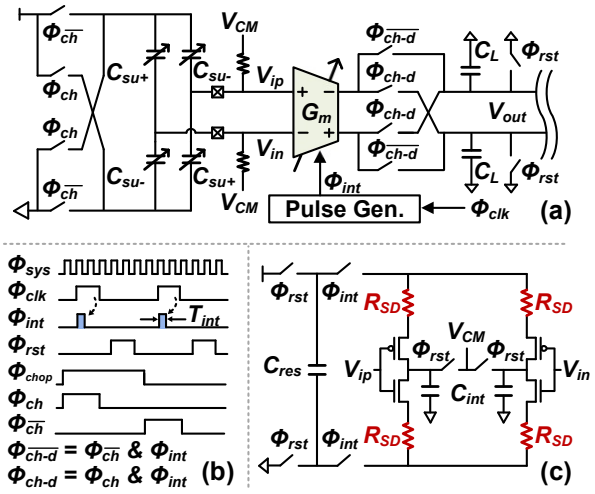

Fig. 4. (a) The architecture of the proposed sensor interface. (b) The system timing diagram. (c) The proposed dynamic SD-FIA.

II. Proposed Vibration Sensor Interface Circuits

The system architecture of the proposed vibration sensor is illustrated in Fig. 1. The outputs of the 3-axis MEMS vibration sensor are multiplexed into the readout circuit in a time-division-multiplexed manner. The multiplexed signal is amplified by an open-loop SD-FIA. A pulse generator is utilized to control the gain of the SD-FIA, which can be calibrated through a T_{int}-based gain tuning loop. The open-loop gain of the SD-FIA suppresses noise from subsequent stages, thereby relaxing the data-converter resolution requirements and facilitating the use of a reconfigurable oversampling SAR ADC. During full-speed operation, both the SD-FIA and the SAR ADC employ an oversampling ratio (OSR) of 8. The SAR ADC can be configured to 10 bits for high-resolution quantization. During the C_{os} cancellation phase, the resolution can be reconfigured to 4 bits for energy efficiency. To mitigate the effects of amplifier offset and flicker noise, a system-level chopping technique is adopted [6]. Notably, the SAR logic in the T_{int}-based gain tuning loop and the digital SINC filter and the amplitude judge module in C_{os} cancellation loop are only activated during the calibration phase, while the pulse generator and the capacitive digital-to-analog converter (CDAC) operate continuously.

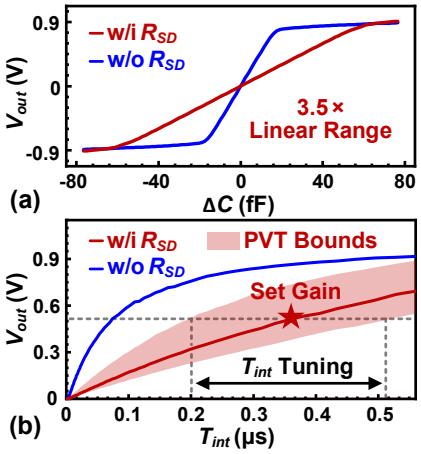

Fig. 5. Simulation results of the (a) linear range and (b) $V_{out} - T_{int}$ characteristics.

Fig. 2 reviews prior-art analog front ends (AFEs) for capacitive sensors and illustrates the proposed dynamic SD-FIA-based AFE. Prior-art interfaces based on the CSA topology operate in a continuous-time closed-loop (CT-CL) manner [1], [7]. The virtual short characteristic of the closed-loop structure prevents charge from transferring to parasitic capacitances, thereby enhancing gain stability. However, reducing gain error and suppressing input-referred noise generally require increased static power consumption. Configuring the circuits in a switched-capacitor topology and operating in a dynamic manner can enhance energy efficiency [4], [8]. However, the discrete-time and closed-loop (DT-CL) operation folds in the out-of-band noise, which in turn degrades overall performance. Operating the amplifier in an open-loop (OL) manner can improve noise performance [9], but the OL topology inherently suffers from poor gain stability and is more susceptible to saturation under large input capacitance C_{os} [2]. While the proposed SD-FIA dynamically operates in an OL manner, a T_{int}-based gain tuning technique is proposed to ensure its gain stability. In addition, the saturation problem is addressed by a C_{os} cancellation loop. To suppress the impact of out-of-band noise, this work adopts a DT-OL boxcar amplifier topology [10]. The signal is integrated over a fixed time window, sampled, and then reset. As shown in Fig. 3, the integration and sampling operations are equivalent to a SINC filter in the frequency domain, thereby forming an intrinsic anti-aliasing filter prior to the analog-to-digital conversion [5].

The schematic of the proposed SD-FIA and its timing diagram are shown in Fig. 4. Conventional FIA operates similarly to an inverter [11]. By introducing source degeneration resistors in the inverter pair, the linear range of the amplifier is extended by 3.5×, as shown in Fig. 5(a), thereby leading to linear OL amplification. Nevertheless, the OL amplification is susceptible to gain variations due to parasitic capacitance as well as PVT variations [2]. According to [5], [10], the SD-FIA gain exhibits a linear dependence on the integration time (T_{int}), as simulated in Fig. 5(b). Since the sensor is capacitive, calibration can be performed using a reference

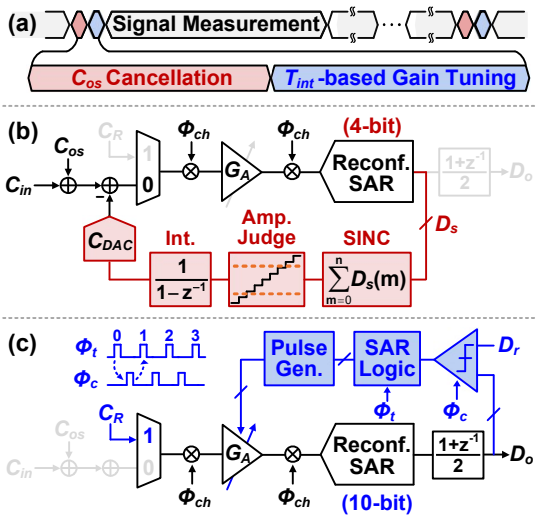

Fig. 6. (a) Timing diagram. (b) Proposed C_{os} cancellation loop. (c) Proposed T_{int}-based gain tuning loop.

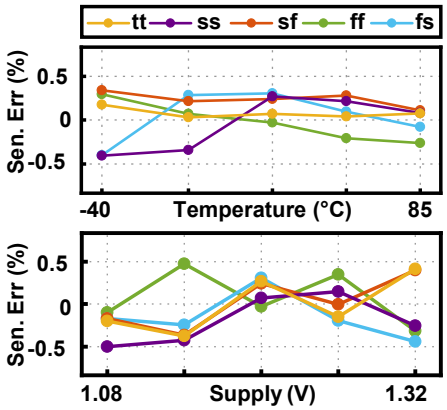

Fig. 7. The simulation results of the proposed T_{int}-based gain tuning.

capacitor, where metal-insulator-metal (MIM) capacitors are adopted due to their high temperature stability. Consequently, fine-tuning of the SD-FIA gain is achieved by introducing this reference capacitor along with a T_{int}-based gain tuning loop. A tunable T_{int} is generated by a pulse generator composed of a cascade of delay inverters, where the output pulse width is selected by digital control bits.

Fig. 6(a) shows the timing diagram of the proposed architecture. The operation of the circuit consists of three phases: signal measurement, C_{os} cancellation and T_{int}-based gain tuning. The latter two phases are performed after every 1024 signal measurement cycles. Fig. 6(b) introduces the proposed C_{os} cancellation technique. During the C_{os} cancellation phase, the 4-bit SAR ADC output is low-pass filtered, and then evaluated by an amplitude judge module to determine whether C_{os} cancellation has been completed. If not, the filtered signal is used to update the CDAC control code through an accumulator until convergence is achieved. After the loop settles, the output signal is regulated between the upper threshold (0.8×VDD) and lower threshold (0.2×VDD), effectively preventing circuit

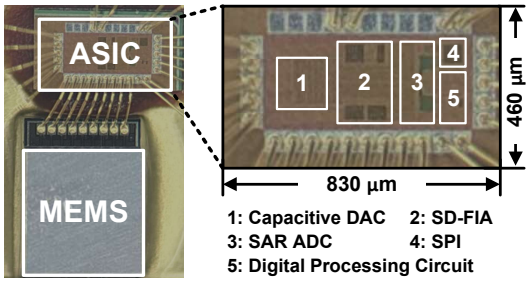

Fig. 8. Micrograph of the proposed interface IC bonded to MEMS.

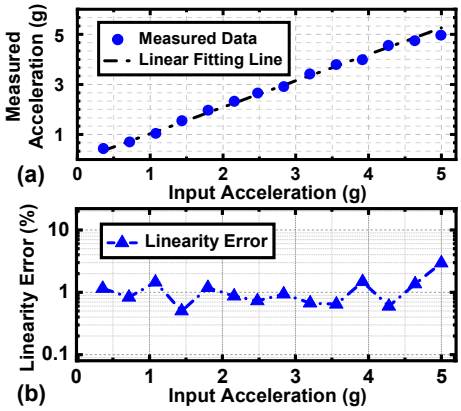

Fig. 9. (a) Measured output code response to DC acceleration and (b) linearity error.

saturation. The proposed T_{int}-based gain tuning technique is shown in Fig. 6(c). A reference capacitor (C_R) shares the same feedforward path with the main signal readout circuits. After C_R is sensed, the output code is compared with a predefined target code corresponding to an input capacitance equal to C_R. The comparison result is processed by the SAR logic to generate a control word that adjusts the pulse width of T_{int}. Simulation results in Fig. 7 demonstrate that the sensitivity error across PVT variations can be lowered to ±0.5% after gain tuning.

III. Measurement Results

Fabricated in 65-nm CMOS technology, the proposed vibration sensor interface occupies a chip area of 0.38 mm^2, as shown in Fig. 8. As shown in Fig. 9(a), the prototype chip supports a maximal input range of ±5 g, and the linearity error is less than 3%. Measurements from six chips are shown in Fig. 10. The temperature coefficient of sensitivity reaches ±0.07%/K (±3σ) before calibration, which is reduced to ±0.014%/K (±3σ) after T_{int}-based gain tuning. Fig. 11 shows the output spectrum under DC acceleration input. With the proposed SD-FIA, the sensor interface achieves a noise level of 139 $\mu g/\sqrt{Hz}$ at a bandwidth of 5 kHz. The absence of a SINC-shaped response is attributed to the effect of downsampling. Fig. 12 illustrates the total power and the power breakdown of the proposed sensor interface circuits. The power consumption scales linearly with operating frequency because of the fully dynamic architecture. In the

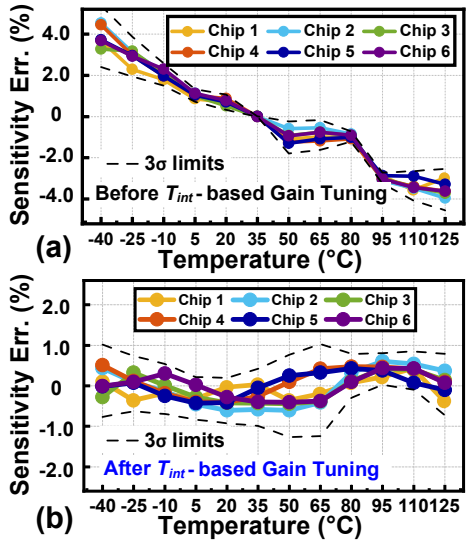

Fig. 10. Measured sensitivity error@1g input over temperature of six chips.

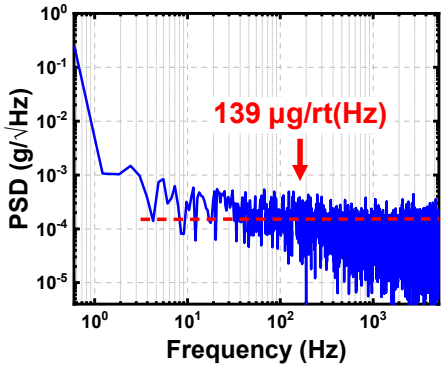

Fig. 11. Measured spectrum of D_o under DC acceleration input.

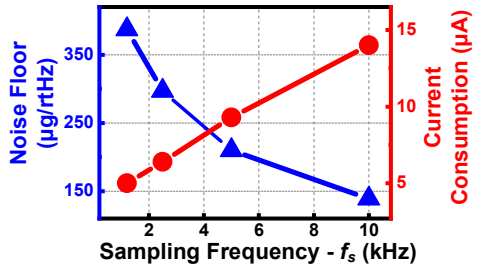

Fig. 12. Measurement results of noise floor and current consumption versus sampling frequency.

normal mode (BW = 5 kHz), the measured supply current is 14 μA at a supply of 1.2 V. TABLE I shows the performance summary and comparison [1]–[4], [12]. Compared with recently published vibration sensors, this work achieves the lowest power consumption in the table. The proposed dynamic SD-FIA realizes low-power and low-noise operation, while T_{int}-based gain tuning stabilizes the interface gain and the C_{os} cancellation loop prevents saturation. As a result, this work achieves a FoM of 2.8 pJ, which is 39% lower than that of prior works.

TABLE I : Performance Summary and Comparison

Parameter	This Work	JSSC 2023[4]	JSSC 2024[1]	JSSC 2024[2]	VLSI 2025[3]	ST-IIS3D WBG1[12]
Architecture	DT-OL	DT-CL	CT-CL	CT-OL	CT-CL	-
Technology	65nm	180nm	180nm	180nm	180nm	-
Output Format	Digital	Digital	Digital	Analog	Analog	Digital
Supply Voltage [V]	1.2	1.8	1.8	1.8	1.8	3
Number of Axis(N)	3	1	3	1	2	3
Full Scale (FS) [±g]	5	6	30	5000	10	16
Noise Density [µg/rtHz]	139	81	58	46.6	22	75
Bandwidth (BW) [Hz]	5000	10000	8000	5700	2000	6300
Current [µA]	14	120	550	65mA	83	1.1mA
Current per Axis [µA]	4.67	120	183	65mA	41.25	367
Figure-of-Merit (FoM)[1] [pJ]	2.8	36.5	7.3	18.1	4.6	81.4

[1] $\text{FoM} = \dfrac{\text{Supply Voltage} \times \text{Current per Axis}}{\text{Full scale}} \times \dfrac{\sqrt{\text{BW}}}{\text{Noise Density} \times \sqrt{\pi / 2}}$ [W. Cao, VLSI, 2025]

IV. Conclusion

In conclusion, this study employs a DT-OL boxcar sampling technique to suppress out-of-band noise folding during sampling. A dynamic amplifier with source degeneration is introduced to extend the linear range of the sensor. Furthermore, an integration-time-based gain calibration technique is proposed to enhance gain stability against PVT variations. In addition, a C_{os} cancellation loop is introduced to prevent saturation of the open-loop amplifier. The implemented vibration sensor achieves a noise density of 139 $\mu g/\sqrt{Hz}$ at a bandwidth of 5 kHz, while consuming 14 μA from a 1.2V supply.

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