A 1GS/s 13-bit Pipelined ADC with kT/C Noise-Cancelled Charge Sharing and Accurate Early Conversion

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***Abstract*—This paper presents a 13-bit 1GS/s SAR-assisted pipelined ADC that overcomes the residue-amplifier settling time bottleneck through two key techniques. The proposed kT/C noise-cancelled charge-sharing scheme enables parallel residue amplification with sampling and conversion while relaxing the trade-off among kT/C noise, attenuation, and hardware. The proposed accurate early-conversion scheme further overlaps amplification with the next-stage conversion, achieving early conversion without additional full-scale range calibration or redundancy. Fabricated in 28nm CMOS, the prototype achieves 61.76dB SNDR at Nyquist while consuming 10.24mW, resulting in a Schreier FoM of 168.6dB.**

***Keywords*—SAR-assisted pipelined ADC, residue amplifier, passive residue transfer, charge sharing, parallel quantization**

I. Introduction

Pipelined ADCs are widely adopted in high-speed medium-to-high-resolution applications. Their performance, however, is often limited by the settling requirement of the residue amplifier (RA), which is constrained by two bottlenecks: 1) the serial operation of sampling, conversion, and amplification within each stage, and 2) the inter-stage dependency between residue amplification and the next stage's conversion.

One method to relax these bottlenecks is to parallelize the RA with the same-stage and next-stage operations, but prior solutions incur trade-offs. For the first bottleneck, parallelization requires residue transfer, which introduces kT/C noise: charge sharing [1-2] introduces a kT/C noise determined by the residue-transfer capacitance. Increasing the capacitance reduces the noise but causes signal attenuation, leading to stricter gain and noise requirements for the RA. Ping-pong CDAC [3-4] avoids the signal attenuation by using two residue-transfer capacitor sets, but at the cost of extra hardware and mismatch. In addition, kT/C noise remains and still requires large transfer capacitances.

For the second bottleneck, overlapping the RA with next-stage conversion requires prediction of the RA output before fully settling, which introduces prediction error. The parallel-operation-based method [5] quantizes the non-amplified residue to predict the final RA output, but it requires additional calibration to match the quantization range with the RA full-scale range. The method based on correlated level shifting (CLS) [6] starts conversion after the first phase coarse amplification to accelerate conversion speed. However, due to the gain difference between the two phases, only the very MSB information is obtained, and additional redundancy is required to prevent residue overflow, which limits the speed improvement.

To overcome these trade-offs, this work proposes two key techniques: 1) a kT/C noise-cancelled charge-sharing scheme suppresses the kT/C noise during the residue transfer, relaxing the transfer capacitor constraint; and 2) an accurate early conversion method based on open-then-closed correlated level shifting (OCCLS) [7] uses the inherently PVT-robust small-error coarse amplification of OCCLS to enable accurate early conversion. Implemented in a 13-bit 1GS/s pipelined ADC, this design achieves 61.76dB SNDR and a FoM_S of 168.6dB.

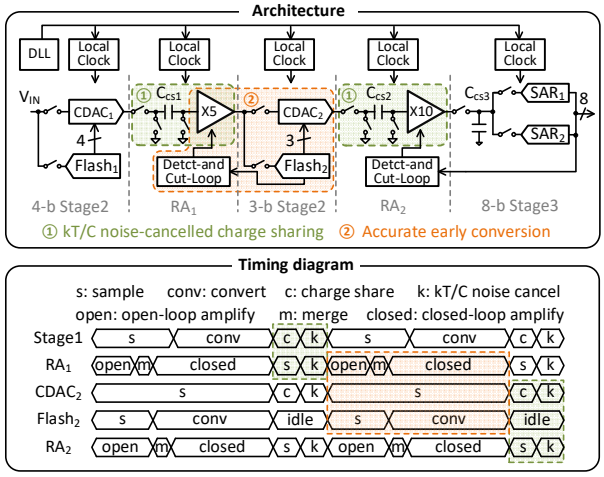


Fig. 1. Block and timing diagram of the proposed ADC.

II. ADC Architecture

Fig. 1 shows the implementation of the 13-bit 1GS/s ADC. It consists of three stages and two RAs, configured as 4b+3b+8b. The kT/C noise-cancelled charge sharing is used in RA_1 and RA_2, while the accurate early conversion is applied in the second stage. One-bit inter-stage redundancy is set between adjacent stages. The reference voltage of the second stage is halved. Combined with the signal attenuation introduced by charge sharing, the effective inter-stage gains are 8 and 4, respectively.

The input is first sampled and converted in the first stage. The residue is then transferred to RA_1 through ~200ps charge sharing with kT/C noise cancellation. RA_1 is allocated about 800ps for amplification using OCCLS. The amplification proceeds in three phases. RA_1 first performs open-loop amplification, followed by capacitor merging to bring the output close to its final value. After the merge phase and before the closed-loop phase, $Flash_2$ is disconnected from RA_1 to enable early conversion. RA_1 then enters the closed-loop phase with correlated level shifting to further reduce gain error. The open-loop phase duration is background-calibrated by the detect-and-cut loop, as in [7], to maintain a PVT-robust open-loop gain. RA_2 operates in a similar manner, with residue transfer, kT/C noise cancellation, and

OCCLS-based amplification. The third stage employs a 2x time-interleaved 8-bit SAR. With an overall gain of 32 from the preceding stages, the mismatch introduced by interleaving in the third stage is negligible.

By parallelizing residue amplification with both the same-stage and next-stage operations, the proposed architecture extends the amplification time to about 80% of the clock period. This relaxes the RA design and improves efficiency while maintaining PVT-robust inter-stage gain.

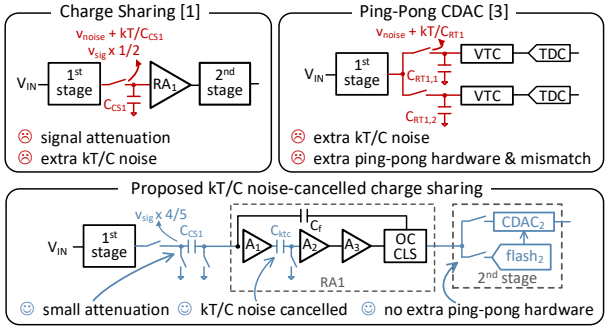
III. KT/C Noise-Cancelled Charge Sharing

Fig. 2 illustrates the proposed kT/C noise-cancelled charge sharing. Conventional approaches suffer from a trade-off among kT/C noise, signal attenuation, and hardware cost. The proposed method breaks this trade-off by introducing a noise-cancellation phase to suppress the kT/C noise, which accounts for about 14% ~ 20% of the total noise in the prior works [1-3]. As a result, a smaller charge-sharing capacitor (200fF) can be used, reducing signal attenuation without additional ping-pong hardware. The reduced attenuation, together with the inherent timing benefit of charge sharing, relaxes the RA requirements in three aspects: 1) longer settling time; 2) larger feedback factor for a given inter-stage gain; and 3) lower input-referred noise contribution from the RA.

The detailed operation is shown in Fig. 3, using RA_1 as an example. C_{S1} (800fF) is the first stage's CDAC. C_{CS1} (200fF) is the charge-sharing capacitor. C_F (40fF) is the feedback capacitor. The auto-zero capacitor of A_1 also serves as the noise-cancellation capacitor C_{ktc} (100fF), avoiding extra hardware. The operation proceeds in three phases as follows. 1) Residue transfer: After the first-stage conversion, C_{S1} and C_{CS1} are merged for passive residue transfer. When ϕ_{samp} falls, the residue V_{res} is sampled onto C_{CS1} with an attenuation of 0.8 (determined by the capacitor ratio), introducing kT/C noise V_{n1}. 2) kT/C noise sampling: When ϕ_{ktc} falls, the amplified noise $A_1 \cdot V_{n1}$ is sampled onto C_{ktc}. 3) Amplification: During ϕ_{amp}, the noise stored on C_{ktc} cancels V_{n1} on C_{CS1}, thereby cancelling the kT/C noise at the input of A_2.

Unlike conventional kT/C noise cancellation schemes [8-9], which need to handle a varying input and face a risk of amplifier saturation, the proposed scheme operates with a DC input. This avoids saturation and decouples gain and noise optimization from bandwidth constraints. An alternative switching mode overlaps ϕ_{samp} with ϕ_{ktc}, deliberately disabling noise cancellation. This mode is used for measurement purposes to enable direct on/off comparison.

For the third stage, due to the inter-stage gain of RA_1 and RA_2, the noise and inter-channel mismatch are suppressed, and the CDAC size is not limited by kT/C noise. Therefore, a ping-pong charge sharing scheme is adopted to extend the conversion time, as shown in Fig. 4. The RA_2 output is first sampled onto C_{CS3} and then transferred to the two interleaved SAR ADCs through 100ps charge sharing. Compared to directly sampling onto the SAR CDAC, this scheme allows the SAR conversion to proceed without waiting for RA_2 amplification. As a result, the conversion time is extended to about 1.8x the clock period. The only cost is signal attenuation, which is negligible in the last stage. This



Technique	Extra kT/C noise	attenuation	C_{CS} or C_{RT}	Hardware cost
Charge sharing [1]	kT/C_{CS1} ☹	x0.5 ☹	512fF ☹	C_{CS1} ☺
Ping-pong CDAC [3]	kT/C_{RT1} ☹	x1 ☺	750fF ☹	Double 2nd stage ☹
Proposed	Cancelled ☺	X0.8 ☺	200fF ☺	C_{CS1} ☺

Fig. 2. Comparison of the conventional charge sharing, ping-pong CDAC, and the proposed kT/C noise-cancelled charge sharing.

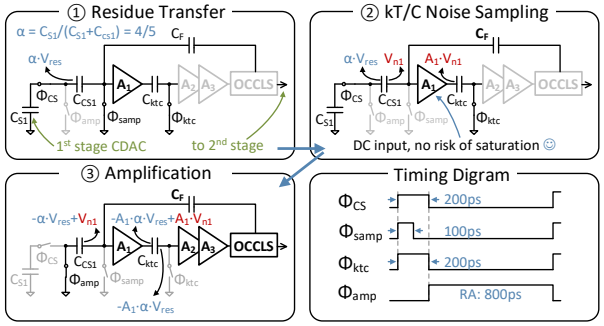


Fig. 3. Circuit and timing diagrams of the proposed kT/C noise-cancelled charge-sharing scheme.

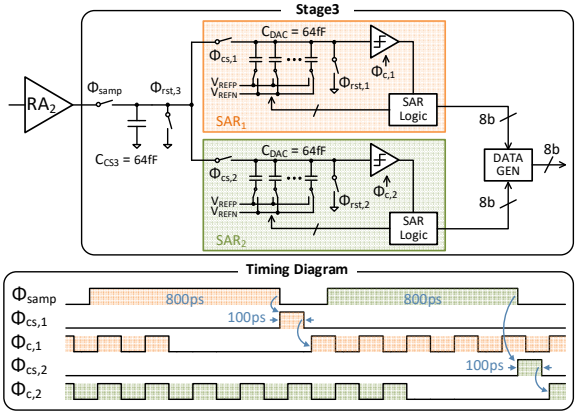


Fig. 4. Circuit and timing diagrams of the third-stage ping-pong charge-sharing scheme.

approach relaxes the conversion speed requirement and simplifies the third stage's clock generation.

IV. Accurate Early Conversion

To parallelize the RA with the next-stage conversion, an accurate early-conversion scheme is proposed based on the three-phase OCCLS. The key idea is to perform conversion after the open-loop and merge phase, before full settling. OCCLS enables this by ensuring a small gain error after the merge phase through its built-in self-tuning loop, which only consists of a comparator, a charge pump, and a voltage-

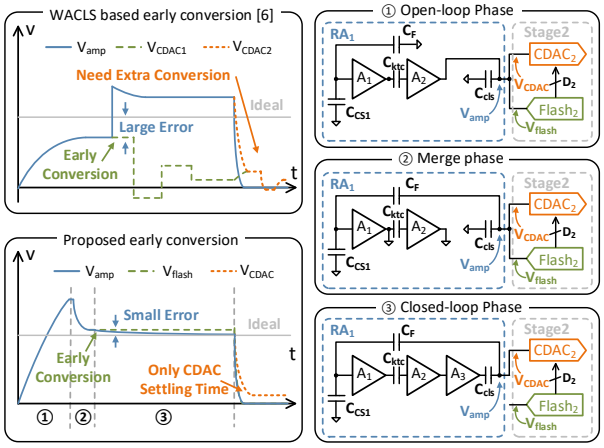


Fig. 5. Waveform and circuit schematic of the proposed accurate early conversion.

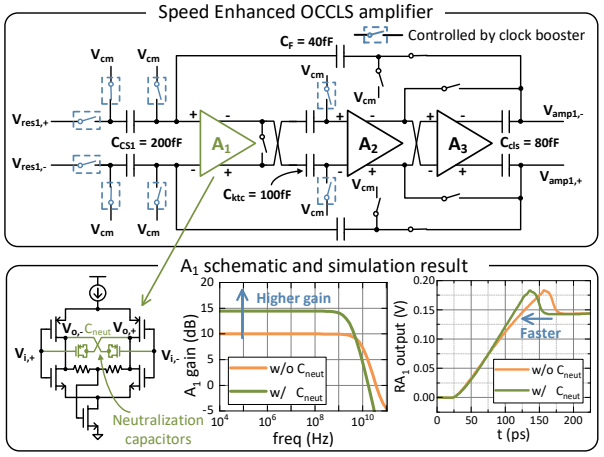


Fig. 6. Circuit implementation of the speed-enhanced OCCLS amplifier (closed-loop phase) and simulation results.

controlled delay line. As a result, the early-conversion accuracy requirement is satisfied without additional full-scale range calibration or redundancy.

The operation, shown in Fig. 5, consists of three phases. 1) In the open-loop phase, $Flash_2$ and $CDAC_2$ sample the RA_1 output. 2) In the merge phase, charge redistribution among C_{cls}, $CDAC_2$, $Flash_2$, and C_F brings the output close to its final value, after which $Flash_2$ is disconnected to start conversion. 3) In the closed-loop phase, RA_1 performs correlated level shifting to further reduce gain error while $Flash_2$ completes the conversion. $CDAC_2$ then switches directly after the closed-loop phase.

To fit OCCLS operation within the 800ps amplification window, two techniques are used to accelerate the open-loop amplification and the switching between phases, as shown in Fig. 6. First, a neutralization capacitor C_{neut} is introduced to partially cancel the feedback introduced by C_{gd}. Without C_{neut}, the feedback reduces the effective gain of A_1 and limits its contribution during the later part of the open-loop phase, leaving the slower A_2 to dominate the later amplification. With C_{neut}, the feedback is reduced, allowing A_1 to maintain a higher effective gain and continue contributing to the amplification throughout the open-loop phase, which shortens the open-loop phase. Precise matching of C_{neut} is not required, as even partial compensation can also improve the

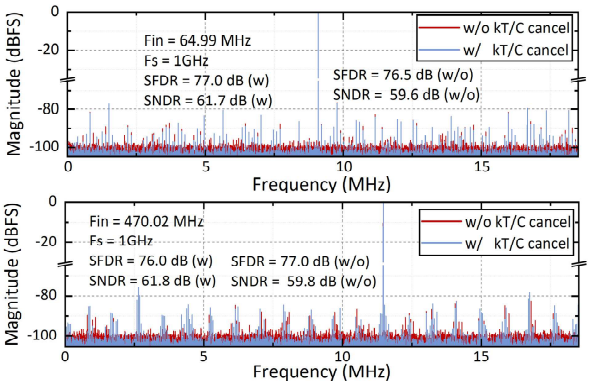


Fig. 7. Measured output spectrum with low frequency and Nyquist inputs (65,536-point FFT, 27x decimated).

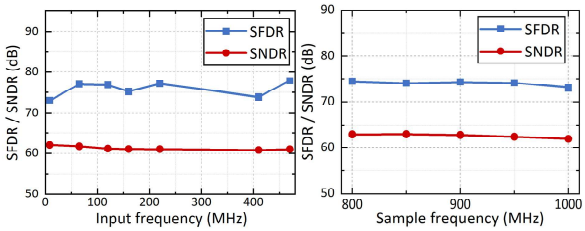


Fig. 8. Measured SFDR/SNDR vs. input frequency and sampling frequency.

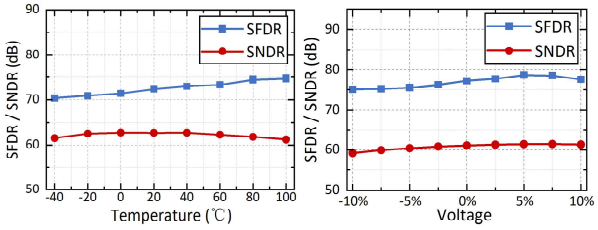


Fig. 9. Measured SFDR/SNDR vs. temperature and supply voltage.

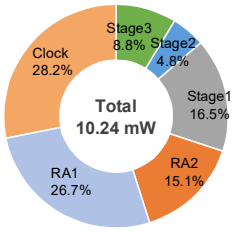


Fig. 10. Power breakdown.

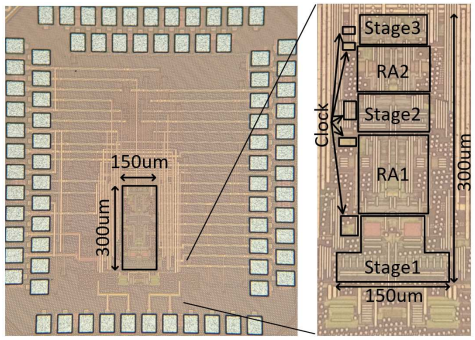


Fig. 11. Die Photo.

open-loop speed. Second, a clock booster [10] is used to reduce the on-resistance and parasitic capacitance of critical switches, further improving speed.

V. Measurement Results

The flash offset is calibrated via on-chip DAC, while CDAC mismatch and inter-stage gain errors are digitally corrected. All calibrations are performed once in the foreground and remain fixed during measurement.

Fig. 7 shows the output spectrum for low-frequency and Nyquist inputs, with the kT/C noise cancellation enabled and disabled. It demonstrates an SNDR improvement of about 2dB. Fig. 8 plots the measured SFDR and SNDR versus input frequency and sampling rate. Fig. 9 shows the SNDR variation is within 1.5dB over temperature and within 2dB under a ±10% supply variation.

Fabricated in a 28-nm process, the ADC occupies 0.045mm^2 and consumes 10.24mW. The power breakdown and a die photo are shown in Fig. 10 and Fig. 11. Table I compares this work with prior ADCs employing passive residue transfer. Despite using a small residue-transfer capacitor of 200fF, this work achieves 61.76dB SNDR and 168.6dB FoM$_S$, representing higher power efficiency. The proposed technique enables faster CLS operation, achieving 5x speed enhancement compared to conventional CLS (Fig. 12), while maintaining PVT robust inter-stage gain at 1GS/s.

VI. Conclusion

This paper presents a 13-bit 1GS/s pipelined ADC with extended amplification time through parallel residue amplification and next-stage conversion. A kT/C noise-cancelled charge-sharing technique is proposed to relax the residue transfer capacitor constraint and reduce signal attenuation. An accurate early-conversion scheme based on OCCLS enables early conversion before RA full settling without additional full-scale range calibration or redundancy. Implemented in a 28-nm process, the ADC achieves 61.76dB SNDR and a FoM$_S$ of 168.6dB. These results demonstrate the effectiveness of the proposed techniques for improving the efficiency of high-speed pipelined ADCs.

Acknowledgment

This work was supported by the National Natural Science Foundation of China (No. 62474004).

TABLE I. Comparison with the ADC Using Passive Residue Transfer

	This work		JSSC 25 Y. Shen [1]	ISSCC 17 H. Huang [2]	CICC 25 X. Zhao [3]	VLSI 14 C. Lin [4]
Architecture	**Pipe SAR**		Pipe SAR	Pipe SAR	TD Pipe	Pipe SAR
Process [nm]	**28**		28	65	28	65
Supply [V]	**0.9**		0.9/1.0	1.3	1.0	1.0
Resolution	**13**		12	12	13	12
fs [GS/s]	**1**		1.5	0.33	2	0.21
Passive residue transfer type	**kT/C noise-cancelled charge sharing**		Charge sharing	Charge sharing	Ping-pong CDAC	Ping-pong CDAC
Input swing [V_{pp}]	**1.4**		1.5	2.4	0.9	1.6
Signal attenuation	**0.8**		0.5	0.77	1	1
Sample cap size [fF]	**800**		512	1000	2000	2000
Residue transfer cap (C_{RT}) size [fF]	**200**		512	300	750	500
kT/C noise cancellation	**yes**	no	no	no	no	no
KT/C noise from residue transfer [nV^2] *		64.7	64.7	46.6	11.0	16.6
SFDR @ Nyq. [dB]	**76.8**	77	74.5	75.8	70.7	74.8
SNDR @ Nyq. [dB]	**61.76**	59.8	58.5	63.5	62.8	60.1
Residue transfer kT/C noise contribution [%]		26.4	16.3	14.5	20.7	5.3
Power [mW]	**10.24**	10.24	21.3	6.23	32.2	5.3
FoM$_W$ [fJ/conv.-step]	**10.2**	12.8	20.7	15.4	14.3	30.5
FOM$_S$ [dB]	**168.6**	166.7	164.0	167.7	167.7	163.1

*: calculated as $2kT/C_{RT}/(A_{attenuation})^2$

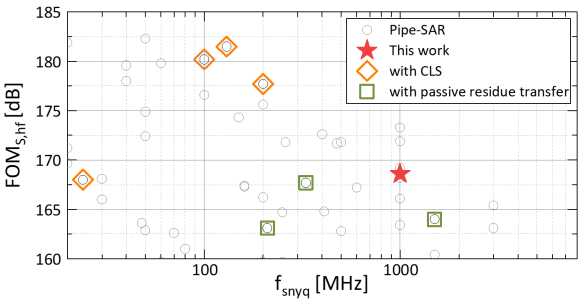


Fig. 12. Comparison of FoM$_S$ between this work and other SAR-assisted pipelined ADCs.

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