A 36-43 GHz Ultra-Compact and Low-Loss 150-ps Bandpass True-Time Delay Circuit with Reduced Loss Variations and Parasitics Absorption

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***Abstract*— This work proposes a bandpass passive true-time delay (TTD) architecture, which can be designed with a minimum resolution corresponding to a half-wavelength delay at the target center frequency of operation. Unlike conventional broadband passive TTDs that exhibit trade-offs between area efficiency, insertion loss (IL), and cut-off frequency, the proposed TTD circuit can be optimized at the target center frequency of operation, simultaneously achieving high area efficiency, low IL, and reduced loss variations across the delay states. To demonstrate the effectiveness of the proposed TTD architecture, a 150-ps 36-43-GHz prototype was fabricated in a 22-nm CMOS SOI process. To the best of the authors' knowledge, the prototype achieves the highest reported area efficiency for a passive CMOS TTD, while simultaneously achieving a 3× reduction in IL and loss variation per total delay compared to the state-of-the-art TTD designs above 30 GHz.**

***Keywords*— CMOS, hybrid array, mm-Wave, passive, phase shifter, phased array, Q-band, SATCOM, true-time delay.**

I. Introduction

To enhance wireless data rates and communication range, wideband and large-scale beamforming arrays have gained increasing interest in many applications, including satellite communication (SATCOM), and 5G and 6G communication. Although the phased array technology, based on phase shifters (PSs), is the mainstream solution for beamforming due to its high scalability, it becomes highly susceptible to the beam-squinting issue when the instantaneous bandwidth and array aperture size increase, requiring TTD units to maintain the array gain. To achieve scalability with such TTDs on the array level, TTD designs should satisfy a list of requirements including: (1) compact size, (2) sufficient delay range and resolution for the target application and array size, (3) accurate delay control with minimum variations across the target band, (4) low power consumption for active TTDs and low loss for passive implementations, and (5) reduced magnitude variations across the delay states to simplify array calibrations.

Trombone-based TTDs with switching amplifiers have been reported in [1], [2]. Although the switching amplifiers compensate for the delay line IL and can be appropriately sized to reduce the magnitude variations across the delay states, the required number of switching amplifiers increases linearly with the number of the delay states, resulting in prohibitively bulky and power hungry TTDs. Even though the area efficiency of the trombone-based TTD is improved to ∼350 ps/mm^2 in [3] with the use of origami inductors, the TTD's cut-off frequency is limited to 9 GHz due to the limited self-resonance frequency of such inductors. On the other hand, several purely passive TTDs have been reported in [4], [5], [6], [7] with broadband operation up to cut-off frequencies exceeding 20 GHz. Nevertheless, they experience large IL and magnitude variations near the cut-off frequency, and their area efficiency is limited to ∼200 ps/mm^2. By adopting coupled-inductor techniques in artificial transmission lines (TLs) and all-pass networks, the area efficiency of the passive TTDs in [8], [9], [10] is enhanced to above 300 ps/mm^2, yet at the cost of reduced cut-off frequencies below 20 GHz. This highlights the trade-off between area efficiency, IL, and cut-off frequency of prior-art TTDs.

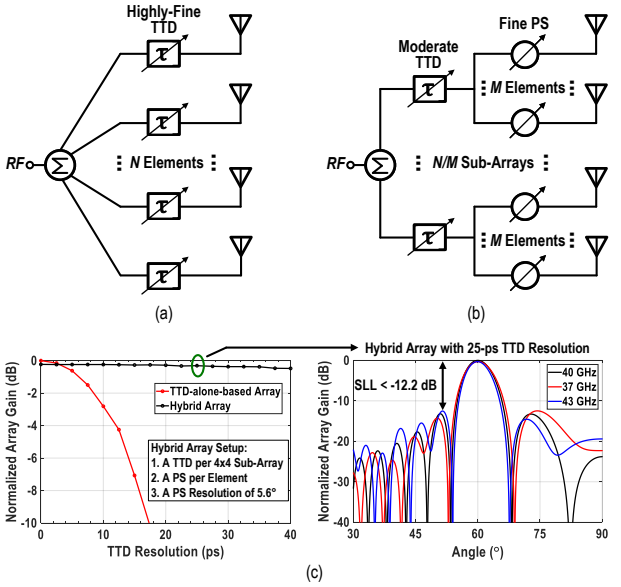

Fig. 1. Beamforming arrays with beam-squinting mitigation: (a) conventional TTD-alone-based arrays (b) emerging hybrid arrays with both TTD and PS beamforming (c) simulation results of 37-43-GHz 32×32 TTD-alone-based and hybrid arrays pointing at 60° for different values of TTD resolution.

Unlike conventional TTD-alone-based arrays, shown in Fig. 1(a), which require a highly-fine TTD unit per element, hybrid arrays that combine both PSs and TTDs, shown in Fig. 1(b), are emerging for wideband large-scale arrays [2], [3]. In such hybrid arrays, the implementation complexity can be reduced compared to TTD-alone-based arrays as: (1) each TTD unit can be shared among multiple elements since a per-element PS complements the TTD operation, saving significant area and power consumption, and (2) the TTD resolution requirement is relaxed as long as the PS resolution is

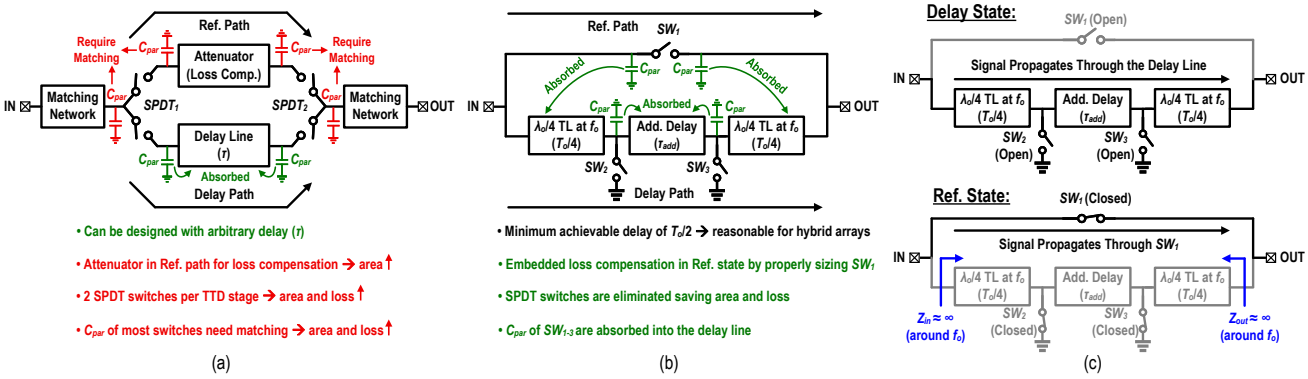

Fig. 2. Proposed passive TTD circuit in comparison to conventional passive TTDs: (a) conventional TTD stage with two SPDTs and an attenuator in the reference path (b) proposed SPDT-less TTD stage with embedded loss compensation and parasitics absorption (c) operation states of the proposed TTD stage.

fine enough (i.e., 5-6 bits). As demonstrated by the simulation results in Fig. 1(c) of 37-43-GHz 32×32 TTD-alone-based and hybrid arrays pointing at 60° for different values of TTD resolution, the TTD resolution of hybrid arrays can be readily relaxed to 25 ps (corresponding to one wavelength at 40 GHz), with a minor degradation of 0.31 dB in the array gain and while maintaining an excellent non-tapered sidelobe level (SLL) of -12.2 dB. However, even with hybrid arrays, simultaneously achieving high area efficiency, low IL, and reasonable cut-off frequency remains a crucial requirement in TTD design.

In order to address the aforementioned demand of hybrid arrays, while also addressing the limitations of the prior-art TTD designs, this work proposes a bandpass passive TTD architecture that can be designed with a minimum resolution corresponding to a half-wavelength delay at the target center frequency of operation, while simultaneously achieving high area efficiency, low IL, highly precise steps, and low magnitude variations across the delay states.

II. Proposed Passive TTD with Implementation

A. Conventional Passive TTDs

Fig. 2(a) shows the implementation of conventional switchable passive TTDs [8], [10]. Each delay stage consists of a delay path that employs a delay line, and another reference path designed with an attenuator to match the IL of the delay path. Although the delay line can be designed with an arbitrary delay value (τ), this architecture suffers from the following limitations: (1) the attenuator in the reference path adds area overhead, (2) each stage requires two SPDT switches, increasing the area and IL, and (3) most of the switches' parasitics cannot be absorbed into the delay line, requiring matching networks that also add to the area and IL.

B. Proposed Bandpass, SPDT-Less Passive TTD

In order to address the limitations of prior-art passive TTDs, this work proposes the passive TTD architecture shown in Fig. 2(b). In this architecture, the delay line is divided into three sections: two $\lambda_o/4$ sections interfacing with the input and output ports of the TTD stage, where λ_o is the wavelength

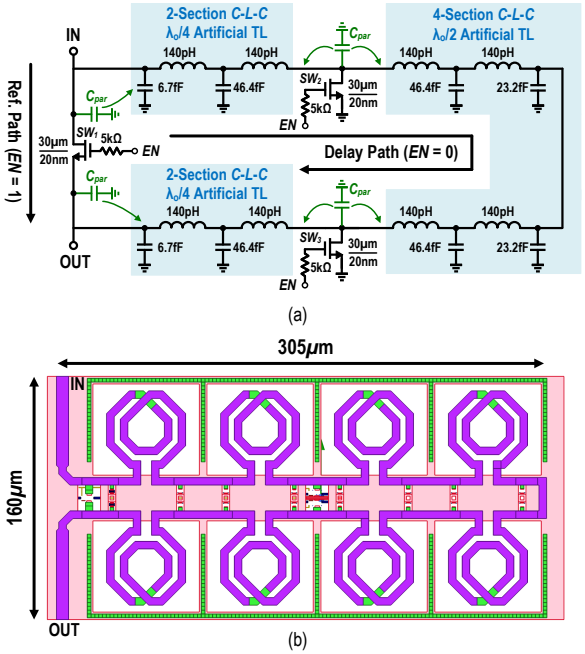

Fig. 3. Implementation of the proposed TTD stage at 40 GHz with a delay of 25 ps in a 22-nm CMOS SOI process: (a) circuit schematic with components' values (b) stage layout with a compact area of 160 μm × 305 μm.

at the target center frequency of operation, and a third section placed in the middle to arbitrarily provide any additional delay needed. With this delay-line arrangement, three simple SPST switches (SW_{1-3}) are utilized to control the TTD operation, eliminating the need for SPDT switches, and saving area and loss. In addition, all the parasitics of SW_{1-3} can be absorbed into the delay line, without adding any matching overhead. Fig. 2(c) shows the operation scheme of the proposed TTD stage. In the delay state, SW_{1-3} are all maintained open, and the signal propagates through the delay line. On the other hand, in the reference state, with SW_{1-3} being closed, the input and output impedances seen from the delay line are very high around the center frequency due to the action of the two

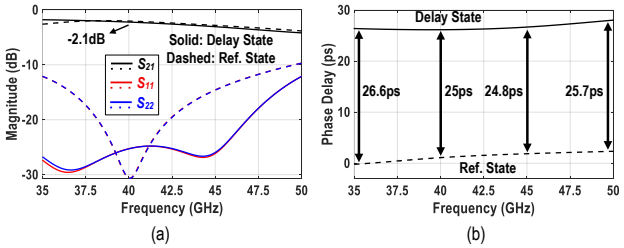

Fig. 4. Simulation results of the implemented 40-GHz 25-ps TTD stage in both reference and delay states: (a) S-parameters (b) phase delay.

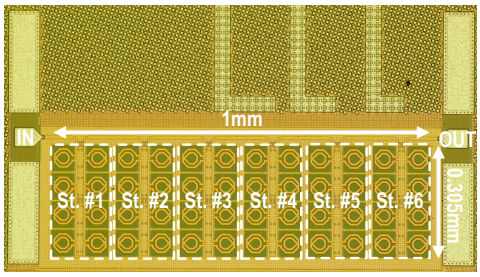

Fig. 5. Chip micrograph of the implemented 36-43-GHz 150-ps CMOS TTD.

$\lambda_o/4$ sections at the interfaces, causing the signal to propagate through SW_1 with eliminated delay-line loading. Further, by appropriately sizing SW_1, the IL of the reference state can be matched to that of the delay line, achieving embedded loss compensation without the need of bulky attenuators.

C. Implementation of a 40-GHz 25-ps TTD Stage

A 40-GHz TTD stage with a delay of 25 ps (i.e., one wavelength at 40 GHz) is implemented based on the proposed TTD architecture in a 22-nm CMOI SOI process. Fig. 3(a) shows the circuit implementation. Each $\lambda_o/4$ TL is implemented using a 2-section C-L-C artificial TL, with the parasitic capacitances of the switches (SW_{1-3}) being absorbed into the artificial TLs. The switch of the reference path (SW_1) is appropriately sized at 30μm/20nm to match the IL of the delay path, which is around 2 dB. As shown in Fig. 3(b), the TTD stage occupies a compact size of 160 μm $\times$ 305 μm, which is enabled by the SPDT-less, embedded loss compensation, and matching network-free features of the proposed TTD architecture. The simulation results of the TTD stage are summarized in Fig. 4, achieving a 10-dB matching bandwidth over 35-50 GHz with an IL of 2.1 dB at 40 GHz in both reference and delay states.

III. Prototype Measurement Results

A six-stage 40-GHz prototype of the proposed bandpass TTD architecture was fabricated in a 22-nm CMOS SOI process, with a delay range of 150 ps and a resolution of 25 ps. The die micrograph is shown in Fig. 5, occupying a compact core area of of 0.305 mm $\times$ 1 mm. On wafer characterization was performed to measure the S-parameters of the design, with SOLT calibration performed up to the tips of the probes. Fig. 6 shows the measurement and simulation results of the

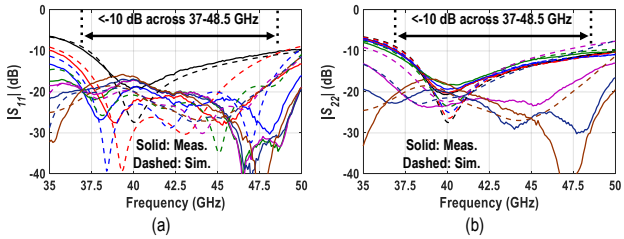

Fig. 6. Matching measurement and simulation results of the implemented 150-ps TTD across all the delay states: (a) S_{11} matching (b) S_{22} matching.

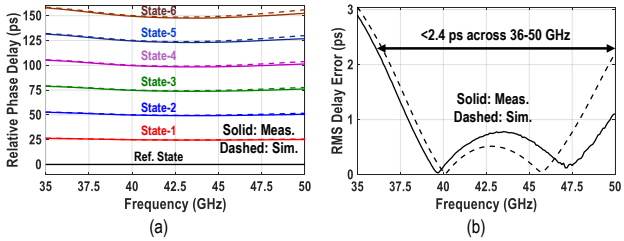

Fig. 7. Delay measurement and simulation results of the implemented 150-ps TTD: (a) relative phase delay of all the delay states (b) RMS delay error.

matching across all the delay states. The measured $|S_{11}|$ and $|S_{22}|$ are maintained below -10 dB across 37-48.5 GHz, with an excellent agreement to simulation results. The delay measurement and simulation results of all the TTD's states are summarized in Fig. 7. As shown in Fig. 7(a), the design achieves a phase delay range of 150 ps relative to the reference state with a resolution of 25 ps. Further, as shown in Fig. 7(b), the measured RMS delay error is lower than 2.4 ps (1.6% relative to the total delay range) across 36-50 GHz, demonstrating the high-precision feature of the proposed TTD architecture. The measured and simulated $|S_{21}|$ of all the delay states are shown in Fig. 8(a), with the average IL and RMS magnitude error presented in Fig. 8(b). At 38 GHz, the TTD design achieves a measured average IL of 13.8 dB with an RMS magnitude error of 0.32 dB. In addition, across 36-43 GHz, the measured average IL is within 13.8-16.9 dB and the RMS magnitude error is lower than 1.27 dB.

Table 1 summarizes the performance of the proposed 36-43-GHz TTD design in comparison to the state-of-the-art TTD implementations. Enabled by the SPDT-less, parasitics absorption, and embedded loss compensation features of

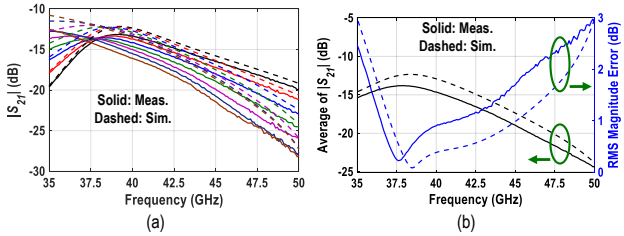

Fig. 8. Insertion loss measurement and simulation results of the implemented 150-ps TTD: (a) $|S_{21}|$ of all the delay states (b) average insertion loss and RMS magnitude error.

Table 1. Performance Comparison with the State-of-the-Art TTD Implementations

	This Work	TMTT'25 [10]	TMTT'24 [9]	MWTL'24 [8]	RFIC'14 [4]	MWCL'13 [1]	Nature'24 [7]	TMTT'20 [6]	RFIC'20 [5]
Technology	**22nm CMOS SOI**	65nm CMOS	65nm CMOS	65nm CMOS	0.25μm SiGe	0.13μm CMOS	45nm CMOS SOI	28nm CMOS	28nm CMOS
Frequency Range (GHz)	**36-43**	2-15	1-11	3-20	10-50	15-40	10-24	3-30	8-24
Delay Range (ps)	**150**	315	106.7	106	32.8	42	21	68.5	51.8
Delay Step (ps)	**25**	5	4.85	2.35	Cont.	5.2	0.16	4.9	7.4
Insertion Loss (dB)	**13.8-16.9**	11.9-36.8	2.8-15.5	5.7-17	13-22#	14^	8.1^	7.1-16.7	7.8-12
Loss Variation (dB)	**$\pm$1.9**	$\pm$2.4	$\pm$3.95#	$\pm$2	$\pm$5.3#	$\pm$2	$\pm$4.3#	$\pm$4.8#	$\pm$3#
RMS Delay Error (ps)	**<2.4**	<8.2	<4.6	<1.7	1.28&	N.A.	N.A.	<2	<1.6
RMS Magnitude Error (dB)	**<1.27**	<1.27	N.A.	N.A.	4.2#	1.6	N.A.	<3.2	N.A.
IP1dB (dBm)	**>8.5**	>3.3	11	5.8-9.8	15.5	N.A.	17	6.2	N.A.
Power Consumption (mW)	**Passive**	Passive	Passive	Passive	Passive	8.6-24.6	Passive	Passive	Passive
Core Area (mm^2)	**0.305**	0.72	0.35	0.314	0.22	0.99*	0.13	0.34	0.48
Delay/Area (ps/mm^2)	**491.8**	437.5	304.9	337.6	149.1	42.4	161.5	201.5	107.9
RMS-Delay-Error/Delay (%)	**1.6**	2.6	4.3	1.6	3.9	N.A.	N.A.	2.9	3.1
Insertion-Loss/Delay (dB/ps) (at 40 GHz)	**0.09-0.11 (0.10)**	0.04-0.12 (N.A.)	0.03-0.15 (N.A.)	0.05-0.16 (N.A.)	0.40-0.67 (0.55#)	0.33 (0.33#)	0.39 (N.A.)	0.10-0.24 (N.A.)	0.15-0.23 (N.A.)
Loss-Variation/Delay (dB/ps)	**$\pm$0.0127**	$\pm$0.0076	$\pm$0.037	$\pm$0.0189	$\pm$0.1616	$\pm$0.0476	$\pm$0.2048	$\pm$0.0701	$\pm$0.0579

#: Estimated from graphs ^: Average insertion loss across band &: Maximum delay error *: Total area including pads

the proposed TTD architecture, the reported TTD design simultaneously achieves: (1) the highest area efficiency compared to all other works, (2) the highest precision (lowest RMS delay error over total delay) compared to all other works, and (3) more than 3$\times$ reduction in insertion loss and loss variation per total delay compared to the TTD designs above 30 GHz ([1] and [4]).

IV. Conclusion

A bandpass passive TTD architecture with center-frequency performance optimization was reported. The passive TTD architecture is SPDT-less, matching networks-free, and parasitics-absorptive, simultaneously achieving high area efficiency, low IL, highly precise delay control, and low loss variations across the delay states. It can be designed with a minimum delay resolution of half-wavelength at the center frequency of operation, and is well suited to emerging hybrid wideband arrays. A 36-43-GHz CMOS prototype with a delay range of 150 ps demonstrates the state-of-the-art TTD performance with an area efficiency of 491.8 ps/mm^2 and an IL per delay of 0.1 dB/ps at 40 GHz.

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